RN821x_RN7213 V2
User Manual

Rev1.1

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Revision Histroy

version number	Release Date	reviewer	Main changes
V1.0	2023-10-18	Systems Department	First Release
V1.1	2023-12-xx		1、Correction of a clerical error, P46 was written as P48 2、Pin diagram revision: P22 P23 delete TC function; P31 P32 corresponds to D2F and CF_OUT serial number modification; RN8213 pin diagram is separated from RN8217; RN8211B pin diagram deletes P10 P11 P57 P50 P51 pulse forwarding and D2F output function, and deletes D2F output function on P32 P56 pin; 3、RN8213B Pin Special Description Modification 56 Pin Description 4、Pin Description Section Revises Pin Functions and Adds Notes on Functions Not Supported by the RN8213 and RN8211B 5、IOCNT Multiplexing Relationship Form Revised to Remove P36 P37 as a Functional Input Function for INT6 and INT7

Table of Contents

1 Overview

1.1 Introduction

Single-phase SOC chip RN821x V2 version and RN721x V2 version are the second generation of single-phase SOC chip of RENERGY, which optimizes the performance and expands the functions on the basis of the first generation, and is compatible with the first generation, i.e. V1 version.

V2 version and V1 version are pin-to-pin compatible in terms of chip hardware and register. Software library functions need to be upgraded to V2 version from V1 version. FLASH and SRAM are upgraded to 512KB and 96KB + 4KB respectively. Power consumption, the performance of the RTC and metering performance are optimized in V2 version along with the support for intelligent miniature circuit breaker applications, newly added ECC/AES/HASH/TRNG encryption hardware acceleration unit, DSP core coprocessor and SPI/UART support for DMA channel. Typical application fields include overseas single-phase meters, rail meters, intelligent power safety products, etc.

1.2 Product Features

1.2.1 Basic features

- Highly integrated: integrated 32bit ARM Cortex-M0, metering module, hardware termperature compensation RTC, LCD controller, DSP co-processor, encryption hardware acceleration.

- Wide voltage range:
  - The voltage range to ensure metering accuracy is 2.8V~5.5V;
  - Typical voltages over which the CPU mini-system can operate range from 1.8V to 5.5V;
  - GPIOs support interfacing with devices of different operating voltages.

- High performance:
  - Under the condition of 32.768KHz single crystal and 32.768KHz crystal + external high-frequency crystal, the maximum operating frequency of CPU is up to 29.4912MHz (32.768KHz, 1.8432MHz, 7.3728MHz, 14.7456MHz, 29.4912MHz optional);
  - The internal high-frequency RCH operates at up to 29.5 MHz with ±1% accuracy over the full temperature range and can be used as a backup clock;

- Low power consumption:
  - At 7.3728 MHz, the power consumption is about 3.5mA for single-phase smart meter application;
  - The power consumption of the system operating at 32 KHz is about 22μA;
  - The overall power consumption of the chip in sleep mode is about 7μA.

- High accuracy:
  - Less than 0.1% active error over 8000:1 dynamic range;
  - 5ppm typical temperature coefficient of metering reference;
  - The RTC has a second pulse error of less than ±5ppm within -25° C~70° C, with a minimum calibration scale of 0.0339ppm;

- Package:

- RN8213B V2: LQFP128L
- RN8217 V2 /RN8215 V2 /RN8213 V2: LQFP100L
- RN7213 V2 /RN8211B V2: LQFP64L

1.2.2 Processor

- ARM Cortex-M0 core;
- 512KBytes FLASH memory, erase and write up to 100,000 times, data retention time greater than 20 years;
- 96KBytes SRAM, of which up to 4KBytes is used for internal cache and 92KBytes is open for customer; the other 4KBytes SRAM is the encrypted module RAM, which can be used by the CPU if the encryption function is not used;
- Single cycle multiplier (32bit*32bit);
- CM0 has an embedded system timer;
- Various wake-up methods such as external interrupt;
- Complete and integrated software and hardware environment;
- CM0 independent reset, online upgrade does not need to reset the whole chip and does not affect the metering.

1.2.3 Metering

- Less than 0.1% active metering error over 8000:1 dynamic range;
- The typical temperature coefficient of reference voltage is 5ppm/° C;
- Support null line and live line dual-channel active power, reactive power, apparent power, current RMS metering at the same time;
- Support null line and live line dual-channel active power, reactive power and apparent power metering at the same time;
- Provides voltage RMS and voltage line frequency measurements;
- Provides sampling channel gain and offset correction functions;
- Provides power factor;
- Providing no voltage mode(NVM) metering solutions
- Providing DC metering solutions
- Voltage dips and drops event monitoring; current overload event monitoring; harmonic analysis solutions;
- Provide raw sampling data of three-way measurement sigma-delta ADC for algorithm development;
- Providing intelligent and safe power solutions
- Support Roche Coil
- Supports half-wave metering mode
- Supports bi-directional metering mode
- Supports base wave metering mode
- 3 independent configuration sets of metering constants
- Supports ADC input inversion
- External input for ADC (Channel IA and IB only)
- 4 types of power accumulation for active and reactive power: algebraic sum, positive, absolute value, negative
- Flexible ADC synchronized sampling of waveform data
- Flexible correction methods: gain correction, phase correction, harmonic compensation;
- Waveform data can be transferred from metering to RAM via DMA;

- Provides synchronized sampling of channel half-wave active power and half-wave RMS value
- Provide half-cycle updated full-wave voltage and current RMS, full-wave active power
- Provide half-cycle updated base wave voltage and current RMS, base wave active power
- Provide FLK module for flash-change hardware computing;
- Provide temperature coefficient compensation module ECT module for

1.2.4 RTC

- Hardware automatic temperature compensation to meet the national standards of precision and power consumption requirements;
- Temperature sensor: Provide accurate temperature value, temperature measurement accuracy is ±1℃ in the range of -25℃～70℃;

1.2.5 LCD

- Support 4*34, 6*32, 8*30 (LQFP100L); or 4*40, 6*38, 8*36 (LQFP128L);
- Support Charge pump mode, support wide voltage and full temperature range clear display;
- Supports Resistor Row Voltage Divider Mode Mode
- The two modes are hardware compatible, and if lower display power consumption is required, the resistor string divider method can be selected;
- Overall power consumption is better than 25μA.

1.2.6 Other peripherals

- High-speed GPIOs to support interfacing with peripheral devices of different voltages;
- 12bit ADC: Temperature sensor/battery voltage detection/general purpose ADC time-sharing multiplexing;
- Voltage Detection LVD: detects chip power supply voltage; detects external voltage.
- Two comparators, CMP1 and CMP2: detect external voltages with a power consumption of about 0.5uA, supporting low-power power monitoring under power failure.
- Timers: 2 32bit extended timers, 2 RTC timers, 1 CM0 embedded system timer, 4 32bit simple timers;
- UART: up to 6, support auto baud rate, support infrared modulation, support UART wake-up, support level inversion, support DMA, note that DMA is not compatible with v1 version
- 7816 ports: 2
- I2C: 1
- SPI: 4, supports DMA, note that DMA is not compatible with V1 version
- LPUART: 1 low-power UART, supports up to 9600 baud rate, infrared modulation, and 4 wake-up modes;
- Watchdog: Hardware watchdog;
- Key interrupts: up to 8, pin-multiplexed;
- External interrupts: up to 8, pin-multiplexed;
- Power Integration Unit D2F: Provides 12 D2F integrators, 3 of which support pulse output.
- Memory Handling Unit M2M: 1 M2M module that enables memory data handling.
- Provides pulse forwarding function IOCNT
- Provides 7/8/16/32-bit CRC test

1.2.7 DSP coprocessor

- Supports interconversion of integers and floating point numbers.
- Supports floating-point addition, subtraction, multiplication, and division.
- Supports single butterfly (plural) and DMA sequential butterfly operations
- Supports base-2FFT in its entirety, supporting point counts of 64, 128, 256, 512, 1024

- Support bit reverse automatic data transfer operation, support points 4, 8, 16, 32, 64, 128, 256, 512, 1024
- Supports sine and cosine calculations
- Calculation of the root mean square of support
- Support for Arbitrary Cut Calculations
- Supports IIR single computation, supports IIR DMA computation
- Supports FIR filtering operations
- Supports linear interpolation
- Supports Lagrange interpolation

1.2.8 Encryption

(Incompatible with V1 version, need to re-modify the application)

- Hardware true random number generator, compliant with NIST's FIPS 140-2 standard;
- AES hardware acceleration unit;
- ECC hardware acceleration unit;
- RSA hardware acceleration unit;
- HASH hashing algorithm hardware acceleration unit;
- Documentation for encryption instructions is available in the Renegade Micro Application Notes;

1.2.9 Cartesian segregation

- Provide card meter isolation low cost and high reliability solution, see the description of RN8501 card isolation solution of RENERGY;

1.3 SOC Product Model List

Product Model	FLASH	RAM	Measurement ADC	LCD	VCC and VBAT switching	Encryption	DSP Core	Package
RN8213B	512KB	96KB+ 4KB	3-way	√	√	√	√	LQFP128L
RN8217	512KB	96KB+ 4KB	3-way	√	√	√	√	LQFP100L
RN8215								
RN7213	512KB	96KB+ 4KB	3-way	×	√	√	√	LQFP64L
RN8213	256KB	32KB	3-way	√	√	×	×	LQFP100L
RN8211B	256KB	32KB	3-way	√	×	×	×	LQFP64L

Table 1-1 List of SOC Product Models

1.4 SOC Product Resource Cross Reference

model number		RN8213B	RN8217 RN8215	RN7213	RN8213	RN8211B
CPU		Cortex-M0				
Max Freq.		29.4912M				
flash		512KB	512KB	512KB	256KB	256KB
CACHE		√	√	√	×	×
RAM		96KB+4KB	96KB+4KB	96KB+4KB	32KB	32KB
Cryptographic SEA		√	√	√	×	×
TRNG		√	√	√	×	×
Timers	32bit Timer	2	2	2	2	2
	32bit Simptc	4	4	4	4	4
	systick	1	1	1	1	1
RTC		1	1	1	1	1
WDT		1	1	1	1	1
KBI		8	8	6	6	5
INTC		8	8	8	8	4
SPI		4	4	4	4	2
UART		6	5	5	5	4
I2C		1	1	1	1	1
7816		2	2	2	0	0
GPIO		108	82	46	46	48
DMA		√				
Measurement EMU		√				
DSP		√	√	√	×	×
D2F		√	√	√	×	×
M2M		√	√	√	×	×

LPUART	√	√	√	×	×
ECT	√	√	√	×	×
FLK	√	√	√	×	×
CRC	√	√	√	×	×
IOCNT	√	√	√	×	×
LCD	4*40/6*38/8*36	4*34/6*32/8*30	×	4*34/6*32/8*30	4*16/6*14/8*12
CMP	2	2	1	2	2
LVD	1	1	0	1	0
Measurement ADC	3	3	3	3	3
SAR-ADC	7	6	5	6	5
TempSensor	√				

Table 1-2 SOC Product Resource Comparison Table

1.5 System Block Diagram

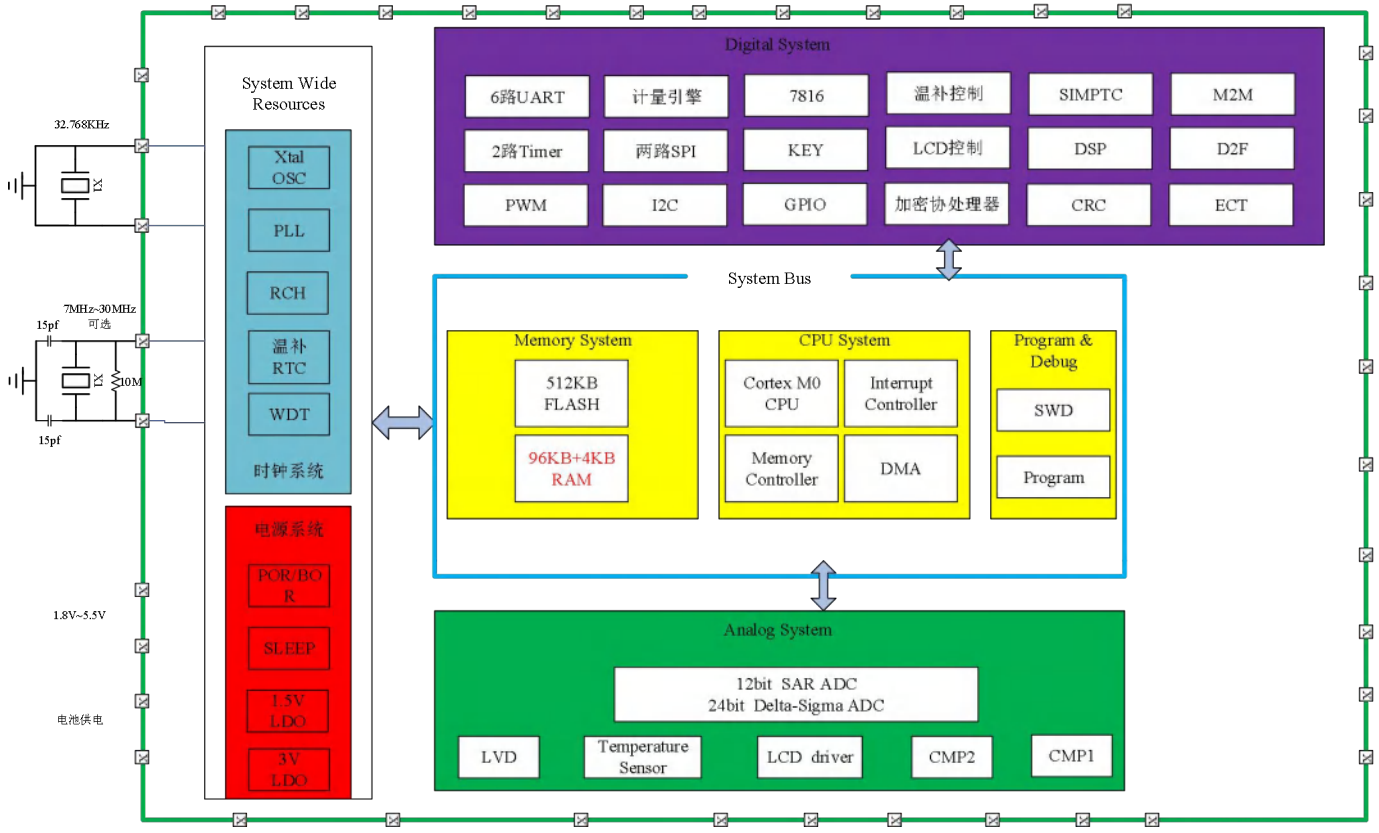


Figure 1.1 Block diagram of single-phase SOC system

1.6 Pin Description

1.6.1 RN8213B LQFP128L Pinouts

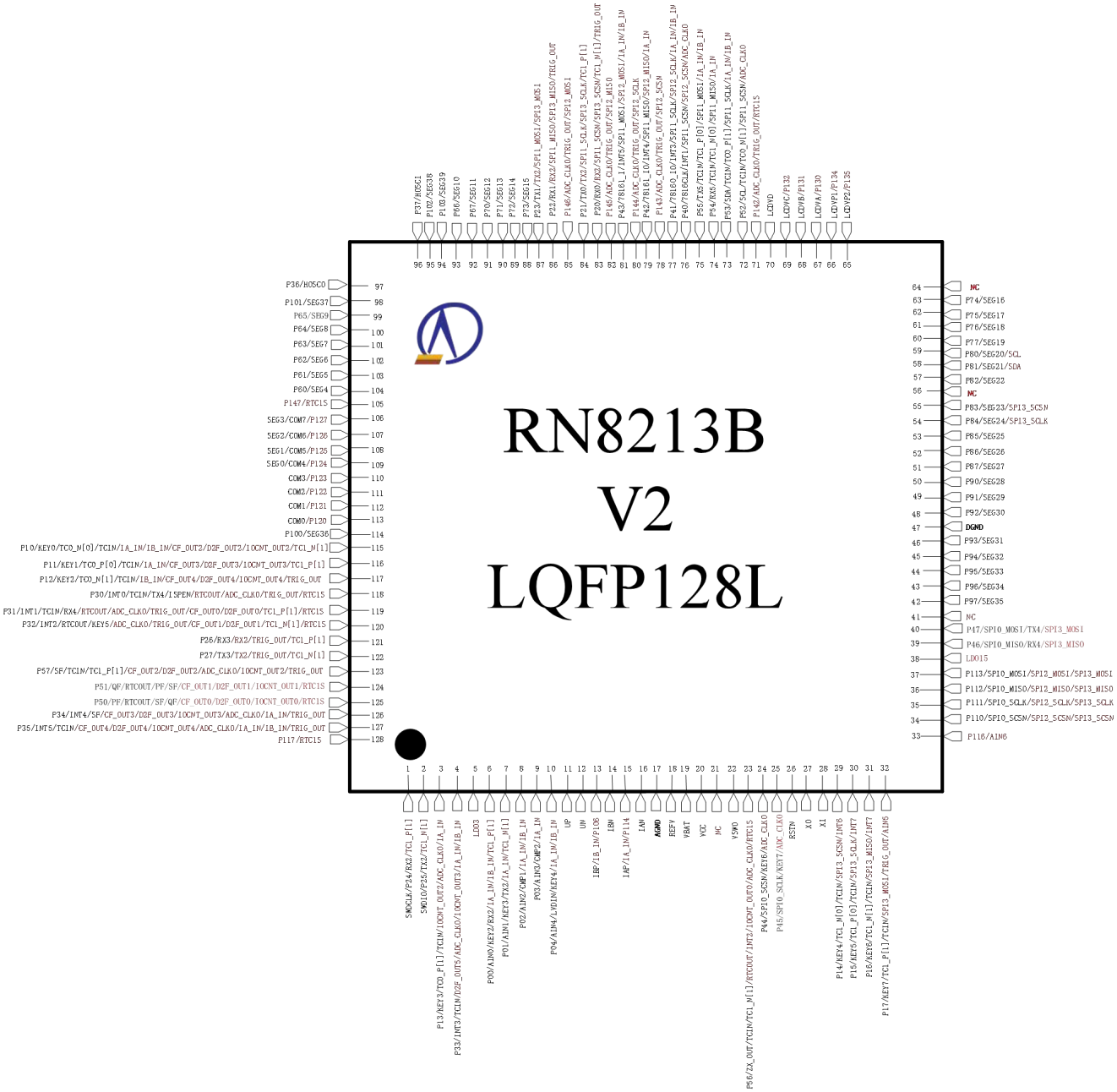


Figure 1-2 RN8213B Pin Arrangement Diagram

PIN pin differences are described:

The RN8213B V2 adds 22 new IOs, 13 of which are multiplexed with the original LCD pins, and the other 10 new IOs were originally ground, power, or NC pins, and are modified to be backward compatible by default.

model number	PIN pin	v1	V2 version	quantities	clarification
RN8213B	5	LDO33	LDO3	1	modifications
	33	DGND	P116/AIN6	1	additional

	38	LDO18	LDO15	1	modifications
	41	DGND	NC, requires suspension, not grounded	1	additional
	56	DGND	P141/ADC_CLKO /TRIG_OUT/RTC1S	1	additional
	64	DGND	NC Pin, Dangling	1	additional
	65~69	LCD	P135/P134,P130~P132	5	additional
	71	DGND	p142/adc_clko/trig_out/rtc1s	1	additional
	78	NC	p143/adc_clko/trig_out/spi2_scsn	1	additional
	80	DVDD	p144/adc_clko/trig_out/spi2_sclk	1	additional
	82	DGND	P145/ADC_CLKO/TRIG_OUT/SPI2_MISO, the output only supports open-drain output, and needs to be configured to open-drain mode when used.	1	additional
	85	DGND	p146/adc_clko/trig_out/spi2_mosi	1	additional
	105	DGND	p147/adc_clko/trig_out/rtc1s	1	additional
	106~113	SEG/COM	P127~P120	8	additional
	128	DGND	P117/RTC1S	1	additional

1.6.2 RN8217/RN8215/RN8213 LQFP100L Pinouts

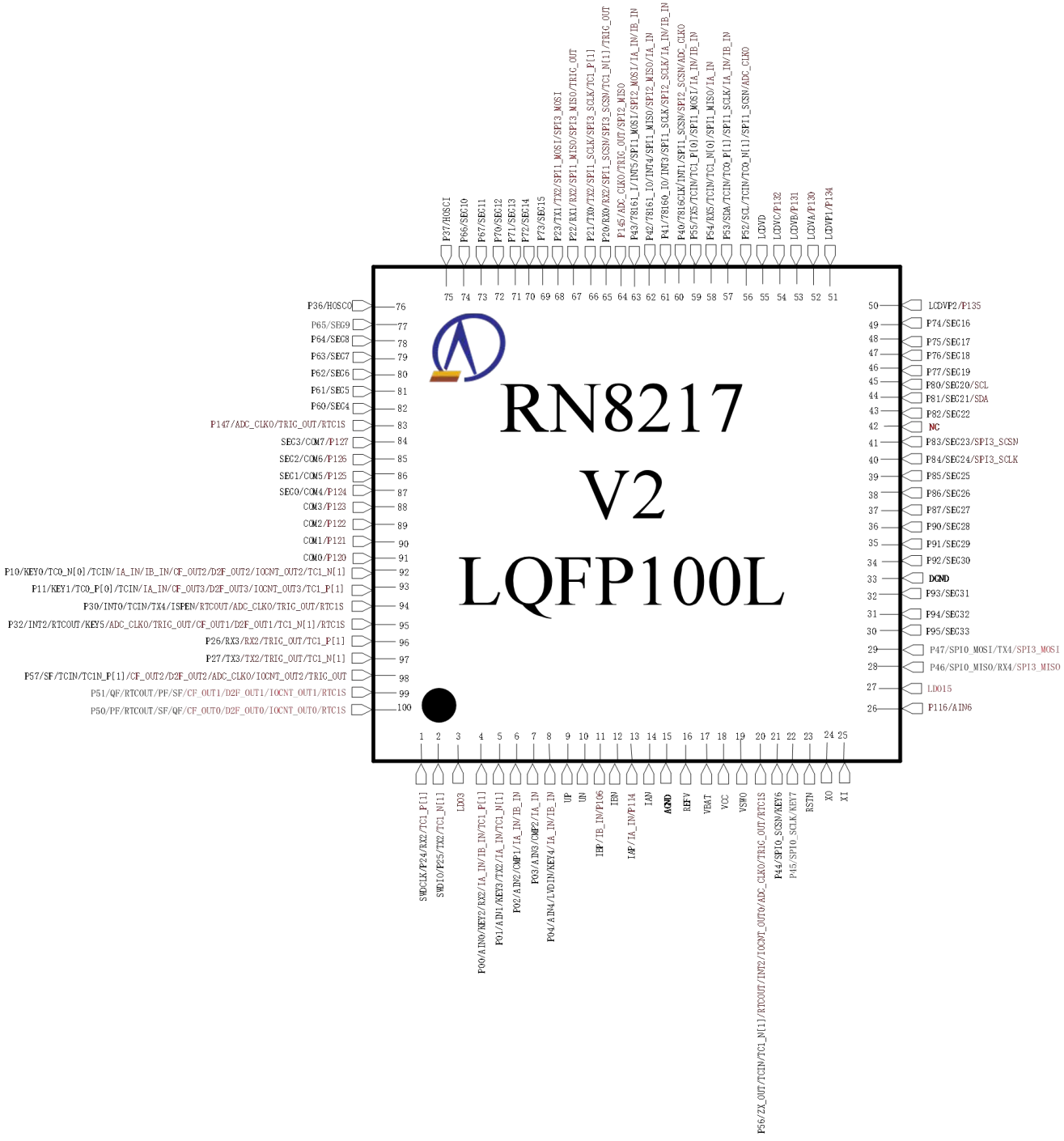


Figure 1-3 RN8217/RN8215/RN8213 Pin Arrangement Diagram

PIN pin differences are described:

The RN8217 V2 adds 16 new IOs, 13 of which are multiplexed with the original LCD pins, and the other 3 new IOs were originally ground pins, which are modified to be backward compatible by default.

model number	PIN pin	v1	V2 version	quantities	clarification
RN8217	3	LDO33	LDO3	1	modifications

	26	DGND	P116/AIN6	1	additional
	27	LDO18	LDO15	1	modifications
	42	DGND	NC Pin, Dangling	1	additional
	50~54	LCD	P135/P134,P130~P132	5	additional
	64	DGND	P145/ADC_CLKO/TRIG_OUT/SPI2_MISO, the output only supports open-drain output, and needs to be configured to open-drain mode when used.	1	additional
	83	DGND	p147/adc_clko/trig_out/rtc1s	1	additional
	84~91	SEG/COM	P127~P120	8	additional

1.6.3 RN8213 LQFP100L Pinouts

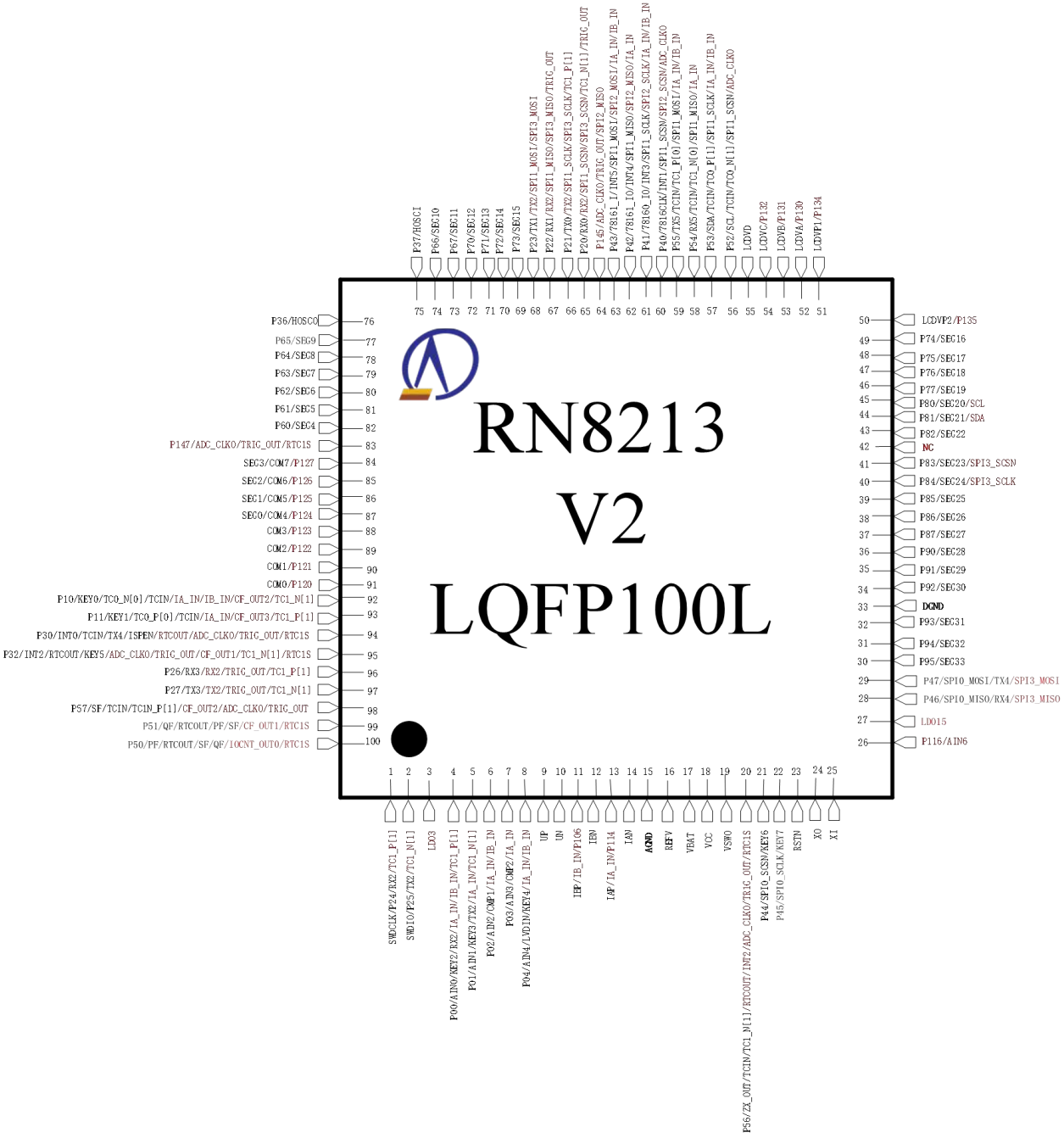


Figure 1-3 RN8217/RN8215/RN8213 Pin Arrangement Diagram

PIN pin differences are described:

The RN8213 V2 adds 16 new IOs, 13 of which are multiplexed with the original LCD pins, and the other 3 new IOs were originally ground pins, which are modified to be backward compatible by default.

model number	PIN pin	v1	V2 version	quantities	clarification
RN8213	3	LDO33	LDO3	1	modifications

	26	DGND	P116/AIN6, open-drain pin, external pull-up resistor required for outputs	1	additional
	27	LDO18	LDO15	1	modifications
	42	DGND	NC Pin, Dangling	1	additional
	50~54	LCD	P135/P134,P130~P132	5	additional
	64	DGND	P145/ADC_CLKO/TRIG_OUT/SPI2_MISO, the output only supports open-drain output, and needs to be configured to open-drain mode when used.	1	additional
	83	DGND	p147/adc_clko/trig_out/rtc1s	1	additional
	84~91	SEG/COM	P127~P120	8	additional

1.6.4 RN7213 LQFP64L Pinouts

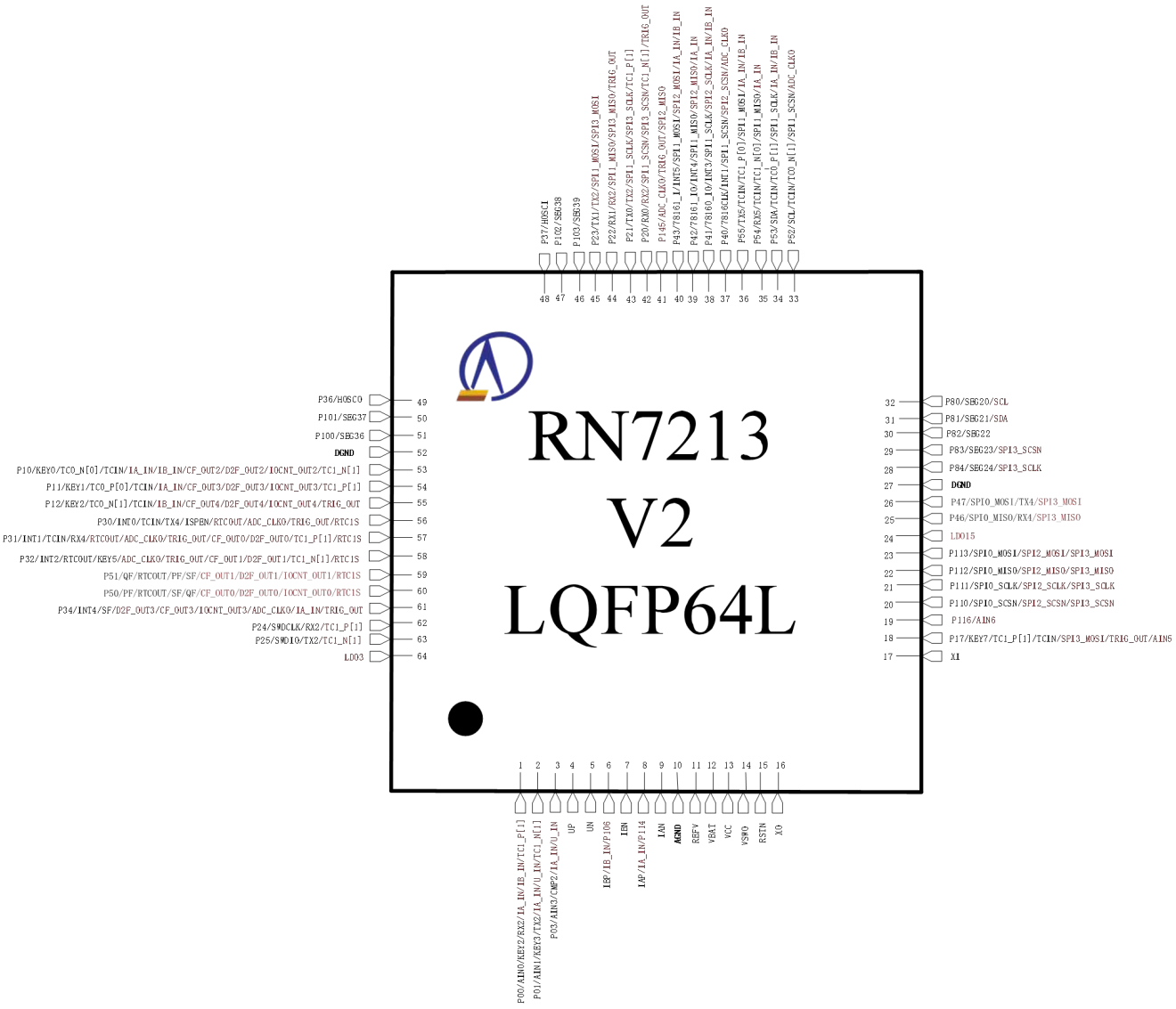


Figure 1-4 RN7213 Pin Arrangement Diagram

PIN pin differences are described:

The RN7213 V2 adds 2 new IOs. The 2 new IOs were originally ground pins and are modified to be backward compatible by default.

model number	PIN pin	v1	V2 version	quantities	clarification
RN7213	19	DGND	P116/AIN6, open-drain pin, external pull-up resistor required for outputs	1	additional
	24	LDO18	LDO15	1	modifications
	41	DGND	P145/ADC_CLKO/TRIG_OUT/SPI2_MISO, the output only supports open-drain output, and needs to be configured to open-drain mode when used.	1	additional
	64	LDO33	LDO3	1	modifications

1.6.5 RN8211B LQFP64L Pinouts

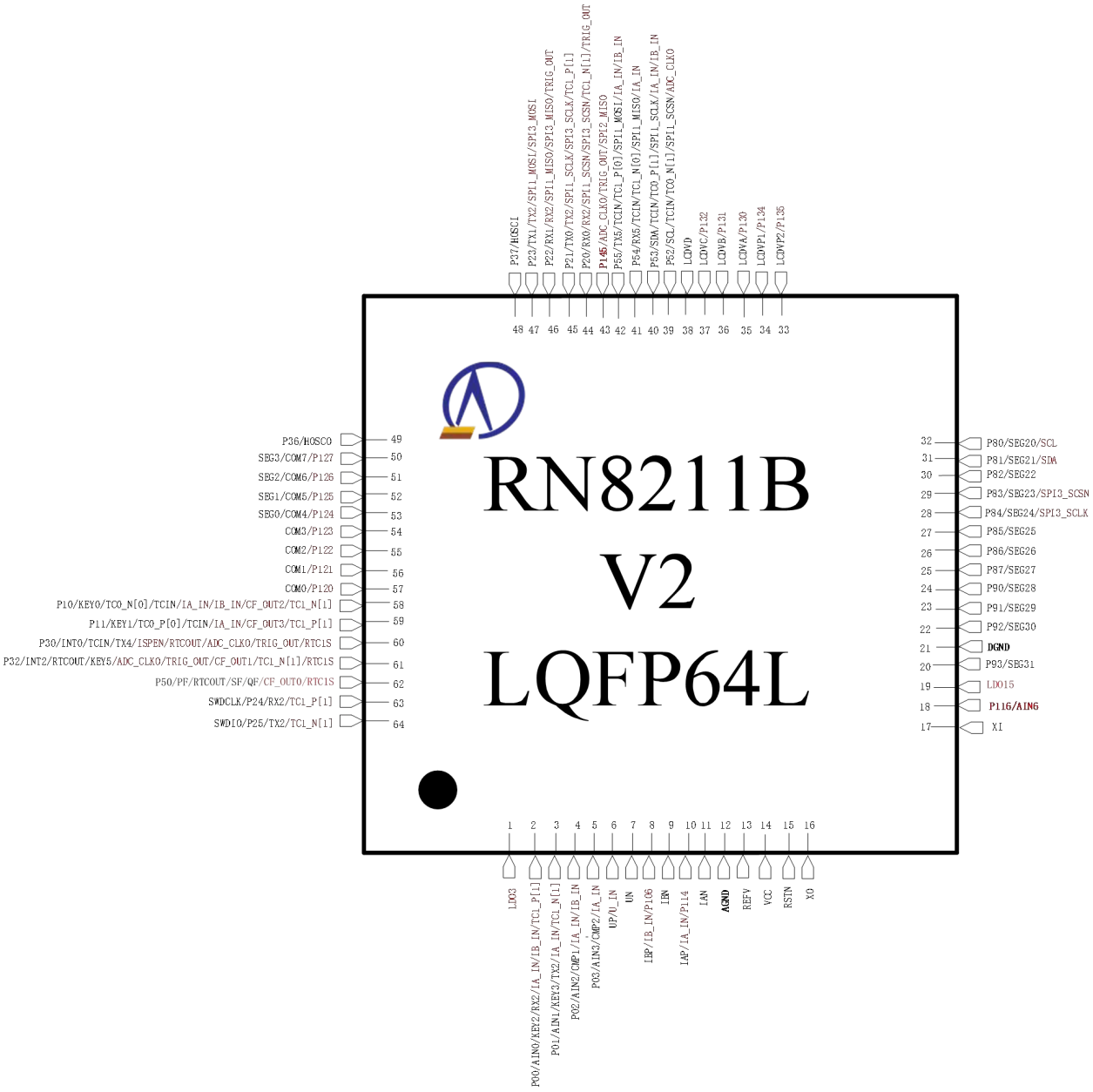


Figure 1-6 RN8211B Pin Arrangement Diagram

PIN pin differences are described:

The RN8211B V2 adds 15 new IOs, 13 of which are multiplexed with the original LCD pins, and the other 2 new IOs were originally ground pins, which are modified to be backward compatible by default.

model number	PIN pin	v1	V2 version	quantities	clarification
RN8211B	1	LDO33	LDO3	1	modifications
	18	DGND	P116/AIN6, open-drain pin, external pull-up resistor required for outputs	1	additional
	19	LDO18	LDO15	1	modifications
	33~37	LCD	P135/P134,P130~P132	5	additional

	43	DGND	P145/ADC_CLKO/TRIG_OUT/SPI2_MISO, the output only supports open-drain output, and needs to be configured to open-drain mode when used.	1	additional
	50~57	SEG/COM	P127~P120	8	additional

1.6.6 Pin Type Description

TYPE	Cell Type				Input Option				Osc Option	Lcd Option	Adc Option	Output Option	
	ANA	DUAL	IN	OUT	UP	DOWN	Schmitt	TTL/ CMOS	crystal oscillator	SEG /COM	ADC	Open Drain	LOAD
	A	B	I	o	U	D	S	L	X	G	C	D	
PABULD3	√	√			√			√				√	3mA
PABUS3	√	√			√		√						3mA
PBDS3		√				√	√					water clock	3mA
PBDSG3		√				√	√			√		water clock	3mA
PBULD3		√			√			√				√	3mA
PBULD6		√			√			√				√	6mA
PBUS6		√			√		√						6mA
PILC			√								√		
PID			√			√							
PIU			√		√								
PIUX			√		√				√				

1.6.7 Pin Definition Description

RN8213B	RN8213 RN8215 RN8217	RN7213	RN8211B	Type	Pin Function	Descriptions
1	1	62	63	PBULD3	P24	GPIO
					SWDCLK	SWD Clock Port
					RX2	UART2 receive
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
2	2	63	64	PBULD3	P25	GPIO
					SWDIO	SWD Data Port
					TX2	UART2 Transmit
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
3				PBULD3	P13	GPIO

					KEY3	External Interrupt Input
					TC0_P[1]	Timer 0 Channel 1 Compare Positive Outputs
					TCIN	Timer Input
					IOCNT_OUT2	Pulse forwarding output 2
					ADC_CLKO	ADC Clock Output
					IA_IN	IA channel external 1bit input
4				PBUS6	P33	GPIO
					INT3	External Interrupt Input
					TCIN	Timer Input
					IOCNT_OUT3	Pulse forwarding output 3
					ADC_CLKO	ADC Clock Output
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
5	3	64	1	power supply	LDO3	The output of the built-in 3V LDO, which powers the ADC, should be decoupled with an external 1uf capacitor in parallel with a 0.1uf capacitor.
6	4	1	2	PABUS3	P00	GPIO
					AIN0	SAR-ADC input
					KEY2	keystroke input
					RX2	UART2 receive
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
7	5	2	3	PABUS3	P01	GPIO
					AIN1	SAR-ADC input
					KEY3	keystroke input
					TX2	UART2 Transmit
					IA_IN	IA channel external 1bit input
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
8	6		4	PABUS3	P02	GPIO
					AIN2	SAR-ADC input
					CMP1	Comparator 1 input
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input

9	7	3	5	PABUS3	P03	GPIO
					AIN3	SAR-ADC input
					CMP2	Comparator 2 input
					IA_IN	IA channel external 1bit input
10	8			PABUS3	P04	GPIO
					AIN4	SAR-ADC input
					LVDIN	Power-down detection input
					KEY4	keystroke input
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
11	9	4	6	PILC	UP	Voltage channel positive input
12	10	5	7	PILC	UN	Voltage channel negative input
13	11	6	8	PILC	IBP	Current channel IB positive input
					IB_IN	IB channel external 1bit input
					P106	GPIO function is not supported
14	12	7	9	PILC	IBN	Current channel IB negative input
15	13	8	10	PILC	IAP	Current channel IA positive input
					IA_IN	IA channel external 1bit input
					P114	GPIO function is not supported
16	14	9	11	PILC	IAN	Current channel IA negative input
17	15	10	12	Ground	AGND	analogically
18	16	11	13	power source	REFV	The 1.25V reference voltage of the metering ADC can also be connected to an external irrigation reference; it should be decoupled by an external 1uf capacitor connected in parallel with a 0.1uf capacitor.
19	17	12		power source	VBAT	Battery or supercapacitor input pin
20	18	13		power source	VCC	The mains power input, should be externally connected to a 4.7uf capacitor and decoupled with a 0.1uf capacitor.
21				NC	NC	NC pin, can be left open, grounded or connected to power supply
22	19	14	14	power source	VSWO	The power output after switching between VCC and VBAT to supply power to the chip should be decoupled with an external 1uf capacitor and connected with a 0.1uf capacitor.
23	20			PBULD6	P56	GPIO, 6mA drive capability in V2, 3mA in V1
					RTCOUT	RTCOUT output
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted

						Outputs
					TCIN	Timer Input
					ZX_OUT	Voltage Over Zero Output
					INT2	External Interrupt Input
					IOCNT_OUT0	Pulse forwarding output 0 (not available on RN8213 and RN8211B)
					ADC_CLKO	ADC Clock Output
					RTC1S	Perpetual calendar 1HZ second pulse output
24	21			PBULD3	P44	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY6	keystroke input
					SPI0_SCSN	SPI chip select
					ADC_CLKO	ADC Clock Output
25	22			PBULD3	P45	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY7	keystroke input
					SPI0_CLK	SPI clock
					ADC_CLKO	ADC Clock Output
26	23	15	15	PIU	RSTN	PIN reset input
27	24	16	16	clocks	P_LXO	32.768KHz passive crystal output.
28	25	17	17	clocks	P_LXI	32.768KHz passive crystal input. The XI/XO does not require external resistors and capacitors and needs to be isolated by ground wires. It is recommended to choose a crystal with a load capacitance of 12.5pF.
29				PBULD3	P14	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY4	keystroke input
					TC1_N[0]	Timer 1 channel 0 compare reverse output
					TCIN	Timer Input

					SPI3_SCSN	SPI3 chip select
					INT6	External Interrupt Input
30				PBULD3	P15	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY5	keystroke input
					TC1_P[0]	Timer 1 Channel 0 Compare Positive Outputs
					TCIN	Timer Input
					SPI3_SCLK	SPI3 Clock
					INT7	External Interrupt Input
31				PBULD3	P16	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY6	keystroke input
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
					TCIN	Timer Input
					SPI3_MISO	SPI data
					TRIG_OUT	Intelligent micro-breakout output signal
32		18		PABULD3	P17	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					KEY7	keystroke input
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
					TCIN	Timer Input
					SPI3_MOSI	SPI3 Data
					TRIG_OUT	Intelligent micro-breakout output signal
					AIN5	SAR-ADC input
33	26	19	18	PABULD3	P116	GPIO, new IO in V2, P116/AIN6, open-drain pin, external pull-up resistor required for output
					AIN6	SAR-ADC input

34		20		PBULD3	P110	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_SCSN	SPI0 chip select
					SPI2_SCSN	SPI2 chip select
					SPI3_SCSN	SPI3 chip select
35		21		PBULD3	P111	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_SCLK	SPI0 Clock
					SPI2_SCLK	SPI2 Clock
					SPI3_SCLK	SPI3 Clock
36		22		PBULD3	P112	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_MISO	SPI0 Data
					SPI2_MISO	SPI2 Data
					SPI3_MISO	SPI3 Data
37		23		PBULD3	P113	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_MOSI	SPI0 Data
					SPI2_MOSI	SPI2 Data
					SPI3_MOSI	SPI3 Data
38	27	24	19	power supply	LDO15	Built-in 1.5V LDO output to power digital 1.5V domain, external 1uF+0.1uF decoupling capacitor

39	27	25		PBULD3	P46	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_MISO	SPI0 Data
					RX4	UART4 receive
					SPI3_MISO	SPI3 Data
40	29	26		PBULD3	P47	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SPI0_MOSI	SPI0 Data
					TX4	UART4 Transmit
					SPI3_MOSI	SPI3 Data
41				PBULD3	NC	Suspended, not grounded
42				PBDSG3	P97	GPIO
					SEG35	LCD driver SEG port
43				PBDSG3	P96	GPIO
					SEG34	LCD driver SEG port
44	30			PBDSG3	P95	GPIO
					SEG33	LCD driver SEG port
45	31			PBDSG3	P94	GPIO
					SEG32	LCD driver SEG port
46	32		20	PBDSG3	P93	GPIO
					SEG31	LCD driver SEG port
47	33	27	21	Ground	DGND	Ground
48	34		22	PBDSG3	P92	GPIO
					SEG30	LCD driver SEG port
49	35		23	PBDSG3	P91	GPIO
					SEG29	LCD driver SEG port
50	36		24	PBDSG3	P90	GPIO
					SEG28	LCD driver SEG port
51	37		25	PBDSG3	P87	GPIO
					SEG27	LCD driver SEG port
52	38		26	PBDSG3	P86	GPIO
					SEG26	LCD driver SEG port
53	39		27	PBDSG3	P85	GPIO
					SEG25	LCD driver SEG port
54	40	28	28	PBDSG3	P84	GPIO

					SEG24	LCD driver SEG port
					SPI3_SCLK	SPI3 Clock
55	41	29	29	PBDSG3	P83	GPIO
					SEG23	LCD driver SEG port
					SPI3_SCSN	SPI3 chip select
56	42			PBULD3	P141	GPIOs, new IOs in V2 version
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					RTC1S	Perpetual calendar 1HZ second pulse output
57	43	30	30	PBDSG3	P82	GPIO
					SEG22	LCD driver SEG port
58	44	31	31	PBDSG3	P81	GPIO
					SEG21	LCD driver SEG port
					SDA	I2C data
59	45	32	32	PBDSG3	P80	GPIO
					SEG20	LCD driver SEG port
					SCL	I2C clock
60	46			PBDSG3	P77	GPIO
					SEG19	LCD driver SEG port
61	47			PBDSG3	P76	GPIO
					SEG18	LCD driver SEG port
62	48			PBDSG3	P75	GPIO
					SEG17	LCD driver SEG port
63	49			PBDSG3	P74	GPIO
					SEG16	LCD driver SEG port
64				NC	NC	NC Pin, Dangling
65	50		33	PBDS3	P135	GPIOs, new IOs in V2 version
					LCDVP2	For analog output, a 100nF capacitor should be connected between LCDVP2 and LCDVP1. The LCD can be suspended if using the resistor divider method.
66	51		34	PBDS3	P134	GPIOs, new IOs in V2 version
					LCDVP1	ibid
67	52		35	PBDS3	P130	GPIOs, new IOs in V2 version
					LCDVA	For LCD voltage output, an external 470nF capacitor is required. This capacitor is required regardless

						of whether a charge pump or resistor voltage divider is used.
68	53		36	PBDS3	P131	GPIOs, new IOs in V2 version
					LCDVB	LCD voltage output, external 470nF capacitor is required.
69	54		37	PBDS3	P132	GPIOs, new IOs in V2 version
					LCDVC	LCD voltage output, external 470nF capacitor is required.
70	55		38	PBDS3	LCDVD	LCD voltage output, external 470nF capacitor is required.
71				PBULD3	P142	GPIOs, new IOs in V2 version
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					RTC1S	Perpetual calendar 1HZ second pulse output
72	56	33	39	PBULD3	P52	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SCL	I2C clock
					TC0_N[1]	Timer 0 Channel 1 Compare Inverted Outputs
					TCIN	Timer Input
					SPI1_SCSN	SPI1 chip select
					ADC_CLKO	ADC Clock Output
73	57	34	40	PBULD3	P53	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					SDA	I2C data
					TC0_P[1]	Timer 0 Channel 1 Compare Positive Outputs
					TCIN	Timer Input
					SPI1_SCLK	SPI1 Clock
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
74	58	35	41	PBULD3	P54	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable,

						please refer to GPIO_IOCFG register for details
					RX5	UART5 receive
					TC1_N[0]	Timer 1 Channel 0 Compare Inverted Outputs
					TCIN	Timer Input
					SPI1_MISO	SPI1 Data
					IA_IN	IA channel external 1bit input
75	59	36	42	PBULD3	P55	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					TX5	UART5 Transmit
					TC 1_P[0]	Timer 1 Channel 0 Compare Positive Outputs
					SPI1_MOSI	SPI1 Data
					TCIN	Timer Input
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
76	60	37		PBULD3	P40	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					7816CLK	7816 Clock Output
					INT1	External Interrupt Input
					SPI1_SCSN	SPI chip select
					SPI2_SCSN	SPI chip select
					ADC_CLKO	ADC Clock Output
77	61	38		PBULD3	P41	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					78160_IO	7816 0 Bidirectional Data Port
					INT3	External Interrupt Input
					SPI1_SCLK	SPI clock
					SPI2_SCLK	SPI clock

					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
78				PBULD3	P143	GPIO, new IO for V2, V2 driver capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					SPI2_SCSN	SPI chip select
79	62	39		PBULD3	P42	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					78161_IO	7816 1 bidirectional data port
					INT4	External Interrupt Input
					SPI1_MISO	SPI data
					SPI2_MISO	SPI data
					IA_IN	IA channel external 1bit input
80				PBULD3	P144	GPIO, new IO for V2, V2 driver capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					SPI2_SCLK	SPI clock
81	63	40		PBULD3	P43	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					78161_I	7816 1 Data Input
					INT5	External Interrupt Input
					SPI1_MOSI	SPI data
					SPI2_MOSI	SPI data
					IA_IN	IA channel external 1bit input

					IB_IN	IB channel external 1bit input
82	64	41	43	PBDS3	P145	GPIO, new IO in V2 version, only support open-drain output, need to configure open-drain mode when using, V2 version drive capability 3mA(default)/1.5mA can be configured, please refer to GPIO_IOCFG register for details.
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					SPI2_MISO	SPI data
83	65	42	44	PBULD3	P20	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					RX0	UART0 receive
					RX2	UART2 receive
					SPI1_SCSN	SPI chip select
					SPI3_SCSN	SPI chip select
					TRIG_OUT	Intelligent micro-breakout output signal
84	66	43	45	PBULD3	P21	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					TX0	UART0 Transmit
					TX2	UART2 Transmit
					SPI1_SCLK	SPI clock
					SPI3_SCLK	SPI clock
85				PBULD3	P146	GPIO, new IO for V2, V2 driver capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal

					SPI2_MOSI	SPI data
86	67	44	46	PBULD3	P22	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					RX1	UART1 receive
					RX2	UART2 receive
					SPI3_MISO	SPI data
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
					TRIG_OUT	Intelligent micro-breakout output signal
87	68	45	47	PBULD3	P23	GPIO, version V2 drive capability 3mA(default)/1.5mA configurable, please refer to GPIO_IOCFG register for details
					TX1	UART1 Transmit
					TX2	UART2 Transmit
					SPI3_MOSI	SPI data
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
88	69			PBDSG3	P73	GPIO
					SEG15	LCD driver SEG port
89	70			PBDSG3	P72	GPIO
					SEG14	LCD driver SEG port
90	71			PBDSG3	P71	GPIO
					SEG13	LCD driver SEG port
91	72			PBDSG3	P70	GPIO
					SEG12	LCD driver SEG port
92	73			PBDSG3	P67	GPIO
					SEG11	LCD driver SEG port
93	74			PBDSG3	P66	GPIO
					SEG10	LCD driver SEG port
94		46		PBDSG3	P103	GPIO
					SEG39	LCD driver SEG port
95		47		PBDSG3	P102	GPIO
					SEG38	LCD driver SEG port
96	75	48	48	PIUX	P37	GPIO
					INT7	External Interrupt Input

					HOSCI	A 10M ohm resistor should be connected in series between the HF crystal input port, and the HOSCO, and a 15pf capacitor to ground in parallel.
97	76	49	49	PIUX	P36	GPIO
					INT6	External Interrupt Input
					HOSCO	A 10M ohm resistor should be connected in series between the HF crystal output port, and the HOSCI, and a 15pf capacitor to ground in parallel.
98		50		PBDSG3	P101	GPIO
					SEG37	LCD driver SEG port
99	77			PBDSG3	P65	GPIO
					SEG9	LCD driver SEG port
100	78			PBDSG3	P64	GPIO
					SEG8	LCD driver SEG port
101	79			PBDSG3	P63	GPIO
					SEG7	LCD driver SEG port
102	80			PBDSG3	P62	GPIO
					SEG6	LCD driver SEG port
103	81			PBDSG3	P61	GPIO
					SEG5	LCD driver SEG port
104	82			PBDSG3	P60	GPIO
					SEG4	LCD driver SEG port
105	83			PBULD3	P147	GPIOs, new IOs in V2 version
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					RTC1S	Perpetual calendar 1HZ second pulse output
106	84		50	PBDSG3	P127	GPIOs, new IOs in V2 version
					SEG3	LCD driver SEG port
					COM7	LCD driver COM port
107	85		51	PBDSG3	P126	GPIOs, new IOs in V2 version
					SEG2	LCD driver SEG port
					COM6	LCD driver COM port
108	86		52	PBDSG3	P125	GPIOs, new IOs in V2 version
					SEG1	LCD driver SEG port
					COM5	LCD driver COM port
109	87		53	PBDSG3	P124	GPIOs, new IOs in V2 version

					SEG0	LCD driver SEG port
					COM4	LCD driver COM port
110	88		54	PBDSG3	P123	GPIOs, new IOs in V2 version
					COM3	LCD driver COM port
111	89		55	PBDSG3	P122	GPIOs, new IOs in V2 version
					COM2	LCD driver COM port
112	90		56	PBDSG3	P121	GPIOs, new IOs in V2 version
					COM1	LCD driver COM port
113	91		57	PBDSG3	P120	GPIOs, new IOs in V2 version
					COM0	LCD driver COM port
114		51		PBDSG3	P100	GPIO
					SEG36	LCD driver SEG port
115	92	53	58	PBULD3	P10	GPIO
					KEY0	keystroke input
					TC0_N[0]	Timer 0 Channel 0 Compare Inverted Outputs
					TCIN	Timer Input
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
					CF_OUT2	Metering pulse output (not available on RN8213 and RN8211B)
					D2F_OUT2	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					IOCNT_OUT2	Pulse Forwarding Output
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
116	93	54	59	PBULD3	P11	GPIO
					KEY1	keystroke input
					TC0_P[0]	Timer 0 Channel 0 Compare Positive Outputs
					TCIN	Timer Input
					IA_IN	IA channel external 1bit input
					CF_OUT3	Metering pulse output
					D2F_OUT3	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					IOCNT_OUT3	Pulse forwarding output (RN8213 and RN8211B do not have this feature)
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
117		55		PBULD3	P12	GPIO
					KEY2	keystroke input
					TC0_N[1]	Timer 0 Channel 1 Compare Inverted

						Outputs
					TCIN	Timer Input
					IB_IN	IB channel external 1bit input
					CF_OUT4	Metering pulse output
					D2F_OUT4	Pulse output of D2F
					IOCNT_OUT4	Pulse Forwarding Output
					TRIG_OUT	Intelligent micro-breakout output signal
118	94	56	60	PBUS6	P30	GPIO, is also the ISPEN detection pin, the chip will detect the state of this port after a reset occurs, if the input is low, the system will enter the ISP mode and will not guide the customer program. Hardware and software design should take care to avoid this pin being in a low level state during the reset process.
					INT0	External Interrupt Input
					TX4	UART4 Transmit
					TCIN	Timer Input
					RTCOUT	Second pulse output
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					RTC1S	Perpetual calendar 1HZ second pulse output
119		57		PBUS6	P31	GPIO
					INT1	External Interrupt Input
					RX4	UART4 receive
					TCIN	Timer Input
					RTCOUT	Second pulse output
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					CF_OUT3	Metering pulse output
					D2F_OUT3	Pulse output of D2F
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
					RTC1S	Perpetual calendar 1HZ second pulse output

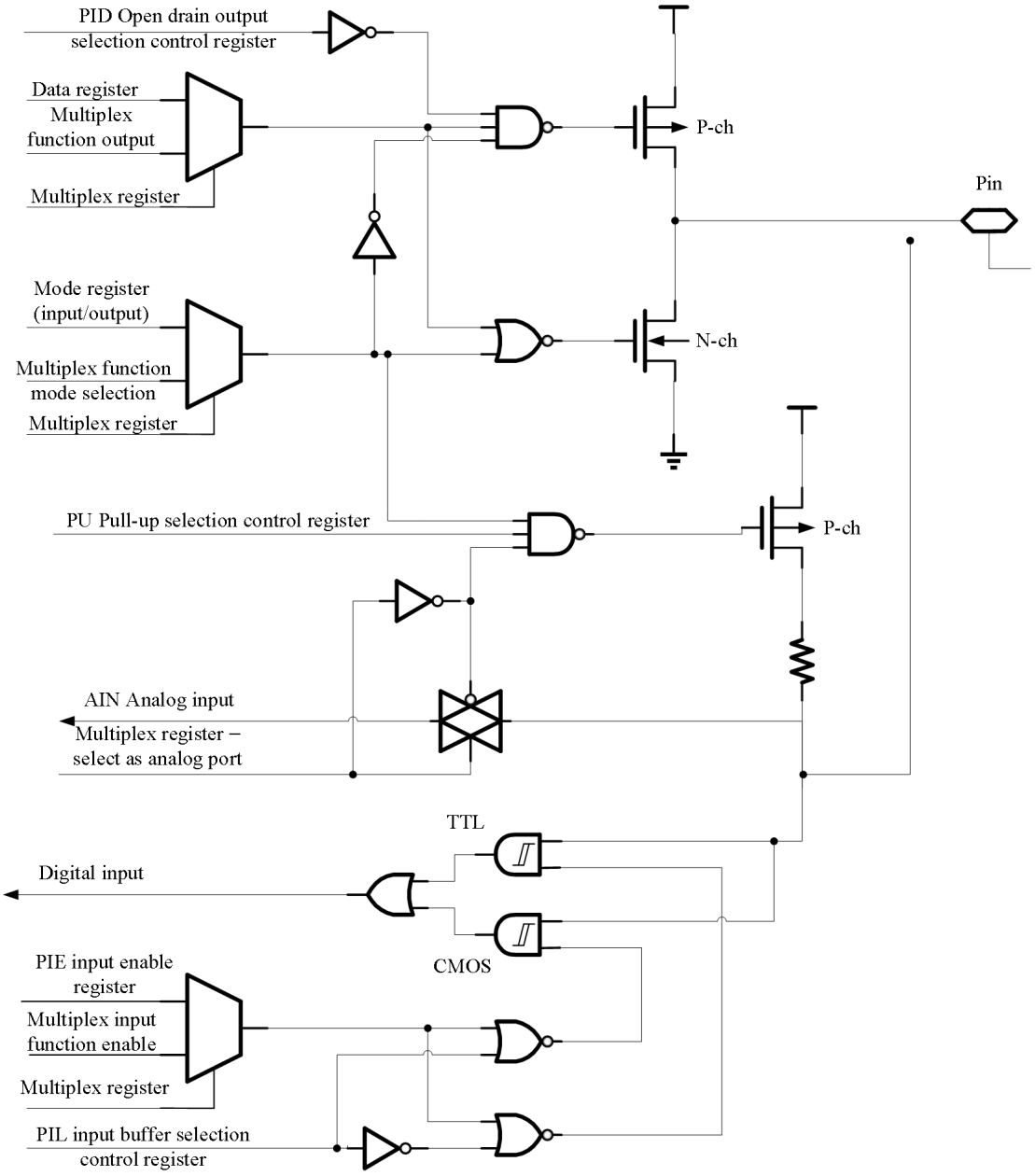
120	95	58	61	PBUS6	P32	GPIO
					INT2	External Interrupt Input
					RTCOUT	RTCOUT output
					KEY5	keystroke input
					ADC_CLKO	ADC Clock Output
					TRIG_OUT	Intelligent micro-breakout output signal
					CF_OUT4	Metering pulse output
					D2F_OUT4	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
					RTC1S	Perpetual calendar 1HZ second pulse output
121	96			PBULD3	P26	GPIO
					RX3	UART3 receive
					RX2	UART2 receive
					TRIG_OUT	Intelligent micro-breakout output signal
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
122	97			PBULD3	P27	GPIO
					TX3	UART3 Transmit
					TX2	UART2 Transmit
					TRIG_OUT	Intelligent micro-breakout output signal
					TC1_N[1]	Timer 1 Channel 1 Compare Inverted Outputs
123	98			PBULD6	P57	GPIO, 6mA drive capability in V2, 3mA in V1
					TC1_P[1]	Timer 1 Channel 1 Compare Positive Outputs
					TCIN	Timer Input
					SF	apparent pulse output
					CF_OUT2	Metering pulse output
					D2F_OUT2	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					IOCNT_OUT2	Pulse forwarding output (not available on RN8213 and RN8211B)
					ADC_CLKO	ADC Clock Output
124	99	59		PBUS6	P51	GPIO

					QF	Reactive pulse output
					RTCOUT	RTCOUT output
					PF	Active pulse output
					SF	apparent pulse output
					CF_OUT1	Metering pulse output
					D2F_OUT1	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					IOCNT_OUT1	Pulse forwarding output (RN8213 and RN8211B do not have this feature)
					RTC1S	Perpetual calendar 1HZ second pulse output
125	100	60	62	PBUS6	P50	GPIO
					PF	Active pulse output
					RTCOUT	RTCOUT output
					SF	apparent pulse output
					QF	Reactive pulse output
					CF_OUT0	Metering pulse output
					D2F_OUT0	Pulse output for D2F (RN8213 and RN8211B do not have this function)
					IOCNT_OUT0	Pulse forwarding output (not available on RN8213 and RN8211B)
					RTC1S	Perpetual calendar 1HZ second pulse output
126		61		PBUS6	P34	GPIO
					INT4	External Interrupt Input
					SF	apparent pulse output
					CF_OUT3	Metering pulse output
					D2F_OUT3	Pulse output of D2F
					IOCNT_OUT3	Pulse Forwarding Output
					ADC_CLKO	ADC Clock Output
					IA_IN	IA channel external 1bit input
					TRIG_OUT	Intelligent micro-breakout output signal
127	NC	NC	NC	PBUS6	P35	GPIO
					INT5	External Interrupt Input
					TCIN	Timer Input
					CF_OUT4	Metering pulse output
					D2F_OUT4	Pulse output of D2F
					IOCNT_OUT4	Pulse Forwarding Output
					ADC_CLK	ADC Clock Output

					O	
					IA_IN	IA channel external 1bit input
					IB_IN	IB channel external 1bit input
					TRIG_OUT	Intelligent micro-breakout output signal
127	NC	NC	NC	PBULD3	P117	GPIOs, new IOs in V2 version
					RTC1S	Perpetual calendar 1HZ second pulse output

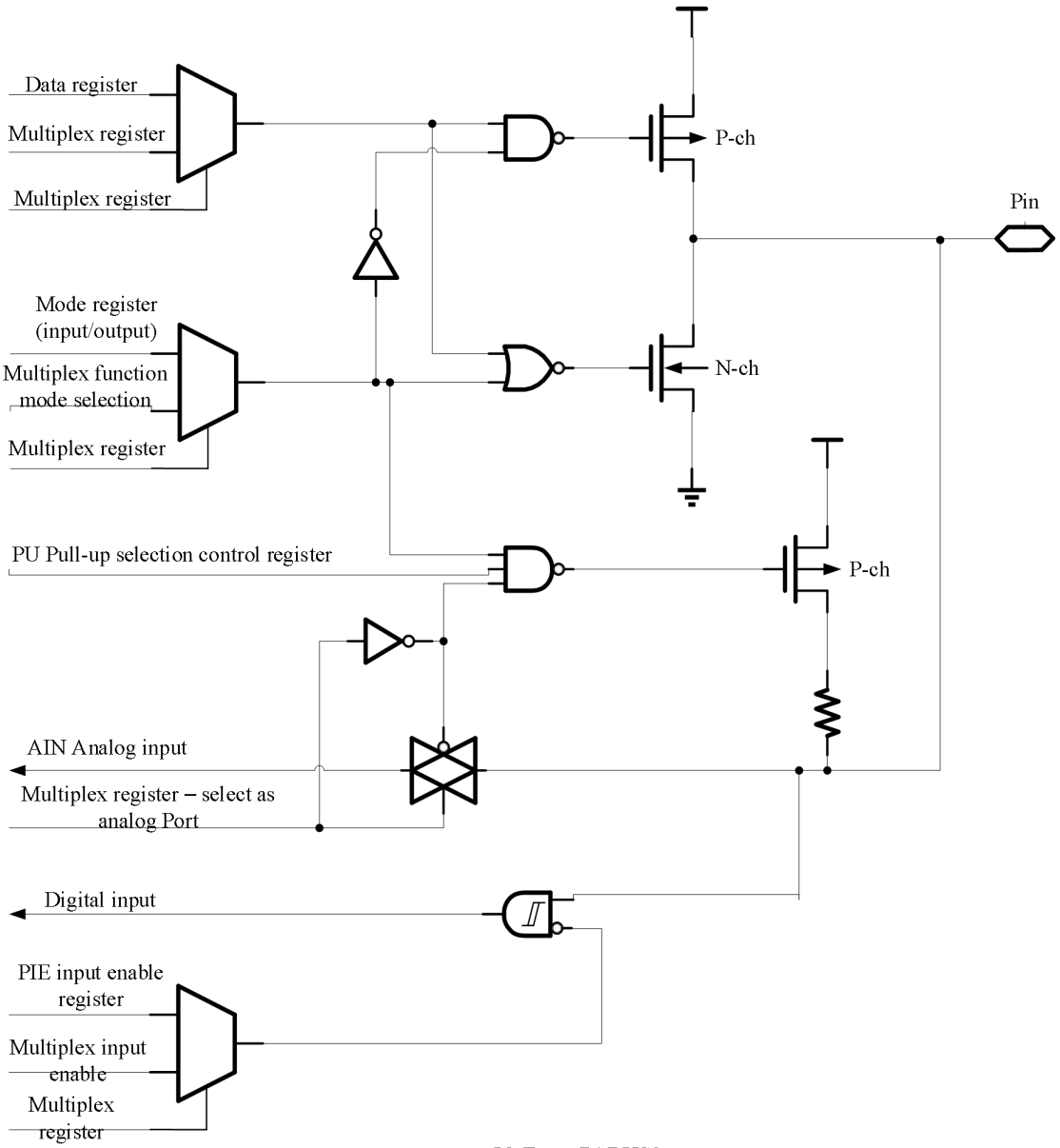
1.7 IO Port Function Block Diagram

1.7.1 PABULD3



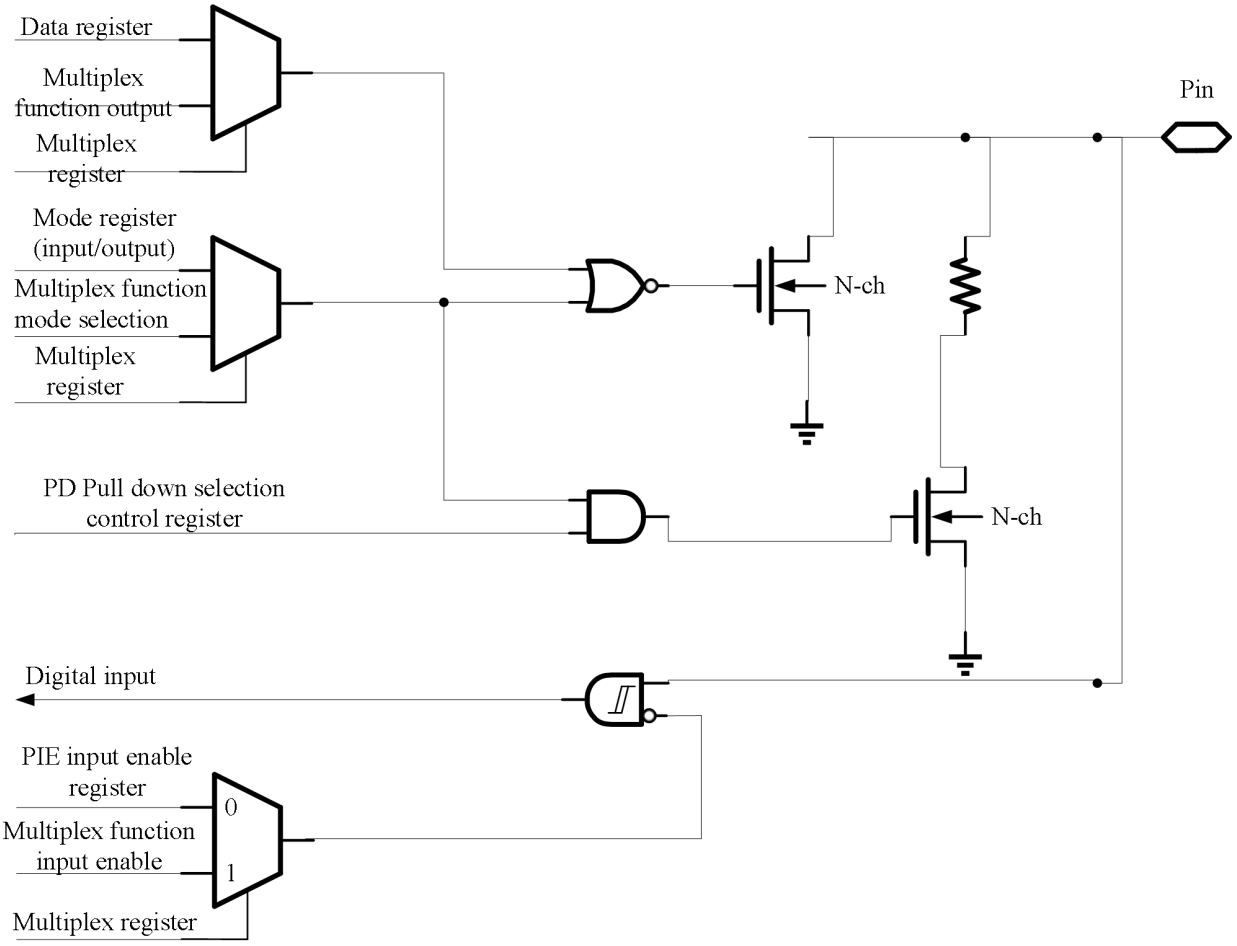
IO Type -PABULD3

1.7.2 PABUS3



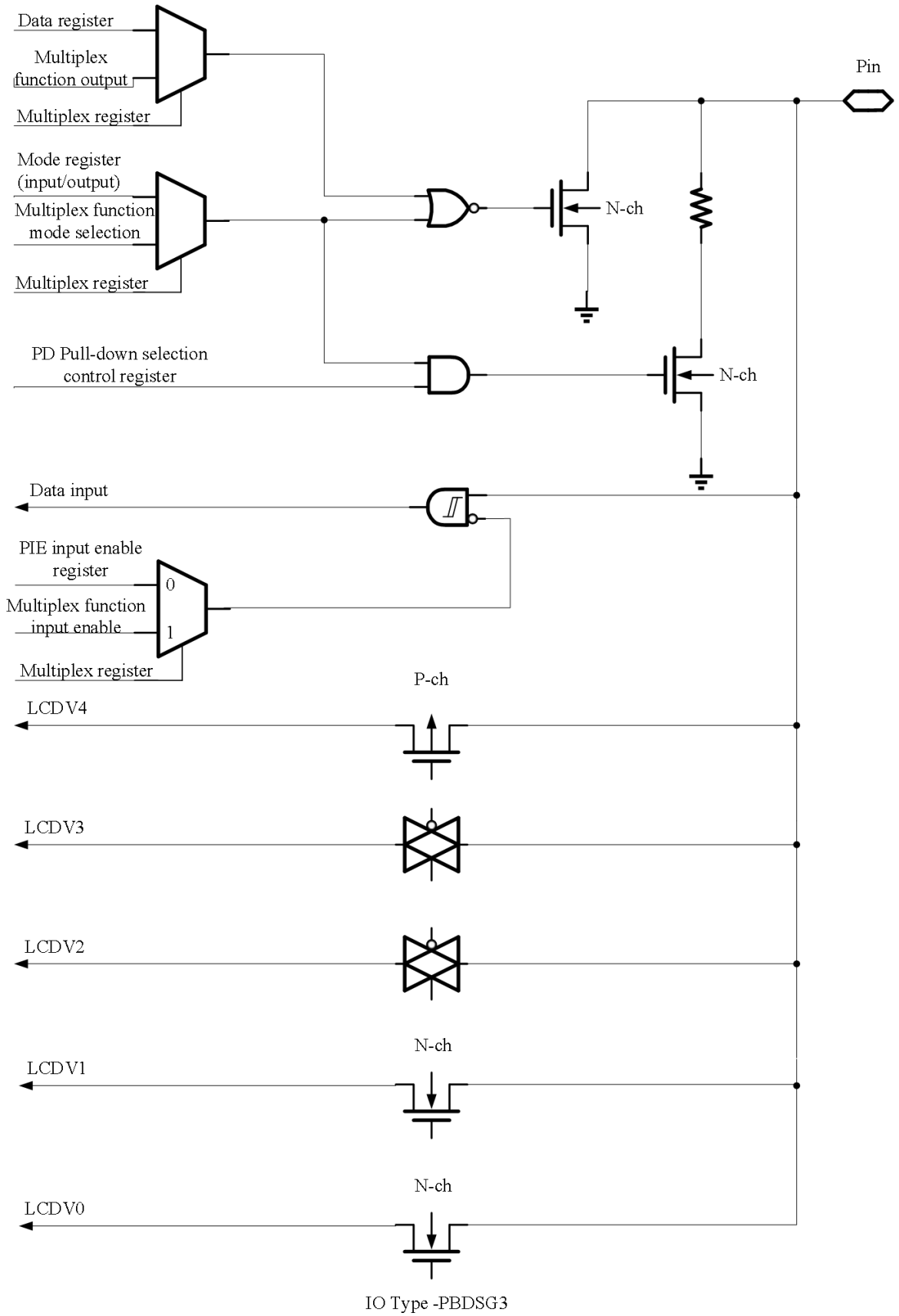
IO Type -PABUS3

1.7.3 PBDS3



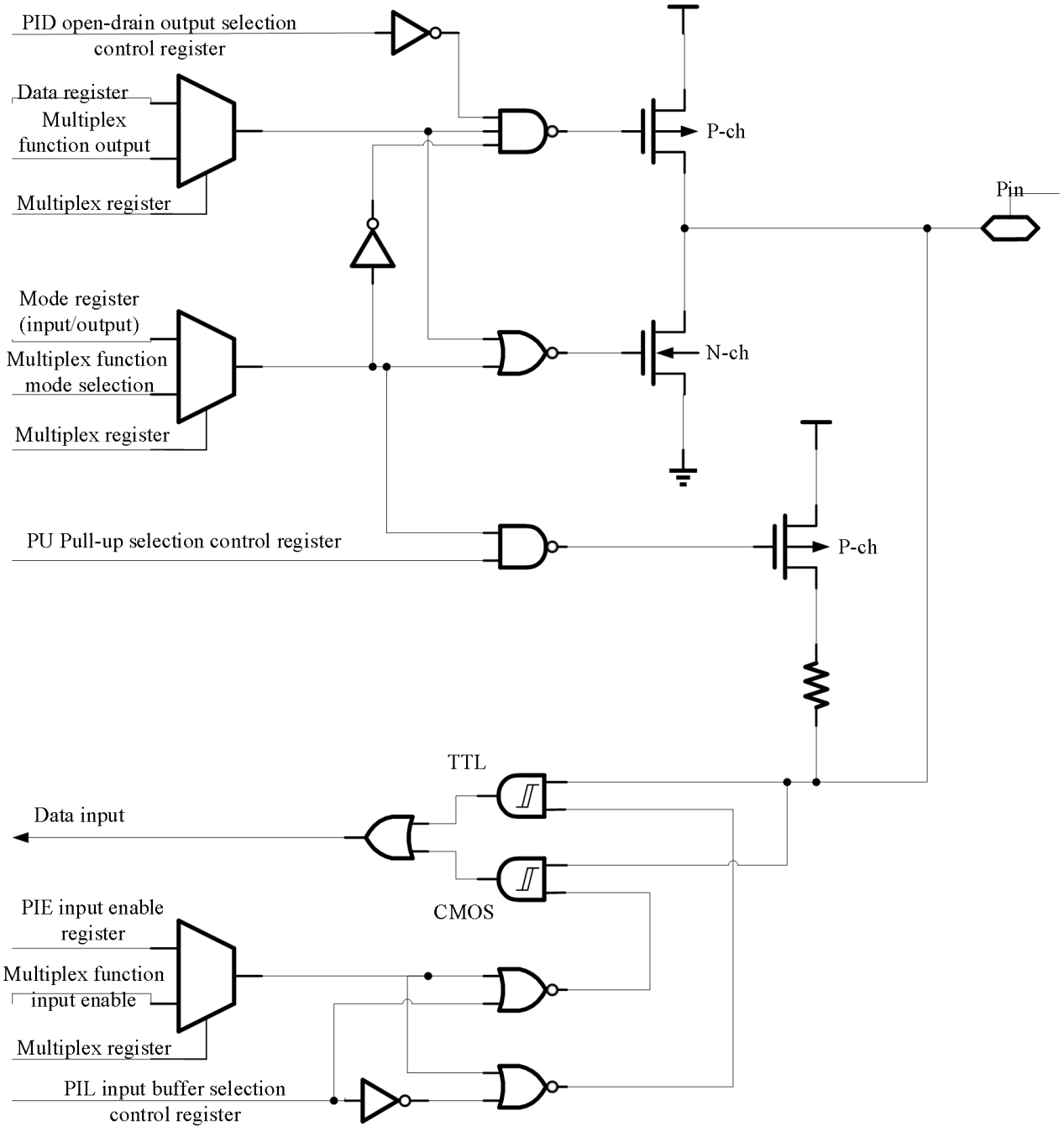
IO Type -PBDS3

1.7.4 PBDSG3



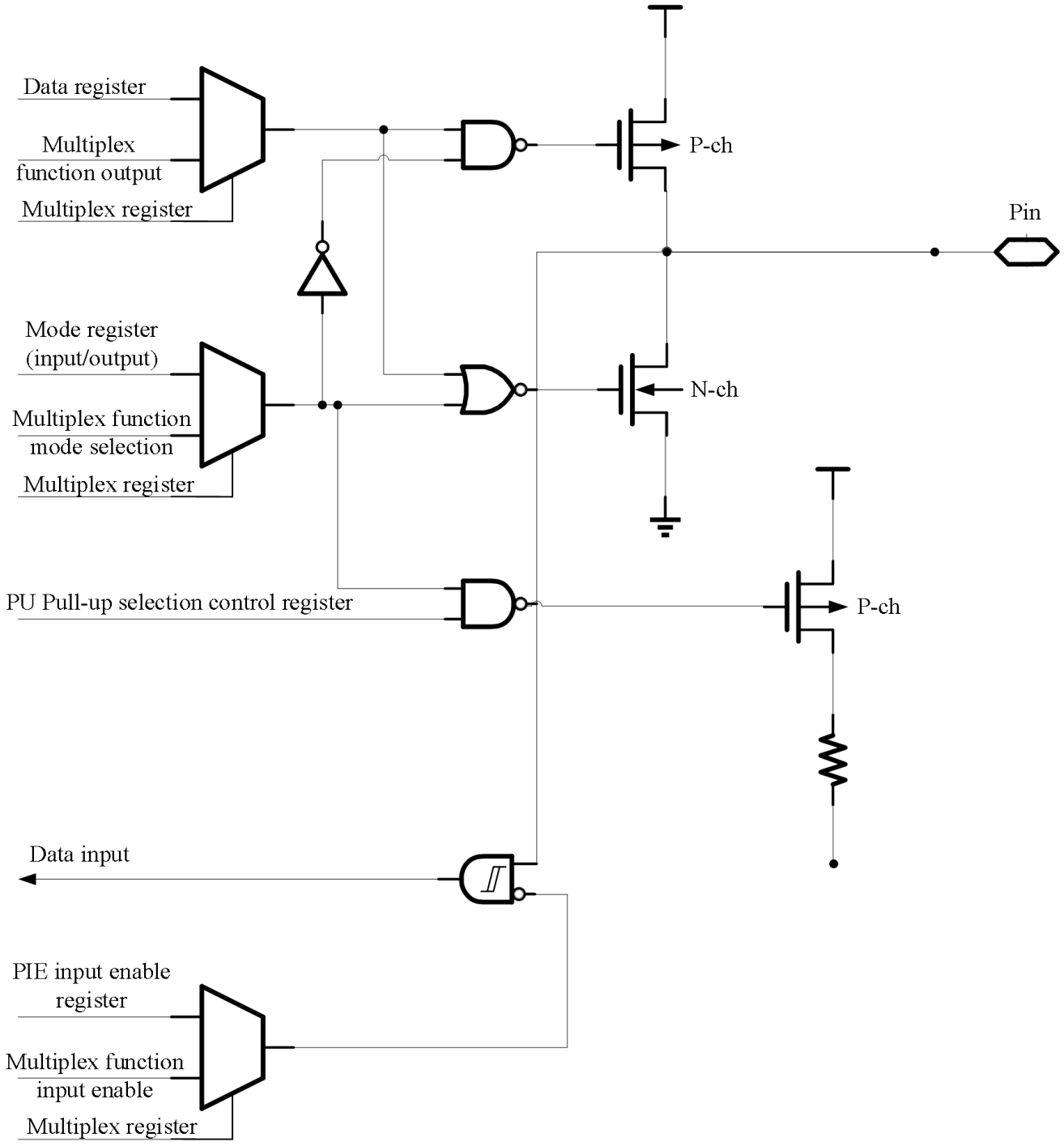
IO Type -PBDSG3

1.7.5 PBULD3/6



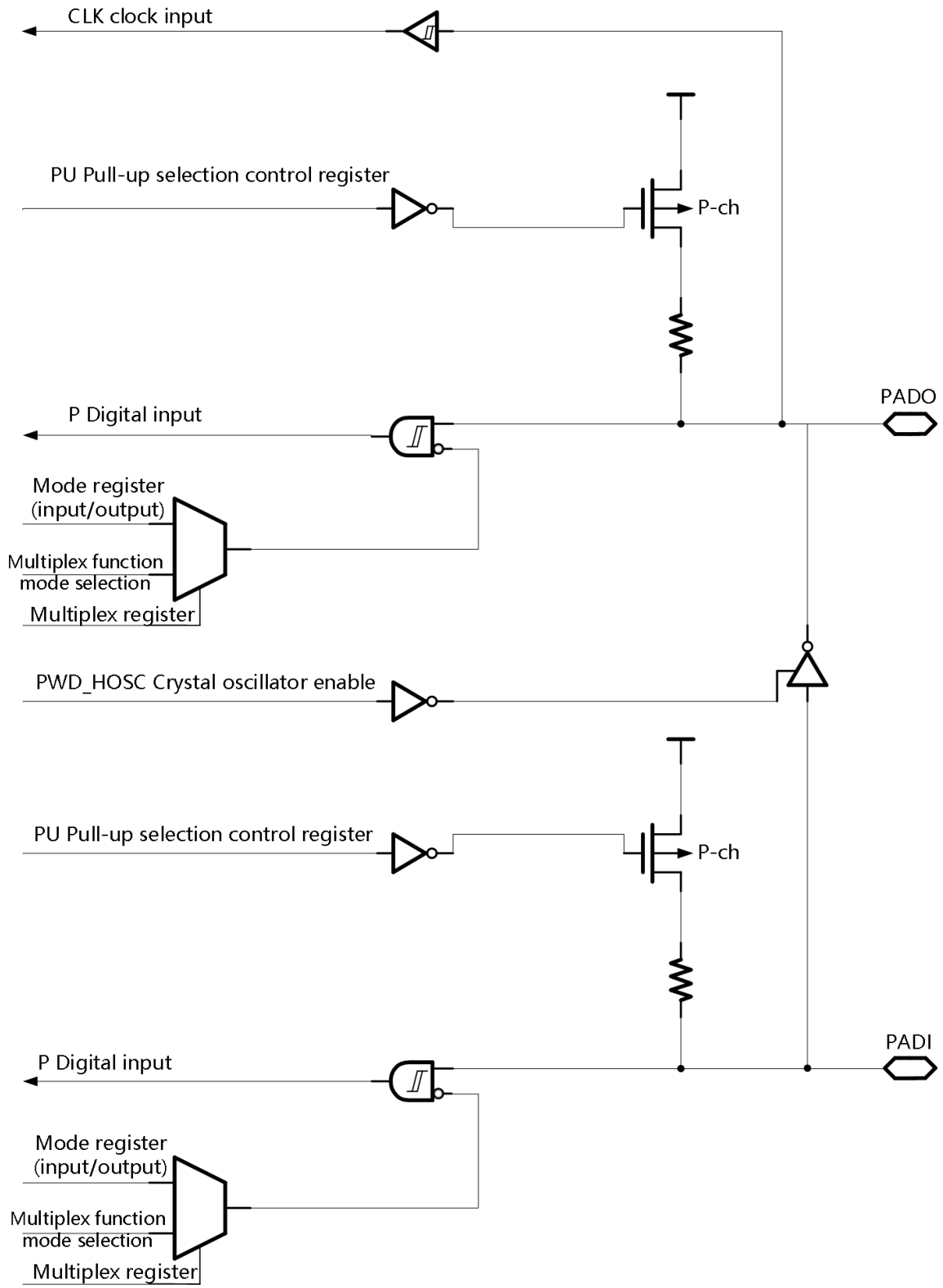
IO Type -PBULD3/PBULD6

1.7.6 PBUS6



IO Type -PBUS6

1.7.7 PIUX



IO Type -PIUX

2 Electrical Characteristics

2.1 Performance Parameters

Measurement parameters (VCC=3V~5.5V, room temperature)						
Items	**Notation**	**inimal**	**typical**	**maximum**	**unit**	**Test conditions and notes**
Active energy measurement error	Err			±0.1%		Normal temperature 8000:1 dynamic range; -40 ℃ ～ +85 ℃ temperature coefficient 5ppm typical, maximum 15ppm;
Active energy measurement bandwidth	BW		7		kHz	
Reactive energy measurement error	Err			±0.1%		
Apparent power measurement error	Err			±0.1%		
RMS measurement error	Err			± 0.2%		Dynamic range of 1000:1 at room temperature; Temperature coefficient of 5ppm typical, 15ppm max. in -40℃～+85℃.
Power Measurement Error	Err			±0.1%		
Electrical Pulse Output	Maximum frequency			20KHz	Hz	
	duty cycle		50%		%	When the pulse width is less than 84ms, equal duty
	High Level Pulse Width		84ms		ms	
Sigma-Delta ADC Performance						
Maximum Signal Level	V_{xn}			±1000	mV	differential post-signal
ADC Offset error	DC_{off}		1		mV	
-3dB bandwidth	B_{-3dB}		7		kHz	
Reference voltage (VCC=3V~5.5V, temperature range: -40℃~+85℃)						
Output Voltage REFV	V_{ref}	1.24	1.25	1.26	V	
temperature coefficient	T_c		5	15	ppm/° C	
Analog peripheral (Temperature range: -40° C to +85° C)						
Low Power Comparator CMP1/CMP2/	Vil1	1.23	1.28	1.33	V	In the default configuration, this threshold is the comparator output low

LVDIN Threshold 1						level comparison result threshold;
	Vih1	1.43	1.48	1.53	V	In the default configuration, this threshold is the comparator output high level comparison result threshold;
	hysteresis		200		mV	Vih-Vil
Low Power Comparator CMP1/CMP2 Threshold 2	Vil2	0.8	0.84	0.88	V	When the 0.9V gear is selected and the selection has hysteresis, this threshold is the comparator output low level comparison result threshold;
	Vih2	0.94	0.98	0.102	V	When the 0.9V gear is selected and the selection has hysteresis, this threshold is the comparator output high level comparison result threshold;
	hysteresis		140		mV	Vih-Vil
SAR ADC Input Range	SAR-IN	0		REFV	V	REFV is an internal low-power reference with a typical value of 1.25V
Switching to main power threshold	Power-up switching threshold	TBD	2.8	TBD	V	The power supply switches to VCC when the mains (VCC) is above this threshold or above VBAT. It is recommended that when the main power selection is 3.3V, it is necessary to ensure that the power supply voltage range is 3.3V ±5%.
Switch to battery threshold	Power-down switching threshold	TBD	2.7	TBD	V	The supply switches to VBAT when the mains (VCC) is below this threshold and below VBAT.
LCD output voltage	LCDVD	4.85	5.05	5.25	V	Full temperature range testing

VBAT measurements	VBATD	0	3.6	3.8	V	SAR ADC measurement range for VBAT;
Clock parameters (Temperature range: -40℃～+85℃)						
Input Low Frequency Clock Frequency Range	XI		32.768		KHz	
Input high-frequency clock frequency range	HOSI	7.3728	14.7456	29.4912	Mhz	
Internal PLL clock frequency range	PLL		14.7456	29.4912	MHz	
Internal high frequency RCH	RCH		29.5		MHz	Default clock for chip reset, frequency 1.8M after frequency division, RCH error < ± 1% over full temperature range
Internal low frequency RCL	RCL	20	32	40	KHz	For WDT clocks
power supply						
main power	VCC	2.8	5/3.3	5.5	V	
Minimum cpu operating voltage	Vil	1.8	1.9	2	V	ordinary temperatures
	Vil	TBD	TBD	TBD	V	Low temperature -40 degrees
	Vil	TBD	TBD	TBD	V	High temperature 85 degrees
batteries	VBAT		3.6		V	
analog current	AIdd		TBD		mA	All three ADCs are on.
digital current	DIdd		TBD		mA	CPU running at 3.6864MHz, metering turned on
Sleep mode power consumption	SIdd		7		μA	RTC auto warm-up; RAM hold; CPU and digital peripherals do not power down; WDT on; Power monitoring on; Wake on Interrupt
LDO3	V33	2.9	3.0	3.1	V	
LDO15	V1P5	1.35	1.5	1.65	V	
Limit parameters						
Mains voltage	Vvcc	-0.3	--	+7	V	
Battery Input Voltage	Vvbat	-0.3	--	+7	V	
DV_{DD} to DGND		-0.3	--	+7	V	

DV_{DD} to AV_{DD}		-0.3		+0.3	V	
iap, ian, ibp, ibn, up, un		-6		+6	V	
Digital IO output high	VOH		--	DV_{DD} +0.3	V	
Digital IO output low	VOL	-0.3	--		V	
Digital IO input high	VIH		0.7VCC			CMOS
Digital IO input low	VIL		0.3VCC			CMOS
Digital IO input high	VIH		0.4VCC			TTL
Digital IO input low	VIL		0.2VCC			TTL
Isource for Digital IO	Isource	5		10	mA	6mA type
Isink for Digital IO	Isink	7		15	mA	6mA type
Isource for Digital IO	Isource	3		5	mA	3mA type
Isink for Digital IO	Isink	5		10	mA	3mA type
Analog input voltage relative to AGND	V_{INA}	-0.3	--	AV_{DD} +0.3	V	
Operating Temperature Range	T_A	-40	--	85	℃	
Storage temperature range	T_{stg}	-65	--	150	℃	
temperature of a bond	T_J		125		℃	
Lead-free soldering temperature	T_{SDR}	--	260		℃	

2.2 Reliability parameters

Items	Notation	Condition	Value	unit
electrostatic discharge	HBM	Complies with JEDEC EIA/JESD22-A114 standards	4000	V
	MM	Complies with JEDEC EIA/JESD22-A115 standard	200	V
	CDM	Complies with JEDEC EIA/JESD22-C101F: 2013 standard	500	V
Latch test	Latchup	Conforms to JESD78F standard	200	mA
moisture sensitivity	MSD	Conforms to IPC/JEDEC J-STD-020D.1 standard	Level 3	/

3 System Control

3.1 Power Management Solutions

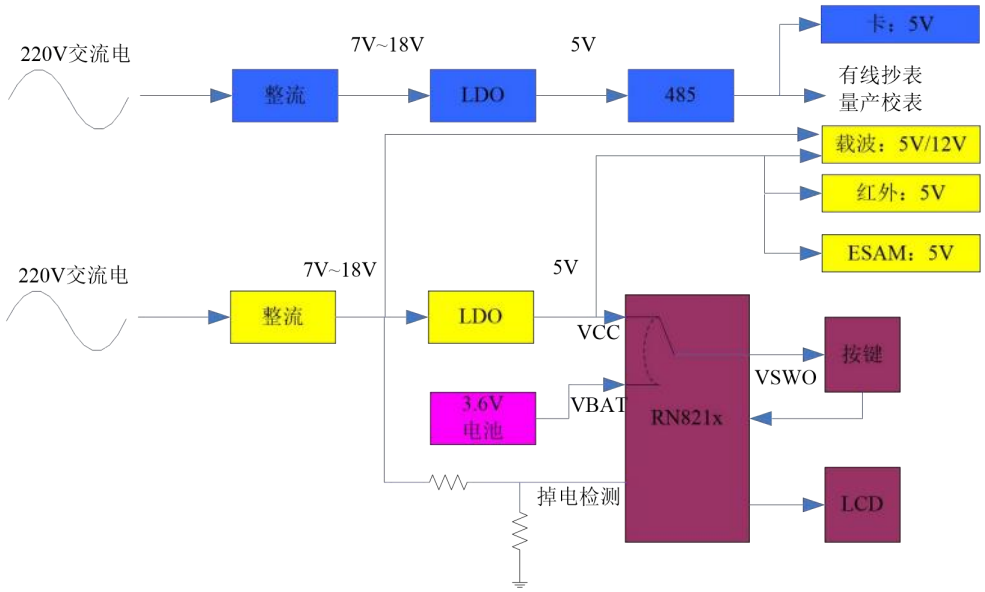


Figure 3.1 Single-phase meter power management scheme: internal battery switching

3.2 Clock source

- 2 external clock sources

LOSC: 32.768 KHz low frequency crystal oscillator

1) For RTC clock and CPU clock under low frequency operation;

(2) Support 32.768 KHz clock external irrigation, need to configure external irrigation clock enable, external irrigation does not increase the additional power consumption;

(3) 32.768 KHz crystal does not require external capacitors and resistors, it is recommended that the external load capacitance typical value of 12.5pF crystal.

HOSC: External High Frequency Crystal

1） Supports 7.3728Mhz, 14.7456Mhz, 29.4912Mhz for CPU main system clock;

2） Supports external high-frequency clock injection, no configuration required, directly from the HOSCI pin injection, no additional power consumption;

3） Need external load capacitance and resistance, recommended load capacitance 15pF, resistance 10M, it is recommended to choose the load capacitance 15pF crystal, 7.3728Mhz crystal ESR less than 80 Ω , 14.7456Mhz, 29.4912Mhz crystal ESR less than 40 Ω .

- 3 internal clock sources

RCH: internal high-frequency RC clock (typical value is 29.5MHz), after CPU reset, the chip default running clock is the 16th division of RCH, i.e., the reset default main frequency is 1.8M; supports 1/2/4/8/16 divisions to switch arbitrarily, and the change of the whole temperature range is <±1%.

RCL: Internal low-frequency RC clock for WDT clock, also used for CPU clock and LCD clock under battery power.

PLL: Internal PLL high-frequency clock, multiplied from 32.768 KHz to 7.3728MHz, 14.7456MHz,

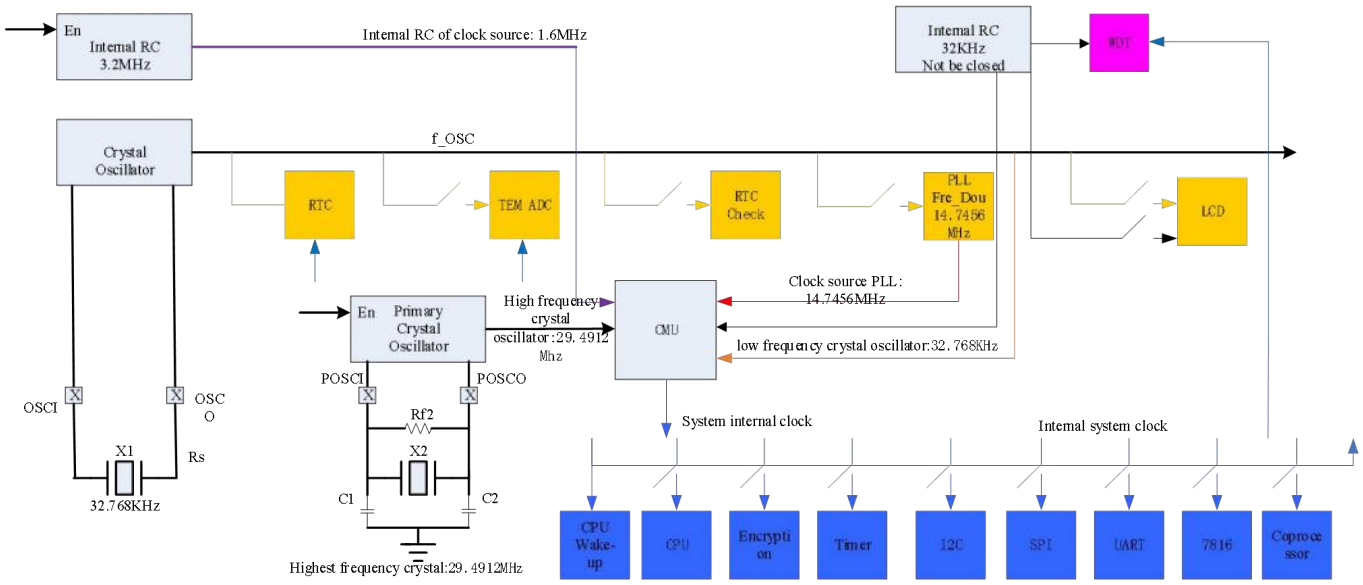
29.4912MHz.

All five of the above clock sources can be used for the CPU main system clock.

The system clock source can be selected as PLL or high-frequency crystal in the run mode.

The CPU switches from a low-frequency clock to a high-frequency clock by instruction. The system master clock can be switched between RC, PLL (or HOSC), and LOSC clocks. To ensure clock accuracy, PLL or external high-frequency clock should be selected as the system master clock in normal operation mode.

The user must call the Sharp Energy micro library function to perform clock switching. Users should not perform write operations to the OSC_CTL1 (0x0), SYS_MODE (0x4) registers in the application program. If a write operation is performed on OSC_CTL2 (0x10), it should be ensured that only the bit that needs to be operated is changed and not the value of the other register bits.



3.3 Clock switching

The following switches are included:

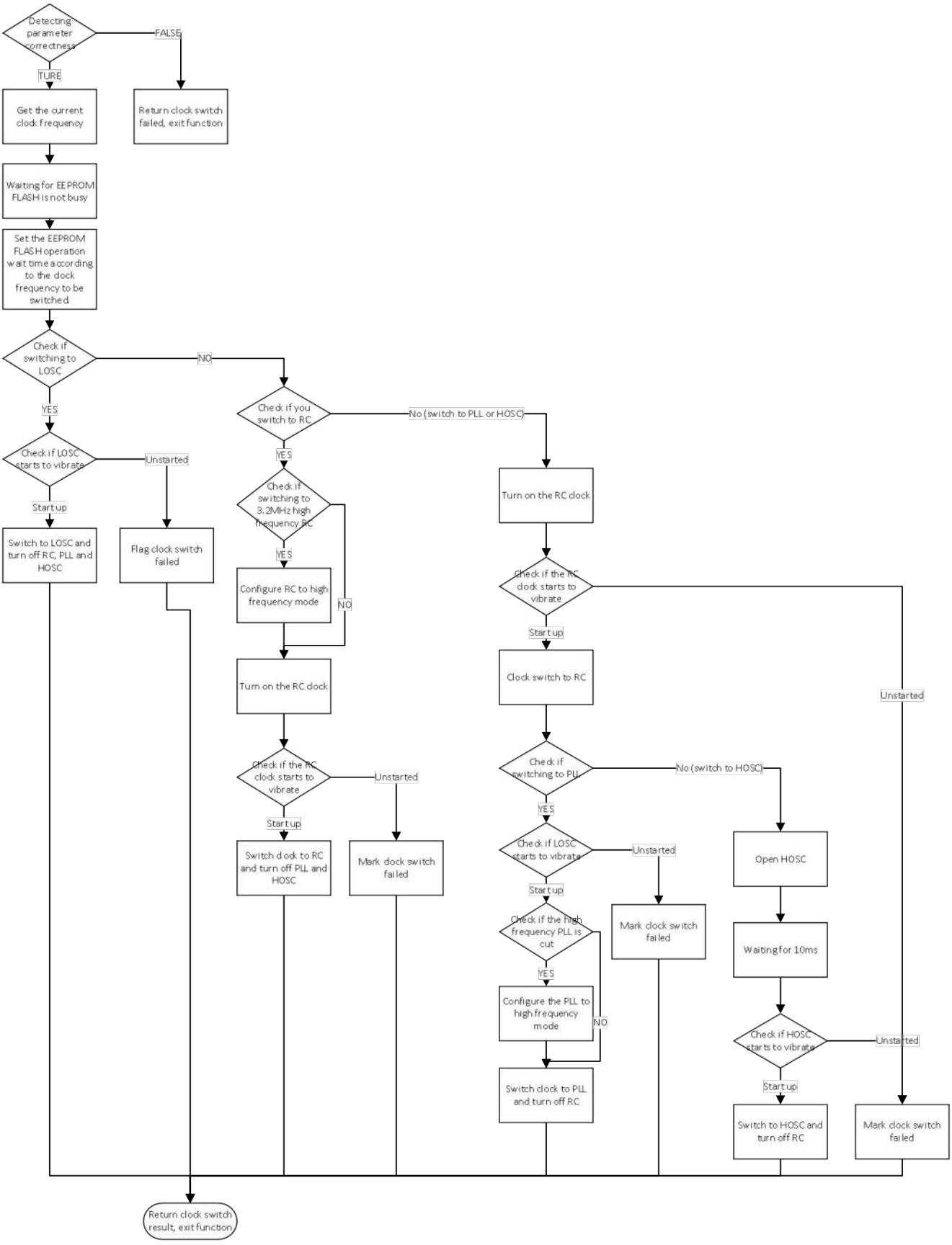
1. Defaults to RCH after reset;
2. PLL/HOSC and RCH switching by CPU instruction;
3. PLL/HOSC and LOSC/RCL switching is done by CPU instructions;
4. LOSC/RCL and RCH switching, done by CPU instruction.

Clock switching should be done by calling the library function provided by Reynolds Micro.

If an external high-frequency crystal HOSC is selected as the system master clock, the OSC_CTL2 register needs to be configured before calling the library function.

If PLL is selected as the system master clock, and it is the first time to power on, you need to wait for the 32KHz crystal to vibrate (the vibration time is about 0.5s) and then call the library function to switch the clock.

Library function clock switching flow chart



3.4 Low Power Mode for SOC

The low power modes of M0 are Sleep and DeepSleep. The difference between these two instructions is:

1. After the CPU runs the Sleep instruction, it will only turn off the CPU core clock; the peripheral clocks require registers to turn off (see MODE0 and MODE1);
2. After the CPU runs the DeepSleep instruction, not only does it turn off the CPU core clock, but it also automatically turns off most of the peripheral clocks (see MODE0 and MODE1);

It is recommended that the software does not distinguish between Sleep and DeepSleep, and uses Sleep directly, and all other peripheral clocks are turned off using the program.

In addition to the low-power mode of M0, the SOC provides a flexible mechanism to realize the user's needs for different power consumption modes:

1. The CPU can switch arbitrarily between the high-frequency clock mode HCM, the low-frequency clock mode LCM, and the system default mode RCH by calling a library function;
2. The clocks of the CPU and peripherals can be turned off;
3. In the lowest power mode (CPU sleep, SRAM and digital peripherals not powered down, RTC running) power consumption is about 7uA or so;

Users can flexibly realize the low-power mode they need according to the mechanism provided by the SOC as above. The default state of the main module after powering up:

Main Modules	Default Operating State
1.5V voltage threshold	
M0 kernel	Turns on, can turn off clock, never loses power
interruption system	Turns on, can turn off clock, never loses power
SRAM	Turns on, can turn off clock, never loses power
ROM	Turns on, can turn off clock, never loses power
flash	On, CPU can be automatically turned off after hibernation
RTC	On, perpetual calendar not off, no reset.
EMM (normal metering)	Off, can turn off clock, never lose power
Other peripherals	Off, can turn off clock, never lose power
5V Voltage Threshold	
Measurement ADC	Close to turn off the power
Measurementref	Off, power can be turned off

3V LDO	Off, power can be turned off
1.5V LDO	On, not off
RC	On, can be powered off
Comparator CMP2	On, can be powered off
Comparator CMP1	Off, power can be turned off
LCD	Off, power can be turned off
Temperature ADC	Timed on
LVD	Off, power can be turned off
comparator	Off, power can be turned off
Power Reset System	Always on.
PLL	Off, power can be turned off
HOSC	Off, power can be turned off
LOSC	Always on.

Modules that are off by default can be selected to be on or off at all three clocks.

3.5 Reset

3.5.1 External PIN reset

The external pin RSTN has a built-in pull-up resistor of approximately 50K ohms and the input level is CMOS level. The internal filtering time is 1ms, and a reset occurs when the external input goes low for more than 1ms.

3.5.2 Upper and lower power reset

Three power-on reset (POR) circuits and two power-off reset (BOR) circuits are built-in to monitor VSWO, LDO15 (1.5V LDO) respectively.

The circuit is always in operation and cannot be turned off, ensuring that the system can operate normally when the threshold is exceeded (about 2.6V); when it is below the threshold (2.2V/1.8V gear can be assigned), the device is in reset state. There is no need to use an external reset circuit.

This product also has a built-in programmable voltage monitor, LVD, which monitors VCC and compares it to a set threshold, generating an interrupt when VCC is below or above the threshold.

3.5.3 Software reset

The Cotex M0 has a built-in SCB_AIRCR register, which can be used to reset the entire chip system by simply resetting the SYSRESETREQ bit of the register, and the reset effect is equivalent to an external PIN reset. For details, please refer to the M0 documentation.

3.5.4 Watchdog reset

If the dog cannot be fed within the specified time, or if an illegal command is used to feed the dog, the chip's built-in hardware watchdog will reset the entire chip, with a reset effect equivalent to an external PIN reset.

3.5.5 CM0 reset

V2 version added CM0 reset, support MCU individual reset, online upgrade does not need to reset the whole chip, can ensure that online upgrade does not affect the metering.

3.6 Brown-out handling

The SOC chip provides the following means to do power-down detection, the application software should finish the necessary work in time after detecting the power-down, turn off the peripherals, and let the cpu enter the low-frequency operation mode or hibernation mode.

1. CMP1/CMP2 for analog peripheral modules

CMP1/CMP2 is a low-power comparator that detects the voltage input to the IO port, detects the power supply voltage at the front of the LDO that powers the chip, and is also the only basis for the power-up judgment; this module consumes less than 1uA, and can be turned on all the time in practical applications, and the customer's software can use the CMP1/CMP2 to interrupt or query the flag bit to make the power-up and power-down judgments.

2. LVD of analog peripheral modules

LVD module can detect the input voltage of external pin LVDIN (external pin is required, power consumption is larger than CMP1/CMP2), and it can also detect the power supply voltage of the chip (no external pin input is required, the detection of VCC power supply is completed inside the chip, and the threshold value can be set in multiple files), and the customer's software can use the interrupt or flag query to do the judgment of the upper and lower power supply.

Customers can choose CMP1/CMP2 or LVD to complete the power-down detection function and optimize the system power management according to the actual hardware circuit design.

3.7 Register Description

Base address of the system control module:

module name	**physical address**	**mapping address**
SYSC	0x40034000	0x40034000
register name	**address offset**	**Description**
OSC_CTRL1	0x0	System OSC control register 1
SYS_MODE	0x4	System Mode Switching Register
SYS_PD	0x8	System power-down control register
ADC_CTRL	0xC	ADC Control Register
OSC_CTRL2	0x10	System OSC control register 2
SYS_RST	0x14	System Reset Register
MAP_CTRL	0x18	Address Mapping Control Register
MOD0_EN	0x1C	Module Enable 0 Register
MOD1_EN	0x20	Module Enable 1 Register
INTC_EN	0x24	INTC Enable Register
KBI_EN	0x28	KBI Enable Register
CHIP_ID	0x2C	Chip version number
SYS_PS	0x30	System control register password protection bit
IRFR_CTRL	0x34	Infrared clock division factor in RCH mode
SYS_CFG (new)	0x38	System Configuration Register
TRIM_CFG1	0x78	Clock Calibration Configuration Register
TRIM_START	0x7C	Clock calibration startup register
DMA_PRI1 (new)	0x80	DMA Priority Configuration Register 1

FAB_UID0 (new)	0xF0	Chip Unique Code Register 0
FAB_UID1 (new)	0xF4	Chip Unique Code Register 1
DMA_PRI2 (new)	0xFC	DMA Priority Configuration Register 2
ADCIN_CTRL (added)	0x114	ADC external irrigation control register
SYSCP_CON (new)	0x118	System Chopper Configuration Register

3.7.1 System OSC control register 1 OSC_CTRL1 (0x0)

Bit	Name	Description	Read/Write	Reset Value
31:17	---	Read only, not write.	R	0
16:11	CLOCK_FLAG	System Clock On Flag Bit: This bit is 1 if the clock is on: { RCM, HOSC, RCL, RCH, PLL, LOSC}	R	001101
10:8	SYSCLK_STAT	System master clock frequency indication: 000: The current system master clock is 7.3728MHz; 001: The current system master clock is 3.6864MHz; 010: The current system master clock is 1.8432MHz; 011: The current system master clock is 32.768KHz; 100: The current system master clock is 14.7456Mhz; 101: The current system master clock is 29.4912Mhz; Other: not meaningful	R	010
7	PLL_LOCK	PLL Lock Status 0: not locked 1: Locked	R	0
6	PLL_HOSC_ON	This bit is 1 when the system is running on an external HF or internal PLL clock; This bit is 0 when the system is running on other clocks.	R	0
5	IRCH_ON	This bit is 1 when the system is running on the internal high-frequency clock; This bit is 0 when the system is running on other clocks.	R	1
4	LOSC_ON	This bit is 1 when the system is running on an external low frequency clock; This bit is 0 when the system is running on other clocks.	R	0
3:2	PLL_HOSC_DIV	System master clock division frequency selection: (valid only for high frequency clock mode) 00: PLL, HOSC as CPU master clock; 01: PLL, HOSC bisection as CPU master clock; 10: PLL, HOSC's Quad as CPU master clock; 11: The octave of HOSC (when the clock frequency is selected as 14MHz and 29MHz) is used as the CPU master clock; Note: Can only be changed in RC or LC mode. Note: The above registers only determine the crossover coefficient, the specific system master frequency needs to be determined according to the crossover coefficient	R/W	01

		and the current clock source selection.		
1	IRCH_PD	Internal RC enable bit: 0: Open; 1: Close.	R/W	0
0	PLL_PD	PLL module enable bit 0: Open 1: Closure	RW	1

It is recommended that the user call the Sharp Energy micro library function for clock switching. It is not recommended that users write to the OSC_CTL1 (0x0) register in the application program.

3.7.2 System mode setting register SYS_MODE (0x4)

Bit	Name	Description	Read/Write	Reset Value
31:6	---	read-only, not writeable	R	0
5	FLASH_BUSY	Flash busy state, cannot enter mode switching: 0: idle 1: BUSY	R	0
4	---	reserved bit	R	0
3:0	MODE	Write D to set up entry into HF mode HCM, bit2 reads 1; Write E, set to enter RC mode RCM, bit1 read as 1; Write F, set to enter 32.768KHz mode LCM, bit0 read as 1. That is, this register reads the value: {0,HCM,RCM,LCM}	R/W	2

Note: The indication of the current mode status should be read from the three states LOSC_ON, IRCH_ON, and PLL_HOSC_ON (OSC_CTL register bits 4~6). Instead, this register should be read, which only represents the mode switching command written and does not mean that it has switched to the expected mode.

It is recommended that the user call the Sharp Energy micro library function for clock switching. It is not recommended that users write to the SYS_MODE(0x4) register in the application program.

3.7.3 System power-down control register SYS_PD (0x8)

Bit	Name	Description	Read/Write	Reset Value
31:18	---	read-only, not writeable	R	0
17	ldo3_pd	LDO3 Power Switch = 0: Power down = 1: Power-up The LDO3 is controlled by the three ADC switches and is turned on whenever one ADC is turned on.	R/W	0
16	vsel_bor5	BOR5 Power-down Threshold Selection Signal =0: vil=2.2v , default configuration = 1: vil = 1.8v Chip reset threshold at power up is always vih=2.5V	R/W	0
[15:12]	Reserved		R	0
11	hysen_cmp2	Internal hysteresis comparator hysteresis switch for cmplp2	R/W	0

		0x1: Open hysteresis 0x0: Turn off hysteresis		
10	hysen_cmp1	Internal hysteresis comparator hysteresis switch for cmplp1 0x1: Open hysteresis 0x0: Turn off hysteresis	R/W	0
9	PWD_CMP2R	CMP2 internal 600K resistor sampling switch 0: CMP2 internal resistor sampling on. Peripheral circuits need attention Effect of Internal 600K Resistance to Ground, Comparator Vil Typical The hysteresis is 1.28V and the hysteresis is 0.22V, so don't assign bit11 to Set to 1; 1: CMP2 internal resistor sampling off. Comparator Threshold Typical 0.9V, no hysteresis by default; bit11 can be set to 1 to have 0.14V hysteresis, when Vil is typically 0.84V; Note: When CMP2_PD=1, the internal sampling resistor is off, when CMP2_PD=0, the internal sampling resistor is configured by PWD_CMP2Rt	R/W	0
8	PWD_CMP1R	CMP1 internal 600K resistor sampling switch 0: CMP1 internal resistor sampling is turned on, the peripheral circuit needs to pay attention to the influence of the internal 600K resistor to ground, the typical value of the comparator Vil is 1.28V, hysteresis is 0.22V, do not configure bit10 to 1 at this time; 1: CMP1 internal resistor sampling off, the typical value of the comparator threshold is 0.9V, no hysteresis by default; bit10 can be set to 1 so that there is 0.14V hysteresis, at this time Vil typical value is 0.84V;	R/W	0
7	BGRLP_PD	BGRLP Power Switch 0: Power up 1: Power down Remarks: When OSC_CTL2.PM_SEL=1, BGRLP is selected as the metering and temperature measurement reference, and BGRLP is turned on when one of the conditions is met by IA channel ADC, IB channel ADC, U channel ADC, temperature measurement startup, and BGRLP_PD register turn on.	R/W	0
6	BGR_PD	BGR Power Switch 0: Power up 1: Power down	R/W	1

		Remarks: When OSC_CTL2.PM_SEL=0, BGRLP is selected as the metering and temperature measurement reference, and the I1 channel ADC, I2 channel ADC, U1 channel ADC, temperature measurement startup, and BGR_PD register turn on BGR is turned on when one of the conditions is met.		
5	CMP2_PD	Comparator 2 Power Switch 0: Power up 1: Power down	R/W	0
4	CMP1_PD	Comparator 1 power switch 0: Power up 1: Power down	R/W	1
3	LVD_PD	LVD Power Switch 0: Power up 1: Power down	R/W	1
2	ADCU_PD	U-Channel ADC Power Switch 0: Power up 1: Power down	R/W	1
1	ADCI2_PD	I2 Channel ADC Power Switch 0: Power up 1: Power down	R/W	1
0	ADCI1_PD	I1 Channel ADC Power Switch 0: Power up 1: Power down	R/W	1

3.7.4 ADC control register ADC_CTRL (0xC)

Bit	Name	Description	Read/Write Flag	Reset Value
31:12	---	read-only, not writeable	R	0
11:9	reservations	Reserved bit, can be written as 1, has no practical meaning.	R/W	0
8:6	ADCU_PGA	U-channel ADC gain configuration =x00 1x =x01 2x = x10 4 times = x11 4 times	R/W	0
5:3	ADCI2_PGA	I2 Channel ADC Gain Configuration =x00 1x =x01 2x = x10 4 times = x11 4 times	R/W	0
2:0	ADCI1_PGA	I1 Channel ADC Gain Configuration =x00 1x =x01 2x = x10 8 times = x11 16 times	R/W	0

3.7.5 System OSC control register 2 OSC_CTRL2 (0x10)

Bit	Name	Description	Read/Write	Reset

			Flag	Value
31:23	---	read-only, not writeable	R	0
22	PM_SEL	Metering power consumption mode selection: 0: Normal power consumption mode. In EMU mode, the metering clock follows the system clock and does not support 32K master frequency; In NVM mode, the NVM clock follows the system clock, and the NVM clock uses the RCH clock at 32K master frequency, which is backward compatible; The reference voltage comes from the BGR. 1: Low power mode. EMU mode does not support configuration to low power mode; In NVM mode, the NVM clock is fixed to RCM; The reference voltage comes from the BGRLP.	R/W	0
21	---	reservations	R	0
20	RCM_PD	Internal RCM enable bit: 0: Closed; 1: Turn on.	R/W	0
18:16	RCH_FREQ	000: The frequency of RCH in RCM mode is 1.8MHz; 001: The frequency of RCH in RCM mode is 3.6MHz; 010: The frequency of RCH in RCM mode is 7.3MHz; 011: The frequency of RCH in RCM mode is 14.7Mhz; 100: The frequency of the RCH in RCM mode is 29.5Mhz; Other: reserved Note: The customer should call the library function to select the chip operating frequency, do not change the value of this bit in the application program.	R/W	0
15	RCL_LOSC_FLT_SEL	Filtered Clock Source Selection 0: Filter clock selection LOSC. 1: Filter clock selection RCL	R/W	0
14	RCL_LOSC_RTC_SEL	RTC module clock source selection 0: RTC module clock selection LOSC. 1: RTC module clock selection RCL.	R/W	0
13	RCL_LCD	0: LCD selects LOSC external low frequency crystal as clock source; 1: LCD selects RCL internal low frequency crystal as clock source;	R/W	0
12	RCL_LOSC_SYS_SEL	CPU system low frequency clock source selection	R/W	0

		0: CPU system low-frequency clock selection LOSC. 1: CPU system low-frequency clock selection RCL.		
11:10	reservations	Writable, internal test register, user should not change the default value of this register.	R/W	00
9	LOSC_WEN	= 0: The LOSC_PD bit is not writable 1; = 1: LOSC_PD bit writable 1 You must write 1 to the LOSC_WEN bit and then write 1 to the PD bit.	R/W	0
8	LOSC_PD	LOSC enable bit: 0: Open; 1: Close. This bit is also the external irrigation clock enable signal, = 1 enables the external irrigation clock; Write available only when the system is running in RC mode.	R/W	0
7:5	PLL_FREQ	The PLL frequency is fixed at 14.7456 MHz and frequency selection is achieved by digital frequency division: 000: The operating frequency is selected as 7.3728 MHz; 001: The operating frequency is selected as 14.7456MHz; 010: The operating frequency is selected as 29.4912Mhz; 011: PLL output frequency selected as 29.4912Mhz; (bisecting 58.9824Mhz) Other: reserved The customer should call the library function to select the chip operating frequency and not change the value of this bit in the application program.	R/W	000
4	PLL_HOSC_SEL	System master clock selection at full speed: 0: Selects the PLL output as the system master clock; 1: Select the spare high-frequency crystal as the system master clock. This configuration item can only be configured in RC mode and low frequency mode.	R/W	0
3	HOSC_PD	External HF oscillator enable bit: 0: Open 1: Closure	RW	1
2:0	HOSC_ FREQ	000: External high-frequency crystal is 7.3728MHz 001: External high-frequency crystal is 14.7456MHz 010: Reserved, users should not use this option 011: External high-frequency crystal oscillator is 29.4912MHz (drive enhancement)	RW	000

If the system clock is selected to be an external high-frequency crystal, the user program needs to configure the OSC_CTL2 register before calling the Sharp Energy micro library function for clock switching.

System clock configuration truth table (in PLL and HOSC modes):

PLL_HOSC_SEL	PLL_FREQ	clock source	PLL_HOSC_DIV =000	PLL_HOSC_DIV =001	PLL_HOSC_DIV =010	PLL_HOSC_DIV =011
			not crossover	bifurcation	quad	eight-way intercom
0	000	PLL	7.3728Mhz	3.6864MHz	1.8432MHz	Does not support octal frequency division, 1.8432MHz if configured
1	000	HOSC	7.3728Mhz	3.6864MHz	1.8432MHz	Does not support octal frequency division, 1.8432MHz if configured
0	001	PLL	14.7456Mhz	7.3728Mhz	3.6864Mhz	1.8432Mhz
1	001	HOSC	14.7456Mhz	7.3728Mhz	3.6864Mhz	1.8432Mhz
0	010	PLL	29.4912Mhz	14.7456Mhz	7.3728Mhz	3.6864Mhz
1	011	HOSC	29.4912Mhz	14.7456Mhz	7.3728Mhz	3.6864Mhz

3.7.6 System reset register SYS_RST (0x14)

Bits 8 to 5 of this register can only be reset by power-on/power-off reset. After power-on reset, other resets will be triggered by mistake, which will cause the reset flag to be set up, and the application needs to clear the flag to 0 before using these flags after power-on to ensure the reliability of these reset flags.

Bit	Name	Description	Read/Write	Reset Value
31:21	---	reserve	R	0
20	I2C_RST_REQ	Software reset of the I2C module: Write 1 resets the I2C Compute Module and the registers and digital logic are reset; Write 0 to cancel the I2C module reset.	R/W	0
19:14	UART_CLKG	UART5~UART0 Latch enable for CM0 reset = 0: not enabled =1: Enable lock function. When enabling CM0 reset, the UART can work normally, but locks the CPU to access the UART function, which is automatically released after CM0 reset is completed.	R/W	0
13	CM0_RST	CM0 reset flag = 0 means not occurring = 1 indicates that the reset has occurred Write 1 clears this bit, which can be reset by any reset source except the CM0 reset, which cannot clear this flag	R/W	0

		bit.		
12	CM0_ENRST	CM0 reset enable Write 1 resets CM0, but does not reset metering and metering-related modules, such as UARTs that contain pulse forwarding functionality Write 0 to cancel reset CM0 Note: CM0 reset is triggered by the rising edge, it is recommended to clear this bit to 0 before enabling CM0 reset or clear this bit to 0 after each CM0 reset.	R/W	0
11	BOR_V2P8_IF	BOR28 interrupt flag, write 1 to clear 0 = 0: Normal supply voltage = 1: Supply voltage below BOR 28 threshold When BOR_V2P8_IE=1, a CPU interrupt is generated.	R/W	0
10	BOR_V2P8_IE	BOR28 interrupt enable = 0: not enabled = 1: Enable	R/W	0
9	BOR_V2P8_ENRST	BOR28 reset CPU enable =0: does not reset CPU when supply voltage is below 2.8V =1: Reset CPU when supply voltage is below 2.8V	R/W	0
8	MCU_RST	CPU reset flag (a software reset or LOCK UP reset has occurred): = 1 indicates that this reset has occurred, = 0 indicates that it has not. Write 1 to clear	R	0
7	WDT_RST	WDT reset flag: = 1 indicates that this reset has occurred, = 0 indicates that it has not. Write 1 to clear	R	0
6	PIN_RST	External pin reset flag: = 1 indicates that this reset has occurred, = 0 indicates that it has not. Write 1 to clear	R	0
5	POWEROK_RST	Power down/up reset flag = 1 indicates that this reset has occurred, = 0 indicates that it has not. Write 1 to clear	R	1
4	---	read-only, not writeable	R	0
3	EMUREG_RST_REQ	Software reset of EMU/NVM/FLK module registers: Write 1 resets the EMU/NVM/FLK configuration registers; Write 0 to cancel the EMU/NVM/FLK configuration registers; Does not reset the EMU Module Calculation Module and Result Register; Note: EMUREG_RST_REQ write 1 will keep resetting the target until write 0 to end the reset	R/W	0
2	LOCKUP_ENRST	LOCKUP enables reset (two Hard Faults of the CPU will	R/W	0

		cause LOCKUP, if this bit is enabled, it can cause a system reset): 0: LOCKUP does not cause a system reset 1: LOCKUP causes a system reset		
1	NVM_RST_REQ	Software reset total loss of pressure calculation module: Write 1 to reset the total loss of voltage calculation module; Write 0 to cancel the full loss of voltage calculation module reset. Does not reset the full loss-of-voltage module configuration register;	R/W	0
0	EMU_RST_REQ	The software resets the EMU calculation module: Write 1 resets the EMU calculation module; Write 0 to cancel the EMU computing module reset. Does not reset the EMU module configuration registers;	R/W	0

3.7.7 Address Mapping Control Register MAP_CTRL (0x18)

Bit	Name	Description	Read/Write	Reset Value
31:5	---	read-only, not writeable	R	0
4	reservations	Writable, password protected	R/W	0
3	---	read-only, not writeable	R	0
2:0	REMAP	Address Mapping: 000: FLASH mapped at address 0 (normal mode) 001: Reservations 010: FLASH and SRAM mapped address swapping 011: Reserved, users should not use this option 100: FLASH mapped at 1/2 capacity address Other: reserved, users should not use this option	R/W	00

3.7.8 Module enable 0 register MOD0_EN (0x1C)

Bit	Name	Description	Read/Write	Reset Value
31:28	---	read-only, not writeable	R	0
27	---	reserve	R/W	0
26	CRC_EN	The CRC module enables clearing, clock gating, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
25	LPUART_EN	LPUART module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
24	---	reserve	R/W	0
23	---	reserve	R/W	0

22	---	reserve	R/W	0
21	---	reserve	R/W	0
20	SIMP_TC_EN	SIMP_TC module enables clearing and clock gating: 0: Clock stop, module clear, 1: Clock start, module enable	R/W	0
19	---	reserve	R	0
18	SPI3_EN	The SPI3 module enables clear, clock gating, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
17	SPI2_EN	The SPI2 module enables clear, clock gating, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
16	--	reserve	R	0
15	SPI0_EN	SPI0 module enable, clock gating, cm0 enter deepsleep synchronization to turn off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
14	I2C_EN	The I2C module enables, the clock gates, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
13	ISO7816_EN	The ISO7816 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
12	UART38K _EN	UART38K infrared modulation clock on enable, cm0 enter deepsleep synchronization off this clock: 0: Clock stop 1: Clock start	R/W	0
11	UART3_EN	The UART3 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
10	UART2_EN	The UART2 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
9	UART1_EN	The UART1 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
8	UART0_EN	The UART0 module is enabled, the clock is gated, and	R/W	0

		cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable		
7	UART5_EN	The UART5 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
6	UART4_EN	The UART4 module enables clearing, clock gating, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
5	TC1_EN	The TC1 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
4	TC0_EN	The TC0 module is enabled, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
3	---	reserve	R/W	0
2	---	Reserved bit, readable and writable, default value is 1; no practical significance.	R/W	1
1	---	read-only, not writeable	R	0
0	---	reserve	R/W	0

3.7.9 Module enable 1 register MOD1_EN (0x20)

Bit	Name	Description	Read/Write	Reset Value
31:19	---	read-only, not writeable	R	0
18	ECT_EN	ECT module clock enable: 0: Clock stop 1: Clock start	R/W	0
17	IOCNT _EN	IOCNT module clock enable: 0: Clock stop 1: Clock start	R/W	0
16	FLK_EN	FLK module arithmetic clock enable: 0: The clock is stopped; 1: Clock start; FLK module register clock is the same as EMU	R/W	0
15	M2M_EN	The M2M module clock is enabled and cm0 enters deepsleep to synchronize off this clock: 0: The clock is stopped; 1: Clock start;	R/W	0
14	DSP_EN	Hardware DSP core modules (FFTs, etc.) clock enable,	R/W	0

		cm0 enters deepsleep to synchronize off this clock: 0: The clock is stopped; 1: Clock start;		
13	D2F_EN	Hardware D2F module (power integrator) clock enable: 0: The clock is stopped; 1: Clock start;	R/W	0
12	NVM_REG_EN	NVM module register read/write clock gating: 0: Clock start 1: Clock stop Default startup	R/W	0
11	SAR_EN	SAR module enable, apb bus clock gating: 0: Clock stop 1: Clock start	R/W	0
10	RTC_EN	RTC apb bus clock gating, cm0 enters deepsleep to synchronize off this clock: 0: Clock stop 1: Clock start **Customers are advised not to turn off this clock.**	R/W	1
9	WDT_EN	WDT apb bus clock gating, cm0 enters deepsleep to synchronize off this clock: 0: Clock stop 1: Clock start **Customers are advised not to turn off this clock.**	R/W	1
8	NVM_EN	Full loss of voltage calculation module enabled, clock gated: 0: Clock stop 1: Clock start	R/W	0
7	EMU_EN	EMU module clock gating and FLK module register clock gating: 0: Clock stop 1: Clock start	R/W	0
6	LCD_EN	LCD module enable, clock gating: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
5	GPIO_EN	The GPIO module is enabled to clear, the clock is gated, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
4	---	reserve	R/W	0
3	SPI1_EN	The SPI1 module enables clear, clock gating, and cm0 enters deepsleep to synchronize off this clock: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
2	---	read-only, not writeable	R	0

1:0	--	reserve	R/W	0

3.7.10 INTC enable register INTC_EN (0x24)

Bit	Name	Description	Read/Write Flag	Reset Value
31:9	---	read-only, not writeable	R	0
8	INTC_EN	INTC apb module clock gating: 0: Clock stop 1: Clock start	R/W	0
7	INTC7_EN	INTC7 module enable, clock gating: 0: Clock stop 1: Clock start	R/W	0
6	INTC6_EN	INTC6 module enable, clock gating: 0: Clock stop 1: Clock start	R/W	0
5	INTC5_EN	The INTC 5 module enables clearing and clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
4	INTC4_EN	The INTC 4 module enables clearing and clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
3	INTC3_EN	The INTC3 module enables clearing and clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
2	INTC2_EN	INTC 2 module enable, clock gating: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
1	INTC1_EN	INTC 1 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
0	INTC0_EN	INTC0 module enable, clock gating: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0

3.7.11 KBI enable register KBI_EN (0x28)

Bit	Name	Description	Read/Write	Reset Value
31:9	---	read-only, not writeable	R	0
8	KBI_EN	KBI apb module clock gating: 0: Clock stop 1: Clock start	R/W	0
7	KBI7_EN	KBI 7 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0

6	KBI6_EN	KBI 6 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
5	KBI5_EN	KBI 5 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
4	KBI4_EN	KBI 4 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
3	KBI3_EN	KBI 3 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
2	KBI2_EN	KBI 2 module enable clear, clock gating: 0: Clock stopped, module cleared 1: Clock start, module enable	R/W	0
1	KBI1_EN	KBI 1 module enable, clock gating: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0
0	KBI0_EN	KBI0 module enable, clock gating: 0: Clock stopped, module off 1: Clock start, module enable	R/W	0

3.7.12 Device ID register CHIP_ID (0x2C)

Bit	Name	Description	Read/Write	Reset Value
31:24	---	read-only, not writeable	R	0
15:0	CHIP_ID	Chip version number: 8217 V2 version reads 8217 for all models All models in D version read out as RN8217 The B and C versions read out as 8215.	R	8217

3.7.13 System control password register SYS_PS (0x30)

Bit	Name	Description	Read/Write	Reset Value
31:8	---	reserve	R	0
7:0	SYS_PSW	When SYS_PSW=0x82, registers 0x00~0x28, 0x38, 0x80, 0x114 are writable; When SYS_PSW = other values, registers 0x00 to 0x28, 0x38, 0x80, 0xFC, 0x114, 0x118 are not writable; This register reads the value written. It is recommended that the user disable write enable immediately after the write operation is completed.	R/W	00

3.7.14 IR Configuration Register IRFR_CTRL (0x34)

Bit	Name	Description	Read/Write	Reset Value
31:6	---	reserve	R	0
5:0	IRFR_CYCLE	IR clock division factor in RCH mode ... 0x19:IR output clock 36.9K. 0x18: IR output clock 38.4K. 0x17:IR output clock 40K. ... Formula: RCH29M/(32*INFRARED_CYCLE) Not configurable to 0.	R/W	0x18

3.7.15 System Configuration Register SYS_CFG (0x38) (new)

Bit	Name	Description	Read/Write	Reset Value
31:16	---	reserve	R	0
15:8	RTC_SW_EN	RTC clock switching enable configuration = 0x75: cut off RTC perpetual calendar clock = Other: RTC perpetual calendar functioning properly When the RTC clock needs to switch between LOSC and RCL, you need to configure RTC_SW_EN to turn off the RTC perpetual calendar clock first, then configure OSC_CTL2[14], RCL_LOSC_RTC_SEL bit to select the clock, and then configure RTC_SW_EN to enable the perpetual calendar to run. This register is writable when SYS_PS=0x82. RTC Clock Switching Enable Configuration Steps: SYSCTL->SYS_PS=0x82; SYSCTL->SYS_CFG|=0x75<<8; SYSCTL->OSC_CTL2 |=(1<<14);	R/W	0
7:0	EXT_REF_EN	VREF external irrigation enable configuration = 0xE8: Enable VREF external irrigation = Other: Do not enable VREF external irrigation. This register is writable when SYS_PS=0x82. When EXT_REF_EN high 4bit[7:4]=0xE, low 4bit[3:0] is only writable. VREF external irrigation enable configuration steps: SYSCTL->SYS_PS=0x82; SYSCTL->SYS_CFG=0xE0; SYSCTL->SYS_CFG=0xE8;	R/W	0

3.7.16 Clock Correction Configuration Register TRIM_CFG1 (0x78)

Bit	Name	Description	Read/Write	Reset

				Value
31:30	---	reserve	R	0
29	CAL_CLK_SEL1	Refer to the description of bit26 CAL_CLK_SEL for specific definitions.	R/W	0
28	CAL_OV_IE	Calibrated clock counter overflow flag interrupt enable: 0: Do not enable interrupts; 1: Enable interrupt;	R/W	0
27	CAL_DONE_IE	Clock calibration complete flag interrupt enable: 0: Do not enable interrupts; 1: Enable interrupt;	R/W	0
26	CAL_CLK_SEL	{CAL_CLK_SEL1, CAL_CLK_SEL} together define the calibrated clock source selection: CAL_CLK_SEL1 is bit29 00: The calibrated clock source selects RCH; 01: The calibrated clock source selects RCL; 10: The source of the clock being calibrated selects RCM; 11: Reservations	R/W	0
25:24	REF_CLK_SEL	Reference Clock Source Selection 00: Reference clock source selection LOSC; 01: HOSC is selected for the reference clock source; 10: Reference clock source selection RCH; 11: Reference clock source selection PLL;	R/W	11
23:20	---	reserve	R	0
19:0	REF_CLK_CNT [19:0]	reference clock value	R/W	0x10000

3.7.17 Clock calibration start register TRIM_START (0x7C)

Bit	Name	Description	Read/Write	Reset Value
31:28	---	reserve	R	0
27	STOP	Clock calibration termination bit: 0: No operation; 1: Terminate clock calibration; Note: If clock calibration is terminated, the bit needs to be written 0 before clock calibration can be restarted.	R/W	0
26	START	Clock calibration start bit: 0: No operation; 1: Initiate clock calibration; Note: This bit is automatically cleared when clock calibration is completed or terminated.	R/W	0
25	CAL_OV	The calibrated clock counter overflow flag: 0: No overflow; 1: Spillage; Note: Write 1 to clear 0.	R/W	0

24	CAL_DONE	Clock calibration complete flag: 0: Not completed; 1: Completed; Note: Write 1 to clear 0.	R/W	0
23:20	---	reserve	R	0
19:0	CAL_CLK_CNT [19:0]	Count value returned by the calibrated clock	R	0

Examples:

1. Select the reference clock as LOSC and the calibrated clock as RCH;
2. Select the reference clock counter REF_CLK_CNT as 0x1000 with a count time of 0.125S;
3. Initiates a clock correction operation, queries a flag bit or waits for a system control interrupt to be generated;
4. Assume that the count value CAL_CLK_CNT = 0x 61A80, decimal 400000, is returned by the read corrected clock;
5. Then the measured RCH frequency value is:

   (CAL_CLK_CNT/REF_CLK_CNT)*32768Hz
   = (400000/4096)*32768Hz
   = 3200000Hz
   =3.2MHz

3.7.18 DMA Priority Configuration Register 1DMA_PRI1 (0x80) (New)

Bit	Name	Description	Read/Write	Reset Value
31:28	WKEY	WKEY is a 0~25bit write operation password protected bit, the password is 0xE. Software writing 0 to 25 bits must ensure that the high 4 bits of the data written at the same time are 0xE and that SYS_PSW is 8'h82.	R	0
27:26	DMA_CH13_PRI	Channel 13: TC1 Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
25:24	DMA_CH12_PRI	Channel 12: CAN DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
23:22	DMA_CH11_PRI	Channel 11: UART5 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
21:20	DMA_CH10_PRI	Channel 10: UART4 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
19:18	DMA_CH9_PRI	Channel 9: UART3 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
17:16	DMA_CH8_PRI	Channel 8: UART2 DMA Access SRAM Priority Configuration	R/W	0x0

		Priority configuration is the same as CH0		
15:14	DMA_CH7_PRI	Channel 7: UART1 DMA access SRAM priority configuration Priority configuration is the same as CH0	R/W	0x0
13:12	DMA_CH6_PRI	Channel 6:UART0 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
11:10	DMA_CH5_PRI	Channel 5: SPI3 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
9:8	DMA_CH4_PRI	Channel 4: SPI2 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
7:6	DMA_CH3_PRI	Channel 3: SPI1 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
5:4	DMA_CH2_PRI	Channel 2: SPI0 DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
3:2	DMA_CH1_PRI	Channel 1: EMU DMA access SRAM priority configuration Priority configuration is the same as CH0	R/W	0x0
1:0	DMA_CH0_PRI	Channel 0: CACHE access SRAM priority configuration, priority fixed at 3 0x3: highest priority; 0x2: next highest priority 0x1: low priority; 0x0: lowest priority When the priority is the same, the smaller channel number has the higher priority.	R	0x3

3.7.19 DMA Priority Configuration Register 2DMA_PRI2(0xFC) (new)

Bit	Name	Description	Read/Write	Reset Value
31:28	WKEY	WKEY is a 0~25bit write operation password protected bit, the password is 0xE. Software writing 0 to 25 bits must ensure that the high 4 bits of the data written at the same time are 0xE and that SYS_PSW is 8'h82.	R	0
27:8	---	reservations	R	0x0
7:6	DMA_CH17_PRI	Channel 17: CPU Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
5:4	DMA_CH16_PRI	Channel 16: M2M Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0
3:2	DMA_CH15_PRI	Channel 15: CRC Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0

1:0	DMA_CH14_PRI	Channel 14: DSP DMA Access SRAM Priority Configuration Priority configuration is the same as CH0	R/W	0x0

3.7.20 Chip Unique Code Register 0FAB_UID0 (0xF0) (New)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	FAB_UID0	Forms a chip unique identifier with FAB_UID1.	R	0

3.7.21 Chip Unique Code Register 1FAB_UID1 (0xF4) (New)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	FAB_UID1	Forms a chip unique identifier with FAB_UID0.	R	0

3.7.22 ADC external irrigation control register ADCIN_CTRL (0x114) (new)

Bit	Name	Description	Read/Write Flag	Reset Value
31:10	---	reservations	R	0
9	ADC_CLKO_SEL	ADC 1bit outfeed mode, ADC_CLKO clock frequency selection. = 0: 1.8432 Mhz = 1: 3.6864 Mhz	R/W	0
8	ADC_CLK_OEN	ADC 1bit outfill mode, ADC clock output enable = 0: not enabled = 1: Enable clock output Need to configure GPIO multiplexing to ADC_CLKO to have clock outputs	R/W	0
7:4	---	reservations	R	0
3	---	reservations	R/W	0
2	---	reservations	R	0
1	ADCIN_IB	IB channel external irrigation 1bit enable configuration = 0: not enabled =1: Enable IB channel external 1bit flooding mode to flood 1bit from IB_IN.	R/W	0
0	ADCIN_IA	IA channel external irrigation 1bit enable configuration = 0: not enabled =1: Enable IA channel external 1bit flood mode, flood 1bit from IA_IN.	R/W	0

3.7.23 System Chopper Configuration Register SYSCP_CON (0x118) (New)

Configured for DC applications

Bit	Name	Description	Read/Write	Reset

			Flag	Value
31:9	--	Read only, not write.	R	0
8	adc_syscp_ph	Valid only if adc_syscp_mode=1: = 0, phase is low, forward sampling; = 1, phase high, reverse sampling.	R/W	0
7:6	--	Read only, not write.	R	0
5:4	adc_syscp_sel	ADC input signal forward and reverse sample switching frequency configuration register, valid only when adc_syscp_mode=0: = 0, N = 2048; = 1, N = 4096; = 2, N = 8192; = 3, N = 16384; Note: The forward and reverse times are the same, i.e. N/2 1bit forward and N/2 1bit reverse. Switching period = (1.8432e6/N) Hz	R/W	0
3	adc_syscp_mode	syschop mode selection 0: Auto mode, ADC input sampling signal direction is automatically switched 1: Manual mode, the adc_syscp_ph configuration determines whether the ADC input sampling signal direction is forward or reverse. Note: In manual mode, the metering module judges whether to do 0/1 inverse operation according to the phase of adc system chop given by the system. If the phase is low, the analog ADC samples the signal in the forward direction, and the metering module does not invert; if the phase is high, the analog ADC samples the signal in the reverse direction, and the metering module does 0/1 inversion.	R/W	0
2	adc_syscpu_en	U-channel syschop enable: 0: not enabled 1: Enabling	R/W	0
1	adc_syscpib_en	IB channel syschop enabled: 0: not enabled 1: Enabling	R/W	0
0	adc_syscpia_en	IA channel syschop enabled: 0: not enabled 1: Enabling	R/W	0

4 CPU system

4.1 Overview

There are 2 ways (2 master devices) to initiate access to the SoC built-in devices:

◎ Cortex-M0:

- Command access and data access;
- Access to all slave devices;

◎ External SWD controller (e.g. JLINK or similarly functioning device):

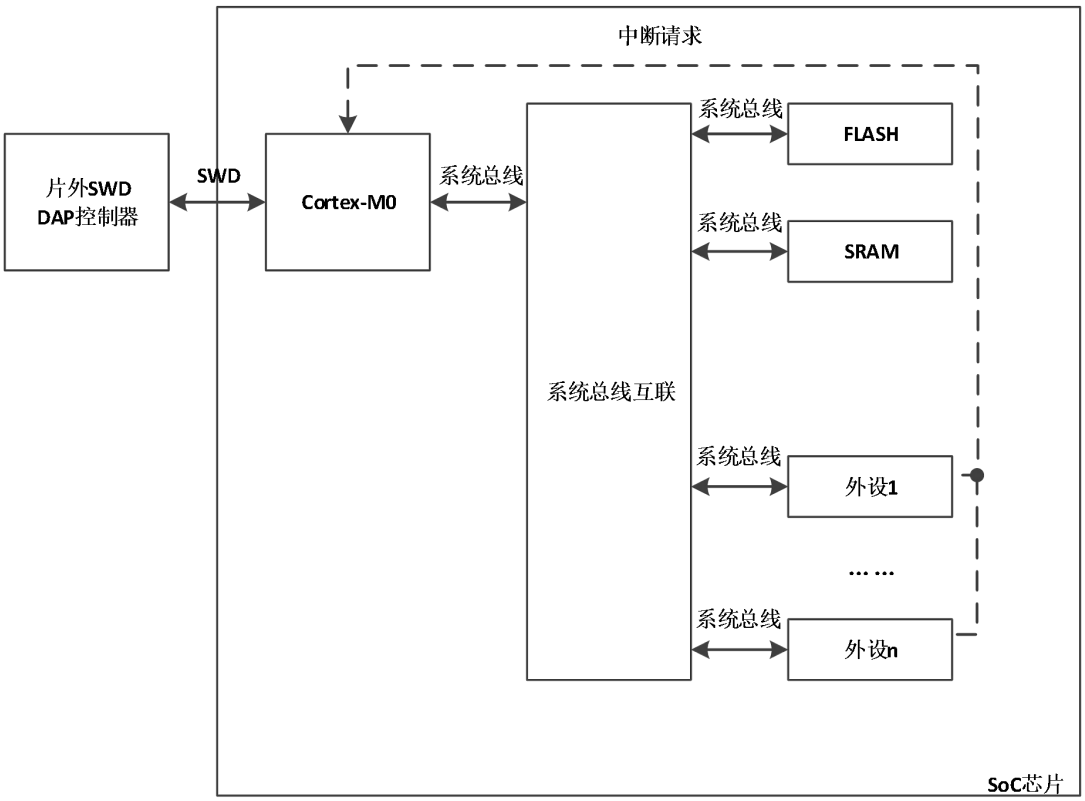
- Debugging interfaces and resource access;
- Access to all slave devices;

The SoC's built-in slave device resources include memory (FLASH and SRAM) and various peripherals (UARTs, timers, watchdogs, etc.).

Some peripherals can initiate interrupt requests, such as UARTs, timers, etc.

Some peripherals can initiate DMA requests, such as UART, LCD, etc.

Figure 4- 1 Physical interconnection architecture of SoC devices



4.2 Cortex-M0 processor

The Cortex-M0 processor is a 32-bit processor designed for embedded system applications with the following features:

◎ EASY-TO-USE PROGRAM MODEL

◎ HIGH CODE INTEGRATION WITH 32-BIT PERFORMANCE

◎ TOOLS AND BINARIES ARE UPWARDLY COMPATIBLE WITH THE CORTEX-M PROCESSOR FAMILY

FOR EASY UPGRADES AND EXPANSION

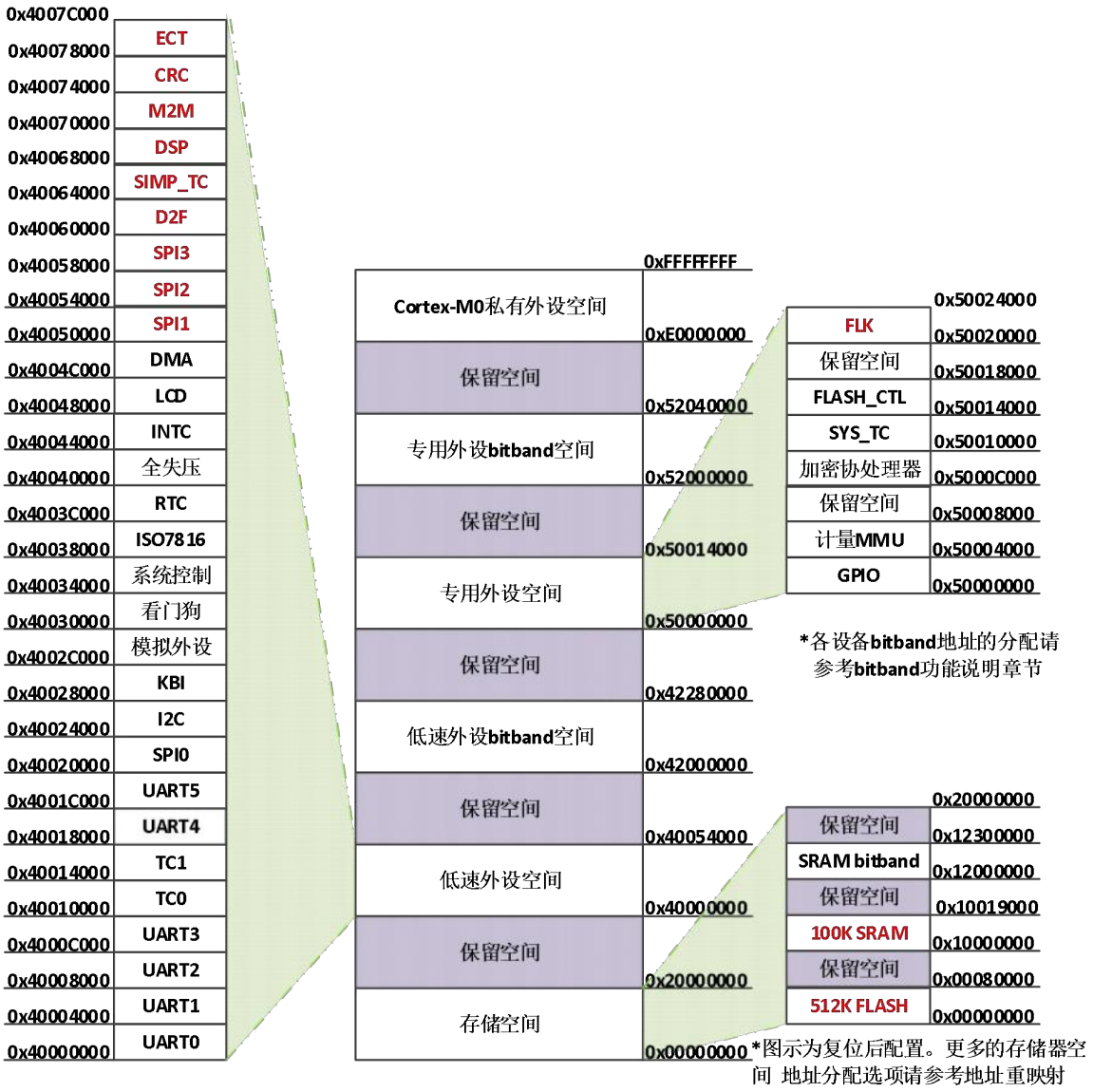
- ◎ INTEGRATED SLEEP MODE FOR EXTREMELY LOW POWER CONSUMPTION
- ◎ EFFICIENT CODE EXECUTION ALLOWS FOR LOWER PROCESSOR CLOCKS OR EXTENDED SLEEP MODES
- ◎ SINGLE-CYCLE 32-BIT HARDWARE MULTIPLIER
- ◎ ZERO JITTER INTERRUPT HANDLING
- ◎ HIGHLY EFFICIENT INTERRUPT HANDLING WITH DEFINED INTERRUPT TIMING
- ◎ SUPPORTS INTERRUPT/EXCEPTION NESTING AND PREEMPTION
- ◎ SUPPORTS 24-BIT SYSTEM BEAT COUNTER
- ◎ PROVIDES 4 INTERRUPT PRIORITIES
- ◎ SUPPORTS 2 WATCHPOINTS, 4 HARDWARE BREAKPOINTS
- ◎ SUPPORTS SERIAL DEBUGGING INTERFACE (SWD) FOR HIGH VISIBILITY AND CONTROL OF THE PROCESSOR'S INTERNAL STATE

DETAILED INFORMATION ON THE Cortex-M0 CAN BE FOUND IN THE ARM DOCUMENTATION.

4.3 Storage Mapping

For SoC memory mapping refer to " Figure - 42 SoC address space mapping ".

Figure 4 2- SoC address space mapping



4.3.1 Storage Remapping

The SoC supports address remapping of the address space of 2 memories, including FLASH and SRAM.

The memory remap operation is accomplished by configuring the REMAP bit field of register SYS_CTL in the system controller.

None of the address assignments of the peripherals are affected by memory remapping.

Table 4 1- Storage Remapping Configuration

memory device	REMAP	mapping address
flash	0	0x00000000~0x0007FFFF
	1	0x00000000~0x0007FFFF
	2	0x10000000~0x1007FFFF
	3	Reserved, not available
SRAM	0	0x10000000~0x10018FFF
	1	0x10000000~0x10018FFF
	2	0x00000000~0x00018FFF

	3	Reserved, not available

4.3.2 Bitband

The system supports the bitband function for three address spaces:

SRAM space:

.0x10000000~0x10018FFF mapped to 0x12000000~0x1205FFFF

.0x00000000~0x00018FFF mapped to 0x02000000~0x0205FFFF

Peripheral space:

. 0x40000000~0x4004FFFF maps to 0x42000000~0x423FFFFF;

.0x50000000~0x50003FFF mapped to 0x52000000~0x5201FFFF; (GPIO)

Access to the bitband area is equivalent to accessing specific bits in the peripheral registers.

The address is the btband address corresponding to the yth bit of the memory cell with address x:

$$Z = (X \ \& \ 0xFC000000) + 0x02000000 + (Y << 2) + ((X << 5) \ \& \ 0x03FFFFFF)$$

4.3.3 SRAM

- system SRAM

The maximum capacity of the on-chip SRAM is 96KB, with addresses 0x1000_0000~0x1001_8000, of which the high 4KB is for CACHE use and should not be used by the user;

RAM runs at the same frequency as the processor;

Supports random access to 8-bit, 16-bit, or 32-bit data and can be used as storage for code or data.

- Algorithmic SRAM

The chip contains 4KB SRAM as the encryption module algorithm RAM, which can also be used as a normal RAM when the encryption module is not working and is accessed by the CPU at addresses 0x1001_8000~0x1001_9000.

WDT, external pins, software reset, etc. will not erase the data in SRAM, but it should be noted that: BOOTROM uses an address space of 92KB~96KB, once the system reset occurs, the cpu will execute the startup program from the BOOTROM, and the data in this address space will be occupied, so please pay attention to this feature when using this address space.

4.3.4 Flash

The SoC has a maximum of 512KB FLASH built-in:

◎ Minimum of 100,000 erasures;

◎ Minimum data retention time of 20 years;

◎ The storage area contains 32 blocks, each block contains 32 pages, and each page contains 512 Bytes.

◎ Supports 8-bit, 16-bit and 32-bit random reads;

◎ Support page erase, block erase, page programming, the specific operation needs to call the Reynolds Micro library function (nvm.a(IAR)/nvm.lib(KEIL))

◎ **FLASH is automatically turned off or on for low power applications;**

The library functions (nvm.a(IAR)/nvm.lib(KEIL)) provide the following interfaces to the FLASH operation functions:

uint8_t flashPageErase(uint32_t pg)
uint8_t flashSectorErase(uint32_t sec)
uint8_t flashProgram(uint32_t dst_addr, uint32_t src_addr, uint32_t len)

For details, please refer to SOC_MCU Application Note 002 - Library Function Usage Description.

4.4 Interrupt Allocation

The SoC supports 32 interrupts, of which 8 external interrupts, external interrupts 0 to 7, are open.

Refer to the ARM-M0 manual for detailed information on interrupts, such as priority mask registers, Nested Vector Interrupt Controller (NVIC), and so on.

Table 4 2- Interrupt/Exception Vector Table and Configuration Information

Exception No.	Interrupt No.	Vector Name	Interrupt Vector Address	Priority
-	-	MSP initial value	0x00	-
1	-	reset (a dislocated joint, an electronic device etc)	0x04	-3, max.
2	-14	unmaskable interrupt	0x08	-2
3	-13	HARDFAULT interrupt	0x0C	-1
4 to 10	-12 to 6	reservations	0x10 to 0x28	-
11	-5	system call	0x2C	configurable
12-13	-4 to -3	reservations	0x30 to 0x34	-
14	-2	PendSV	0x38	configurable
15	-1	system beat counter	0x3C	configurable
16	0	System Control/EMU_RCD	0x40	configurable
17	1	CMP/LVD	0x44	configurable
18	2	PWRSWH/EMU2	0x48	configurable
19	3	RTC	0x4C	configurable
20	4	EMU/D2F	0x50	configurable
21	5	MADC/FLK	0x54	configurable
22	6	UART0	0x58	configurable
23	7	UART1	0x5C	configurable
24	8	UART2	0x60	configurable
25	9	UART3	0x64	configurable
26	10	SPI0	0x68	configurable
27	11	I2C	0x6C	configurable
28	12	7816_0/SPI3	0x70	configurable
29	13	7816_1/SPI2	0x74	configurable
30	14	TC0	0x78	configurable
31	15	TC1	0x7C	configurable
32	16	UART4	0x80	configurable
33	17	UART5/LPUART	0x84	configurable
34	18	Watchdog WDT	0x88	configurable
35	19	KBI	0x8C	configurable
36	20	LCD/DSP cores	0x90	configurable
37	21	SEA/SYS_TC	0x94	configurable
38	22	EMU_DMA	0x98	configurable

39	23	NVM total loss of voltage / SPI1	0x9C	reservations
40	24	External interrupt 0/INTx (0~7 combined)	0xA0	configurable
41	25	External Interrupt	0xA4	configurable
42	26	External Interrupt	0xA8	configurable
43	27	External Interrupt	0xAC	configurable
44	28	External Interrupt	0xB0	configurable
45	29	External Interrupt 5/M2M	0xB4	configurable
46	30	External Interrupt 6/CRC	0xB8	configurable
47	31	External Interrupt 7/ECT	0xBC	configurable

Note: The actual stack top is two words higher than the one assigned by the compiler, e.g., the stack top assigned by the compiler is 0x10001918, but the actual one is 0x10001920; be careful not to assign these two words to other variables when applying.

4.5 Interrupt application

You can use each SOC interrupt by adding the SOC header file #include <RN8xxx_V2.h> to the header file. The RN8xxx_.h file contains some of the header files defined by the Cortex-M0, core_cmFunc.h, core_cmFunc.h, and core_cmInstr.h. All of the above files can be found in the header files provided by Reynolds Micro.

Disable interrupt enable: __disable_irq().

Enable general interrupts: __enable_irq().

Interrupt operation

The interrupt program of each module can be completely written in C language, and users do not need to consider the problem of stack-in and stack-out. The interrupt operation steps are as follows, taking the KBI interrupt as an example:

1、 Enable general interrupts: __enable_irq().

2、 To configure a module that needs to generate interrupts, such as a KBI module, set KBI_MASK to interrupt enable.

3、 Enable KBI interrupt: find the interrupt number in RN8xxx.h and turn on the interrupt, for example, the interrupt number of KBI is KBI_IRQn, turn on the KBI interrupt as NVIC_EnableIRQ(KBI_IRQn), if you need to set the priority of the interrupt you can use void NVIC_SetPriority(IRQn_t IRQn , uint32_t priority). uint32_t priority).

4、 Write the interrupt service function, for different interrupts, the function name has been fixed and can be found in the vector table of startup_RN821x.s. For example, the KBI interrupt service program function name is KBI_HANDLER and the interrupt service function can be written as:

```
void KBI_HANDLER(void)
        {
            /* Start adding user code. Do not edit comment generated here */
        }
```

5、 Turn off interrupt enable: void NVIC_DisableIRQ0 (IRQn_t IRQn).

5 Metering

5.1 Features

- Basic metering
  - 3 channels Σ - Δ ADC, internal PGA, configurable magnification, of which IA channel supports up to 16 times.
  - Active energy and reactive energy metering error less than 0.1% in the dynamic range of 8000: 1
  - Reference voltage coefficient is 5ppm/℃ typically
  - Support external reference voltage. When input external reference voltage, it’s necessary to call Renergy library functions.
  - Support measurement active power, reactive power, apparent power, and current RMS value of null and live line channel simultaneously
  - Support meter active energy, reactive energy and apparent energy of null-line and fire-line channel simultaneously.
  - Support measurement voltage RMS and voltage line frequency, and the update speed of frequency is 1-cycle and 32-cycle optional.
  - Support sampling channel gain and offset calibration.
  - Provide power factor.
  - Provide NVM (no-voltage metering) solution.
  - Provide DC metering solution.
  - Provide monitoring of voltage swells and sags event and current overload event.
  - Provide harmonic analysis solutions.
  - Provide the original sampling data of the three-channel metering sigma-delta ADC, which is convenient for the development of secondary algorithms
  - Provide intelligent and safe electricity solutions
  - Support Rogowski Current Coil
  - Support half-wave metering mode, bidirectional metering mode and fundamental-wave metering mode.
  - Electrical coefficient has 3 independent sets configurable.
  - Support ADC reverse input
  - Support ADC external input
  - Active/reactive energy support 4 energy accumulation: algebraic sum, positive, absolute, and negative
- Simultaneous sampling waveform output
  - Provide flexible ADC simultaneous sampling waveform data
  - Support flexible calibration methods, gain calibration, phase calibration, and harmonic compensation
  - Waveform data can be transferred from metering to RAM via DMA
- Energy metering
  - Provide half-cycle active power and half-cycle RMS of simultaneous sampling channel
  - Provide half-cycle update’s full-wave voltage/current RMS and active power.
  - Provide half-cycle update’s fundamental-wave voltage/current RMS and active power.

Note1: For details about enabling the ADC, setting the gain of the ADC, and enabling the metering clock, see the System Control section.

5.2 Register list

5.2.1 Metering configuration and status registers

Offset address	Name	R/W	Word length	Reset value	Description	Checksum
Calibration parameters and metering control registers, basic address: 0x50004000						
00H	EMUCON	R/W	3	1C0007	Metering control register, write protect	checksum 1
04H	EMUCON2	R/W	3	0	Metering control register, write protected	checksum 1
08H	HFConst	R/W	2	1000	Pulse frequency register, write protected	checksum 1
0CH	PStart	R/W	2	60	Active start power configuration, write protected	checksum 1
10H	QStart	R/W	2	120	Reactive start power configuration, write protected	checksum 1
14H	GPQA	R/W	2	0	A channel power gain calibration register, write protected	checksum 1
18H	GPQB	R/W	2	0	B channel power gain calibration register, write protected	checksum 1
1CH	PhsA	R/W	2	0	A channel phase calibration register, the calibration scale is approximately 0.01 degrees, write protected. The calibration range has changed, please refer to the function introduction or register description for details.	checksum 1
20H	PhsB	R/W	2	0	B channel phase calibration register, the calibration scale is approximately 0.01 degrees, write protected. The calibration range has changed, please refer to the function introduction or register description for details.	checksum 1
24H	QPhsCal	R/W	2	0	Reactive power phase calibration, write protected.	checksum 1
28H	APOSA	R/W	2	0	A channel active offset calibration register, write protected.	checksum 1
2CH	APOSB	R/W	2	0	B channel active offset calibration register, write protected.	checksum 1
30H	RPOSA	R/W	2	0	A channel reactive offset calibration register, write protected.	checksum 1
34H	RPOSB	R/W	2	0	B channel reactive offset calibration register, write protected.	checksum 1
38H	IARMSOS	R/W	2	0	A channel RMS offset calibration register, write protected.	checksum 1
3CH	IBRMSOS	R/W	2	0	B channel RMS offset calibration register, write protected.	checksum 1

40H	URMSOS	R/W	2	0	Voltage channel RMS offset calibration register, write protected (the same as IARMSOS and IBRMSOS). It's working on RMS, apparent power and apparent energy.	checksum 1
44H	IAGAIN	R/W	2	0	Current A channel gain configuration, write protected. Use way is the same as IBGAIN, and working on RMS, apparent power and apparent energy.	checksum 1
48H	IBGAIN	R/W	2	0	Current B channel gain configuration, write protected.	checksum 1
4CH	UGAIN	R/W	2	0	Voltage channel gain configuration, write protected. Use way is the same as IBGAIN, and working on RMS, apparent power and apparent energy.	checksum 1
50H	IADCOS	R/W	3	0	Current A channel DC Offset calibration, 24bit, write protected	checksum 1
54H	IBDCOS	R/W	3	0	Current B channel DC Offset calibration, 24bit, write protected	checksum 1
58H	UDCOS	R/W	3	0	Voltage channel DC Offset calibration, 24bit, write protected	checksum 1
5CH	UADD	R/W	3	0	Voltage channel bias register, 24 bits, used for writing fixed voltage values during apparent energy metering, only affecting apparent energy. No impact on active, reactive, or effective value, write protected.	checksum 1
60H	USAG	R/W	2	0	Voltage sag threshold setting, write protection; Do not enable this function when the value is 0; When a non-zero value is written and a sag detection is initiated, the detection result is interrupted and reported.	checksum 1
64H	IAPEAK	R/W	2	0	Current A channel peak detection threshold setting, write protected.	checksum 1
68H	IBPEAK	R/W	2	0	Current B channel peak detection threshold setting, write protected.	checksum 1
6CH	UPEAK	R/W	2	0	Voltage channel peak detection threshold setting, write protected.	checksum 1
70H	D2FP	R/W	4	0	Custom power register. When SADD=011, the power value will be write in this register, the electrical energy can be calculated by integrating the written power value through the apparent channel.	No checksum

74H	EMUCON3	R/W	3	0	Metering control register 3, write protected	checksum 2
78H	EMUCON4	R/W	3	F5F5	Metering control register 4, used to configure the second and third sets of active and reactive energy accumulation modes, write protected.	checksum 2
7CH	EMUCON5	R/W	3	D34	Metering control register 4, used to configure the fundamental-wave active energy accumulation mode, write protected.	checksum 2
80H	CF_CFG	R/W	3	10543	Pulse output configuration register, used to configure pulse output mode1, write protected.	checksum 2
84H	HWRMS_CFG	R/W	3	0	Half-cycle RMS configuration register, used to configure the half-cycle update RMS, write protected.	checksum 2
88H	HWP_CFG	R/W	3	0	Half-cycle active power configuration register, used to configure the half-cycle full-wave active power, write protected.	checksum 2
8CH	HWFP_CFG	R/W	3	0	Half-cycle fundamental-wave active power configuration register, used to configure the half-cycle fundamental-wave active power, write protected.	checksum 2
90H	HWQ_CFG	R/W	3	0	Half-cycle reactive power configuration register, used to configure the half-cycle full-wave reactive power, write protected.	checksum 2
94H	HFConst2	R/W	2	1000	Configure the constant of quick pulse counting 2, write protected.	checksum 2
98H	HFConst3	R/W	2	1000	Configure the constant of quick pulse counting 3, write protected.	checksum 2
9CH	ADCNEG_EN	R/W	3	0	ADC reverse input enable configuration register, write protected.	checksum 2
A0H	EMUMODE	R/W	3	0	Metering mode configuration register, write protected.	checksum 2
A4H	ATCHOP_CFG	R/W	3	0	Automatic mode configuration register, write protected.	checksum 2
A8H	FGAIN	R/W	2	-	Fundamental-wave channel gain calibration register, write protected.	checksum 2
ACH	APOSFA	R/W	2	0	A channel fundamental active power offset calibration register, write protected.	checksum 2
B0H	APOSFB	R/W	2	0	B channel fundamental active power	checksum 2

					offset calibration register, write protected.	
B4H	IAHWRMSOS	R/W	2	0	Current A channel half-cycle RMS offset calibration register, write protected.	checksum 2
B8H	IBHWRMSOS	R/W	2	0	Current B channel half-cycle RMS offset calibration register, write protected.	checksum 2
BCH	UHWRMSOS	R/W	2	0	Voltage channel half-cycle RMS offset calibration register, write protected.	checksum 2
300H	ZXOTCFG	R/W	2	1C	Zero-crossing calculation configuration and flag register, write protected.	checksum 2
304H	ZXOTI	R/W	2	34	Current channel zero-crossing threshold register, write protected.	checksum 2
308H	ZXOTU	R/W	2	2D0	Voltage zero-crossing threshold register, write protected.	checksum 2
30CH	ROS_CTRL	R/W	2	0	Rogowski Current Coil integral enable control register, write protected.	checksum 2
310H	ROS_DCATTC	R/W	2	7FDF	Rogowski Current Coil integral DC attenuation coefficient register, write protected.	checksum 2
314H	ROS_TRANK	R/W	2	2CB	Rogowski Current Coil integral transform coefficient register, write protected.	No checksum
318H	PQSRUN	R/W	3	0	Electrical energy accumulation enable register, write protected.	checksum 2
330H	ECT_EN	R/W	4	0	The enable register for ECT to be effective for measurement. Any byte value that satisfies 0xd9715a33, ECT_ Gain plays a role in measurement.	No checksum
334H	ECT_IAGAIN	R/W	2	0	IA channel ECT gain register	No checksum
338H	ECT_IBGAIN	R/W	2	0	IB channel ECT gain register	No checksum
33CH	ECT_UGAIN	R/W	2	0	U channel ECT gain register	No checksum
Interrupt and DMA registers						
18CH	EMUIE	R/W	4	0	Interrupt enable register, write protected	
190H	EMUIF	R/W	4	0	Interrupt flag register, write 1 and cleared	
1A0H	EMUIE2	R/W	3	0	Interrupt enable register 2, write protected	
1A4H	EMUIF2	R/W	3	0	Interrupt flag register 2, write 1 and cleared	
1B0H	EMUIE3	R/W	3	0	Interrupt enable register 3, the interrupt relative with DMA, write protected	

1B4H	EMUIF3	R/W	3	0	Interrupt flag register 3, write 1 and cleared	
194H	--	R/W	3	0	Delete, reserved address	
Status registers						
188H	EMUStatus2	R	4	0	Metering status register 2	
198H	Rdata	R	4	--	Data of last time read	
19CH	Wdata	R	4	--	Data of last time written	
1ACH	EMUStatus3	R	3	FD5460	Checksum register 2	
1B8H	---	R	3	0	Reserved	
Special registers						
1A8H	SPCMD				Special command register	

5.2.2 Metering parameter registers list

Offset address	Name	R/W	Word length	Reset value	Description
Metering parameter and status registers, basic address: 0x50004000					
C0H	PFBCnt	R/W	2	0	B channel quick active pulse counting, write protected
C4H	QFBCnt	R/W	2	0	B channel quick reactive pulse counting, write protected
C8H	SFBCnt	R/W	2	0	B channel quick apparent pulse counting, write protected
E0H	PFBCnt2	R/W	2	0	B channel quick active pulse counting 2, write protected
E4H	QFBCnt2	R/W	2	0	B channel quick reactive pulse counting 2, write protected
E8H	PFBCnt3	R/W	2	0	B channel quick active pulse counting 3, write protected
ECH	QFBCnt3	R/W	2	0	B channel quick reactive pulse counting 3, write protected
F0H	PFACnt2	R/W	2	0	A channel quick active pulse counting 2, write protected
F4H	QFACnt2	R/W	2	0	A channel quick reactive pulse counting 2, write protected
F8H	PFACnt3	R/W	2	0	A channel quick active pulse counting 3, write protected
FCH	QFACnt3	R/W	2	0	A channel quick reactive pulse counting 3, write protected
100H	PFACnt	R/W	2	0	A channel quick active pulse counting, write protected
104H	QFACnt	R/W	2	0	A channel quick reactive pulse counting, write

					protected
108H	SFACnt	R/W	2	0	A channel quick apparent pulse counting, write protected
10CH	IARMS	R	3	0	ADC sampling current channel A RMS, update speed is 14.0625Hz.
110H	IBRMS	R	3	0	ADC sampling current channel B RMS, update speed is 14.0625Hz.
114H	URMS	R	3	0	ADC sampling voltage channel RMS, update speed is 14.0625Hz.
118H	UFREQ	R	2	0x2400	Voltage frequency. Update speed is changed, please refer to function description or register description.
11CH	PowerPA	R	4	0	A channel active power, update speed is 1.7578125Hz.
120H	PowerPB	R	4	0	B channel active power, update speed is 1.7578125Hz.
124H	PowerQA	R	4	0	A channel reactive power, update speed is 14.0625Hz.
128H	PowerQB	R	4	0	B channel reactive power, update speed is 14.0625Hz.
12CH	PowerSA	R	4	0	A channel apparent power, update speed is 14.0625Hz.
130H	PowerSB	R	4	0	B channel apparent power, update speed is 14.0625Hz.
134H	EnergyPA	R	3	0	A channel active energy, which can be configure as clear or don't clear after read, and clear after read is default.
138H	EnergyPB	R	3	0	B channel active energy, which can be configure as clear or don't clear after read, and clear after read is default.
13CH	EnergyQA	R	3	0	A channel reactive energy, which can be configure as clear or don't clear after read, and clear after read is default.
140H	EnergyQB	R	3	0	B channel reactive energy, which can be configure as clear or don't clear after read, and clear after read is default.
144H	EnergySA	R	3	0	A channel apparent energy, which can be configure as clear or don't clear after read, and clear after read is default.
148H	PFA	R	3	0	A channel power factor
14CH	PFB	R	3	0	B channel power factor
150H	ANGLEA	R	2	0	Included angle between fundamental-wave current A channel and fundamental-wave voltage.
154H	ANGLEB	R	2	0	Included angle between fundamental-wave current B channel and fundamental-wave voltage.

15CH	SPL_IA	R	3	0	Metering sampling current A channel instantaneous waveform sampling value after high pass filter, update speed 7.2KHz
160H	SPL_IB	R	3	0	Metering sampling current B instantaneous waveform sampling value after high pass filter, update speed 7.2KHz
164H	SPL_U	R	3	0	Metering sampling voltage channel high-pass filter instantaneous waveform sampling value after high pass filter, update speed 7.2KHz
168H	PowerPA2	R	4	0	A channel active power 2, update speed 14.0625Hz.
16CH	PowerPB2	R	4	0	B channel active power 2, update speed 14.0625Hz.
170H	EnergySB	R	3	0	B channel apparent energy, cleared or don't clear after read can be configure, default cleared after reading.
174H	SPL_PA	R	3	0	A channel simultaneous active power, update speed is 7.2KHz or half-cycle (100Hz typical). The 24bit is not enough, need to switch in 32bit output when hafl-cycle update.
178H	SPL_PB	R	3	0	B channel simultaneous active power, update speedis 7.2KHz or half-cycle (100Hz typical). The 24bit is not enough, need to switch in 32bit output when hafl-cycle update.
17CH	SPL_QA	R	3	0	A channel simultaneous reactive power, update speedis 7.2KHz or half-cycle (100Hz typical). The 24bit is not enough, need to switch in 32bit output when hafl-cycle update.
180H	SPL_QB	R	3	0	B channel simultaneous reactive power, update speed is 7.2KHz or half-cycle (100Hz typical). The 24bit is not enough, need to switch in 32bit output when half-cycle update.
184H	---	R	4	0	Reserved. Read only.
200H	HW_RMSIA	R	3	0	Fundamental-wave current RMS of half-cycle fundamental current A channel, update speed is 100Hz typical.
204H	HW_RMSIB	R	3	0	Fundamental-wave current RMS of half-cycle fundamental current B channel, update speed is 100Hz typical.
208H	HW_RMSU	R	3	0	Fundamental-wave current RMS of half-cycle fundamental voltage channel, update speed is 100Hz typical.
20CH	HW_FPA	R	4	0	Fundamental-wave active power of half-cycle fundamental current A channel, update speed is 100Hz typical.

210H	HW_FPB	R	4	0	Fundamental-wave active power of half-cycle fundamental current B channel, update speed is 100Hz typical.
214H	SPL_IA2	R	3	0	Metering sampling current A channel instantaneous waveform sampling value before high pass filter, update speed 14.4KHz.
218H	SPL_IB2	R	3	0	Metering sampling current B channel instantaneous waveform sampling value before high pass filter, update speed 14.4KHz.
21CH	SPL_U2	R	3	0	ADC sampling voltage channel instantaneous waveform sampling value before high pass filter, update speed 7.2KHz.
22CH	SPL_FIA	R	3	0	Instantaneous fundamental-wave waveform sampling value of fundamental-wave current A channel, update speed 7.2KHz.
230H	SPL_FIB	R	3	0	Instantaneous fundamental-wave waveform sampling value of fundamental-wave current B channel, update speed 7.2KHz.
234H	SPL_FU	R	3	0	Instantaneous fundamental-wave waveform sampling value of fundamental-wave voltage channel, update speed 7.2KHz.
238H	EnergyPA2	R	3	0	A channel active energy 2, cleared or don't clear after read can be configure, default cleared after reading.
23CH	EnergyPB2	R	3	0	B channel active energy 2, cleared or don't clear after read can be configure, default cleared after reading.
240H	EnergyQA2	R	3	0	A channel reactive energy 2, cleared or don't clear after read can be configure, default cleared after reading.
244H	EnergyQB2	R	3	0	B channel reactive energy 2, cleared or don't clear after read can be configure, default cleared after reading.
248H	EnergyPA3	R	3	0	A channel active energy 3, cleared or don't clear after read can be configure, default cleared after reading.
24CH	EnergyPB3	R	3	0	B channel active energy 3, cleared or don't clear after read can be configure, default cleared after reading.
250H	EnergyQA3	R	3	0	A channel reactive energy 3, cleared or don't clear after read can be configure, default cleared after reading.
254H	EnergyQB3	R	3	0	B channel reactive energy 3, cleared or don't clear after read can be configure, default cleared after

					reading.
258H	IADCOS_Calc	R	3	0	AUTO DC current A channel DC Offset calibration register
25CH	IBDCOS_Calc	R	3	0	AUTO DC current B channel DC Offset calibration register
260H	UDCOS_Calc	R	3	0	AUTO DC voltage channel DC Offset calibration register.

5.2.3 Simultaneous sampling channel registers

Base address: 0x40040080, no checksum

Offset address	Name	R/W	Word length	Reset value	Description	Checksum
Calibration parameter and control registers, base address: 0x40040080						
00H	WAVE_WKEY	R/W	1	0	Simultaneous sampling channel write key.	
04H	WAVECFG	R/W	3	0	Simultaneous sampling channel configuration register, with write protect.	
08H	WAVECFG2	R/W	3	0	Simultaneous sampling channel configuration register, with write protect.	
0CH	WAVE_EN	R/W	1	0	Simultaneous sampling channel enable register, with write protect.	
10H	WAVECNT	R/W	2	0	Simultaneous sampling channel sampling rate control register, with write protect.	
14H	WAVE_DC_EN	R/W	2	0	Simultaneous sampling channel AUTO DC enable register, with write protect.	
18H	WAVE_PhsIA_	R/W	2	0	A channel phase calibration of simultaneous sampling current A channel, with write protect.	
1CH	WAVE_PhsIB	R/W	2	0	B channel phase calibration of simultaneous sampling current B channel, with write protect.	
20H	WAVE_PhsU	R/W	2	0	Voltage channel phase calibration of simultaneous sampling voltage channel, with write protect.	
24H	WAVE_IAGain	R/W	2	0	A channel gain register of simultaneous sampling current A channel, with write protect.	

28H	WAVE_IBGain	R/W	2	0	B channel gain register of simultaneous sampling current B channel, with write protect.	
2CH	WAVE_UGain	R/W	2	0	Voltage channel gain register of simultaneous sampling voltage channel, with write protect.	
50H	WAVE_HW_RMSIA	R	3	0	Half-cycle RMS of simultaneous sampling current A channel.	
54H	WAVE_HW_RMSIB	R	3	0	Half-cycle RMS of simultaneous sampling current B channel.	
58H	WAVE_HW_RMSU	R	3	0	Half-cycle RMS of simultaneous sampling voltage channel.	
5CH	WAVE_HW_PA	R	4	0	Half-cycle active power of simultaneous sampling current A channel.	
60H	WAVE_HW_PB	R	4	0	Half-cycle active power of simultaneous sampling current B channel.	

5.2.4 DMA waveform buffer registers list

Base address: 0x50004000

Calibration pameter and control registers, base address: 0x40040080						
Offset address	**Name**	**R/W**	**Word length**	**Reset value**	**Description**	**Checksum**
400H	DMA_WAVE_CFG	R/W	2	1C	DMA waveform buffer configuration register, write protect.	checksum2
404H	DMA_BUF_CTRL	R/W	1	0	DMA waveform buffer enable register, write protect.	checksum2
408H	DMA_BUF _BADDR	R/W	2	0	DMA waveform buffer base address register, write protect.	checksum2
40CH	DMA_BUF_DEPTH	R/W	2	008F	DMA waveform buffer depth register, write protect.	checksum2
410H	DMA_GAP_CFG	R/W	3	0	Channel gap configuration register, with write protect.	checksum2
414H	DMA_BUF_ADDR	R	2	0	Current DMA waveform buffer pointer address.	no checksum
418H	DMA_ERR_ADDR	R	2	0	DMA waveform buffer error address register.	no checksum

41CH	DMA_CHECKSUM	R	3	0	DMA waveform checksum register.	no checksum
420H	DMA_RCD_CFG	R/W	3	0	Residual current DMA waveform buffer configuration register, with write protect.	checksum2
424H	DMA_BUF_RCD_CTRL	R/W	3	0	Residual current DMA waveform buffer enable register, with write protect.	checksum2
428H	DMA_BUF_RCD_BADDR	R/W	3	0	Residual current DMA waveform buffer offset address of target address register, with write protect.	checksum2
42CH	DMA_BUF_RCD_DEPTH	R/W	3	0	Bank residual current DMA waveform buffer Bank block size, with protect.	checksum2
430H	DMA_BUF_RCD_ADDR	R	2	0	Current Residual current DMA waveform buffer pointer address.	no checksum
434H	DMA_BUF_RCD_ERR_ADDR	R	2	0	Error address register of Residual current DMA waveform buffer.	no checksum

5.2.5 RCD registers for intelligent micro circuit breakers list

Base address: 0x50004000, no checksum

Offset address	Name	R/W	Word length	Reset value	Description
Intelligent micro circuit breakers RCD					
480H	RCD_CTRL	R/W	4	0xF0235	RCD control register
484H	RCD_EN	R/W	4	0	RCD enable control register
488H	RCD_THRE	R/W	4	0x6CA024F	RCD input signal threshold register
48CH	RCD_ATTHRE	R/W	4	0xC800C8	RCD threshold register of solution A
490H	RCD_BTTHRE	R/W	4	0x4C	RCD threshold register of solution B
494H	RCD_ACNT	R	4	0	RCD integrator output register of solution A
498H	RCD_BCNT	R	4	0	RCD integrator output register of solution B
49CH	RCD_IE	R/W	4	0	RCD interrupt enable register
4A0H	RCD_IF	R/W	4	0	RCD interrupt flag register
4A4H	RCD_STA	R	4	0	RCD status register
Intelligent micro circuit breakers trig signal generator					
4B0H	TRIG_CTRL	R/W	4	0x7	TRIG control register
4B4H	TIRG_EN	R/W	4	0	Universal trig software enable control register
4B8H	TRIG_STOP	R/W	4	0	Trig over control register
4BCH	TRIG_LEN	R/W	4	0x12001	Universal trig signal length control register
4C0H	TRIG_DLY	R/W	4	0	Universal trig start delay register

4C4H	TRIG_STA	R	4	0	Universal trig status register
4C8H	TRIG_LEN2	R/W	4	0x12001	Dedicated hardware trig length register
4CCH	TRIG_STA2	R	4	0	Dedicated hardware trip status register

5.3 Register description

5.3.1 Metering configuration register

5.3.1.1 Metering control register EMUCON (0x0)

Metering control register EMUCON

Offset address: 00H; Word length: 3 bytes; default: 0x1C0007

Bit	Name	Description	R/W	Reset value
31: 24	--	Read only	R	0
23	Cf2_cfg2	Related to EMUCON2CF2_ CFG is used in conjunction to determine which type of electrical pulse the QF pin outputs	R/W	0
22	Cf1_cfg2	Related to EMUCON2CF2_ CFG is used in conjunction to determine which type of electrical pulse the PF pin outputs	R/W	0
21	Sag_Freq_sel	=0: SAG (voltage sag) cycle is 50Hz application =1: SAG (voltage sag) cycle is 60Hz application	R/W	0
20	SBRUN	=1: enable B channel apparent energy register accumulation =0: disable B channel apparent energy register accumulation	R/W	1
19	QBRUN	=1: enable B channel reactive energy register accumulation =0: disable B channel reactive energy register accumulation	R/W	1
18	PBRUN	=1: enable B channel active energy register accumulation =0: disable B channel active energy register accumulation	R/W	1
17	CF3_CFG	=0: Original SF pin=SFA =1: Original SF pin=SFB	R/W	0
16	U_start	=0: The voltage channel participates in the calculation of apparent energy =1: The voltage channel does not participate in the calculation of apparent energy, only UADD participates	R/W	0
15: 14	QMOD	Reactive energy accumulation mode select: =00, algebra accumulation mode, both positive and negative power participate in accumulation, and negative power is indicated by the REVQ symbol; =01, positive mode, only accumulation positive power; =10, absolution accumulation mode. After taking the absolute value, both the positive and negative power participate in accumulation, and there is no negative power symbol indication; =11, negative mode, only accumulation negative power.	R/W	0
13: 12	PMOD	Active energy accumulation mode select: =00, algebra accumulation mode, both positive and negative	R/W	0

		power participate in accumulation, and negative power is indicated by the REVQ symbol; =01, positive mode, only accumulation positive power; =10, absolution accumulation mode. After taking the absolute value, both the positive and negative power participate in accumulation, and there is no negative power symbol indication; =11, negative mode, only accumulation negative power.		
11	ZXD1	The initial value of ZX output is 0. Different zero-crossing waveforms ZX_OUT are output according to the configuration of ZXD1 and ZXD0: ZXD1=0, indicating that the ZX output changes only at the selected zero-crossing point; ZXD1=1, indicating that the ZX output changes at both positive and negative zero-crossing points.	R/W	0
10	ZXD0	ZXD0=0, indicates that the positive over-zero point is selected as the zero-crossing detection signal; ZXD0=1, indicates that the negative zero crossing point is selected as the zero-crossing detection signal.	R/W	0
9	Energy_clr	=0: All energy registers are cleared after reading; = 1: All energy registers are not cleared after reading.	R/W	0
8	HPFIBOFF	=0: Enables the IB channel digital high-pass filter; = 1: disables the IB channel digital high-pass filter.	R/W	0
7	HPFIAOFF	=0: Enables the IA channel digital high-pass filter; = 1: disables the IA channel digital high-pass filter.	R/W	0
6	HPFUOFF	=0: Enables the U-channel digital high-pass filter; = 1: disables the U-channel digital high-pass filter.	R/W	0
5	CFSUEN	CFSUEN is the control bit of PF/QF pulse output acceleration module. = 0, the pulse acceleration module is turned off and the pulse is output normally; = 1, enable the pulse acceleration module, the output rate of the pulse is increased by a factor of 2^(CFSU[1: 0] + 1). (Note the negative power when verifying)	R/W	0
4: 3	CFSU	This bit is used in conjunction with CFSUEN, see CFSUEN description.	R/W	0
2	SRUN	= 1, enables SF pulse output and apparent energy register totalization; = 0, disables SF pulse output and apparent energy register accumulation. The default state is 1.	R/W	1
1	QRUN	= 1, enable QF pulse output and reactive energy register totalization; = 0, disables QF pulse output and reactive energy register	R/W	1

		accumulation. The default state is 1.		
0	PRUN	= 1, enable PF pulse output and active energy register totalization; = 0, disables PF pulse output and active energy register accumulation. The default state is 1. Configure PRUN/QRUN/SRUN/PBRUN/QBRUN/ SBRUN to 1 and initiate a read operation to any of the metering registers or a write operation to registers PQSRUN.bit4~bit23 for metering to actually turn on; if only a write 1 is done to PRUN/QRUN/SRUN/PBRUN/QBRUN/SBRUN , then metering will not start. This allows multiple integrators to be able to integrate at the same time, ensures integration consistency across multiple sets of integrators, and also allows for software backward compatibility, as the MCU will definitely initiate a read operation after the configuration is complete.	R/W	1

5.3.1.2 Metering control register EMUCON2(0x4)

Metering control register EMUCON2

Offset address: 04H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset value
31: 24	--	Read only	R	0
23: 21	SADD[2: 0]	Channel A apparent energy channel power input selects SADD[2: 0]: = 000, S = SA or SB as determined by CHNSEL; = 001, S = SB; = 010, S = QB; = 011, S = custom power; = 100, S = + SA + SB; =101, S=+SA-SB; =110, S=-SA+SB; = 111, S=-SA-SB.	R/W	0
20: 18	QADD[2: 0]	Channel A reactive energy channel power input selection QADD[2: 0]: = 000, Q = QA or QB, as determined by CHNSEL; = 001, Q = PA; = 010, Q = PB; = 011, Q = |QA| + |QB|; = 100, Q = +QA + QB; =101, Q=+QA-QB;	R/W	0

		=110, Q=-QA+QB; =111, Q=-QA-QB.		
17: 15	PADD[2: 0]	Channel A Active Energy Channel Power Input Selection PADD[2: 0]: = 000, P = PA or PB, as determined by CHNSEL; = 001, P = PA; = 010, P = PB; = 011, P = |PA| + |PB|; = 100, P = + PA + PB; = 101, P = +PA-PB; = 110, P = -PA + PB; = 111, P = -PA-PB.	R/W	0
14: 13	CF2_CFG[1: 0]	Used in conjunction with cf2_cfg2 to determine the selection of the electrical energy pulse output for the P51/QF pin [cf2_cfg2, cf2_cfg]: = 000, original QF pin = QFA; = 001, original QF pin = QFB; = 010, original QF pin = SFA; = 011, original QF pin = SFB; = 100, original QF pin = PFA; = 101, original QF pin = PFB.	R/W	0
12: 11	CF1_CFG[1: 0]	Used in conjunction with cf1_cfg2 to determine the electrical energy pulse output selection for the P50/PF pin, [cf1_cfg2, cf1_cfg]: = 000, original PF pin = PFA; = 001, original PF pin = PFB; = 010, original PF pin = QFA; = 011, original PF pin = QFB; = 100, original PF pin = SFA; = 101, original PF pin = SFB. Remarks: PFA/QFASFA corresponds to energy register EnergyPA/ EnergyQA/ EnergySA respectively; PFB/QFB/SFB corresponds to energy register EnergyPB/ EnergyQB/ EnergySB respectively.	R/W	0
10: 3	usag_cfg[7: 0]	usag_cfg[7: 0] is used to configure the number of half-cycles for voltage dip detection.	R/W	0
2	u_dc_en	u_dc_en, ib_dc_en, ia_dc_en Write 1 enables channel DC Offset1 measurement, which is automatically cleared after the measurement is completed. DC Offset calculation modes are different and realize different functions, see DC Offset	R/W	0
1	ib_dc_en		R/W	0
0	ia_dc_en		R/W	0

		correction related description for detailed function description.		

5.3.1.3 Metering control register EMUCON3(0x74new)

Metering control register EMUCON3

Offset address: 74H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset value
31:18	--	Read only	R	0
17	AUTO_DC_MODE	AUTO DC mode control register: = 0, auto mode, after the metering is completed, the metered value is automatically written to the metering channel DC Offset calibration register 0x38~0x40, the default works for both metering channel and simultaneous sampling channel, and can be individually configured so that it does not work for metering channel and simultaneous sampling channel. =1, manual mode, after the metering is completed, the metered value is only written to DC Offset metering value parameter register 0x258~0x260, the software fills in the DC Offset calibration register after the software judges the reliability of the DC Offset metering value. The normalized DC Offset is calculated as RegValue/2^23.	R/W	0
16	Bypass_EMU_DCOS_EN	Bypass DC Offset calibration enable bit: =0: Not enabled, DC Offset calibration is active, i.e. the value of the UDCOS/IADCOS/IBDCOS registers affects the metering channel; =1: Enable, DC Offset calibration is invalid, i.e., UDCOS/IADCOS/IBDCOS register's do not affect the metering channel.	R/W	0
15:14	--	Read only, not write.	R	0
13	ZX_CFG	Outputs zero-crossing interrupts with different update cycles according to the configuration UZX/IAZX/IBZX of ZX_CFG and EMUCON.ZXD0: = 1, indicating that the zero-crossing interrupt is output only at the zero-crossing point selected by ZXD0; = 0, indicating that zero crossing interrupts are output at both positive and negative zero crossing points.	R/W	0

12	ZX_WAVE_SEL	Waveform data source for zero-crossing detection of UZX/IAZX/IBZX: = 0, selected as metered sampling channel waveform data SPL_U/SPL_IA/SPL_IB; = 1, selected as fundamental-wave data SPL_FU/SPL_FIA/SPL_FIB.		
11	rmshw_zx_sel	Half-cycle RMS zero-crossing source selection. = 0, base wave zero-crossing, default; = 1, full wave zero-crossing.	R/W	0
10	Lpf_10Hz_en	10Hz low-pass filter enable configuration bit: = 0, not enabled; = 1, enable, DC metering use, at this time the base wave filter is replaced with a low-pass filter with a bandwidth of 10 Hz, and you need to configure FGain_CalcAutoDis=1.	R/W	0
9	FGain_CalcAutoDis	= 0, enable the base wave channel automatic gain calibration function, at this time, the base wave channel gain calibration register can be written, but the written value does not work; = 1, in addition to enabling the automatic gain calibration function of the base wave channel, the software fills in the gain calibration value of the base wave channel.	R/W	0
8	FreqCnt	FreqCnt determines the frequency register update period: = 0, frequency update period 32 week waves, backward compatible; = 1, frequency update period 1 week wave.	R/W	0
4: 3	QB_MOD	B channel reactive 1 accumulation mode selection, valid only when PQMOD_ABINDEP=1: = 00, Algebra and Accumulation; =01, positive cumulative; = 10, absolute value cumulative; = 11, reverse cumulative.	R/W	00
7: 5	--	Read only, not write.	R	0
2: 1	PB_MOD	B-way active 1 accumulation mode selection, valid only when PQMOD_ABINDEP=1: = 00, Algebra and Accumulation; =01, positive cumulative; = 10, absolute value cumulative; = 11, reverse cumulative.	R/W	00
0	PQMOD_ABINDEP	Enable bits are independently configured for active 1 and reactive 1 accumulation methods for A and B circuits:	R/W	0

		= 0, not enabled, EMUCON.PMOD/QMOD control 2-way active 1/reactive 1 accumulation mode; =1, enable, EMUCON.PMOD/QMOD control A channel active1/reactive1 accumulation mode, EMUCON3.PB_MOD/QB_MOD control B channel active1/reactive1 accumulation mode.		

5.3.1.4 Metering control register EMUCON4 (0x78new)

Metering control register EMUCON4

Offset address: 78H; Word length: 3 bytes; Default value: 0xF5F5

Bit	Name	Description	R/W	Reset value
31: 16	--	Read only	R	0
15: 14	QB3_MOD	B-channel reactive energy 3 accumulation mode selection: see EPA1_MOD for function description.	R/W	11
13: 12	PB3_MOD	B-channel active energy 3 accumulation mode selection: see EPA1_MOD for function description.	R/W	11
11: 10	QB2_MOD	B-channel reactive energy 2 accumulation mode selection: see PA2_MOD for function description.	R/W	01
9: 8	PB2_MOD	B-channel active energy 2 accumulation mode selection: see PA2_MOD for function description.	R/W	01
7: 6	QA3_MOD	A-way reactive energy 3 accumulation mode selection: see PA2_MOD for function description.	R/W	11
5: 4	PA3_MOD	A-way active energy 3 accumulation mode selection: see PA2_MOD for function description.	R/W	11
3: 2	QA2_MOD	A-way reactive energy 2 accumulation mode selection: see PA2_MOD for function description.	R/W	01
1: 0	PA2_MOD	A-way active energy 2 accumulation mode selection: = 00, Algebra and Accumulation; =01, positive cumulative; = 10, absolute value cumulative; =11, negative cumulative.	R/W	01

5.3.1.5 Metering control register EMUCON5 (0x7C new)

Metering control register EMUCON5, is mainly used for fundamental-wave accumulation method configuration.

Offset address: 7CH; Word length: 3 bytes; Default value: 0xD34

Bit	Name	Description	R/W	Reset value
31: 12	--	Read only	R	0
11: 10	FPB3_MOD	Fundamental-wave B channel active 3 accumulation mode selection, see FPA1_MOD for function description.	R/W	11
9: 8	FPB2_MOD	Fundamental-wave B channel active 1 accumulation mode selection, see	R/W	01

		FPA1_MOD for function description.		
7: 6	FPB1_MOD	Fundamental-wave B channel active 1 accumulation mode selection, see FPA0_MOD for function description.	R/W	00
5: 4	FPA3_MOD	Fundamental-wave A channel active 2 accumulation mode selection, see FPA1_MOD for function description.	R/W	11
3: 2	FPA2_MOD	Fundamental-wave A channel active 1 accumulation mode selection, see FPA1_MOD for function description.	R/W	01
1: 0	FPA1_MOD	Fundamental-wave A channel active 1 accumulation method selection: = 00, Algebra and Accumulation; =01, positive accumulation; = 10, absolute value accumulation; = 11, negative accumulation.	R/W	00

5.3.1.6 Energy Accumulation Enable Register PQSRUN (0x318 new)

Offset address: 318H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset value
31: 24	--	Read only	R	0
23	FPB3_AutoCalc	The B B channelase wave active energy 3 automatic output control bit, see FPA1_AutoCalc for a description, uses the D2FP5 unit.	R/W	0
22	FPB2_AutoCalc	B B channelase wave active energy 2 automatic output control bit, see FPA1_AutoCalc for description, uses D2FP4 unit.	R/W	0
21	FPB1_AutoCalc	The B B channelase wave active energy 1 automatic output control bit, see FPA0_AutoCalc for description, uses the D2FP3 unit.	R/W	0
20	FPA3_AutoCalc	The A channel fundamental-wave active energy 3 automatic output control bit, see FPA1_AutoCalc for a description, uses the D2FP2 unit.	R/W	0
19	FPA2_AutoCalc	The A channel fundamental-wave active energy 2 automatic output control bit, see FPA1_AutoCalc for description, uses the D2FP1 unit.	R/W	0
18	FPA1_AutoCalc	A Channel Fundamental-wave Active Power 1	R/W	0

		Automatic Output Control Bit: =0, disable; =1, enable, the hardware can automatically read the 32bit SPL_FPB register value to fill the 32bit D2FP0 register for integration and output power and pulse. Note: D2FP0 does not support manual writing by software in this mode.		
17	SBRUN	B channel apparent power accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
16	SARUN	A channel apparent power accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
15	QBRUN3	B channel reactive energy 3 Accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
14	QBRUN2	B channel reactive energy 2 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
13	QBRUN	B channel reactive energy 1 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
12	QARUN3	A channel reactive energy 3 Accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
11	QARUN2	A channel reactive energy 2 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
10	QARUN	A channel reactive energy 1 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
9	PBRUN3	B channel active energy 3 Accumulation enable bit: = 0, disable; = 1, enable.	R/W	0

8	PBRUN2	B channel reactive energy 2 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
7	PBRUN	B channel active energy 1 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
6	PARUN3	A channel active power 3 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
5	PARUN2	A-A channel ctive power 2 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
4	PARUN	A channel active energy 1 accumulation enable bit: = 0, disable; = 1, enable.	R/W	0
3: 1	--	read-only, not write-only (ROW)	R	0
0	RUN_SEL	Set to 1 A and B active/reactive/apparent power accumulation enable bit selection: = 0, backwards compatible by default, controlled using the EMUCON register; = 1, controlled using the PQSRUN register.		

5.3.1.7 Pulse output configuration registerCF_CFG(0x80new)

Pulse output configuration register CF_CFG

Offset address: 80H; Word length: 3 bytes; Default value: 0x10543

Bit	Name	Description	R/W	Reset value
31: 20	--	Read only.	R	0
19: 16	CF_OUT4_CFG	Pulse type selection register for CF_OUT4 output: Configuration options are the same as CF_OUT0_CFG, default output PFA pulse.	R/W	0001
15: 12	CF_OUT3_CFG	Pulse type selection register for CF_OUT3 output: Configuration options are the same as CF_OUT0_CFG, default output PFA pulse.	R/W	0000
11: 8	CF_OUT2_CFG	Pulse type selection register for CF_OUT2 output: Configuration options are the same as CF_OUT0_CFG, default output SFB pulse.	R/W	0101

7: 4	CF_OUT1_CFG	Pulse type selection register for CF_OUT1 output: Configuration options are the same as CF_OUT0_CFG, default output QFB pulse.	R/W	0100
3: 0	CF_OUT0_CFG	Pulse type selection register for CF_OUT0 output: =0000, PFA pulse; = 0001, QFA pulse; = 0010, SFA pulse; = 0011, PFB pulse; = 0100, QFB pulse; =0101, SFB pulse; =0110, PFA2 pulse; = 0111, QFA2 pulse; = 1000, PFA3 pulse; = 1001, QFA3 pulse; = 1010, PFB2 pulse; = 1011, QFB2 pulse; = 1100, PFB3 pulse; = 1101, QFB3 pulse; = Other, reserved.	R/W	0011

5.3.1.8 Half-cycle RMS configuration register HWRMS_CFG (0x84 new)

Half-cycle RMS configuration register HWRMS_CFG

Offset address: 84H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	reserved	Read-only	R	0
14:13	HW_RMS_SEL	=00: Select the source of the 3-channel RMS data calculation for the half-cycle update as the ADC sampling channel waveform data SPL_U/SPL_IA/SPL_IB; =01: Select the source of 3-channel RMS data calculation for half-cycle update as ADC sampling channel waveform data SPL_U2/SPL_IA2/SPL_IB2; =10: Select the source of the 3-channel RMS data calculation for the half-cycle update as the fundamental waveform data; = 11: Reserved.	R/W	0
12	HW_RMS_MODE	=0: 3 RMSs are averaged and squared according to the fixed number of sampling points configured in HW_RMS_NUM; = 1: The 3 RMSs are summed and averaged and squared using a zero crossing drive.	R/W	0

11:9	reserved	Read-only	R	0
8:0	HW_RMS_NUM	RMS cumulative averaging calculation for half-cycle updates: = 9'b0, calculated by averaging 72 points cumulatively over a half-circle wave; = 9'b1, calculated by averaging 1-point accumulations over half-cycles; = 9'b1x, calculated by averaging the 2-point cumulative half-cycle; = 9'b1xx, calculated by averaging the 4-point cumulative half-cycle; = 9'b1xxx, calculated by averaging the 8-point cumulative half-cycle; = 9'b1xxxx, calculated by averaging the 16-point cumulative half-cycle; = 9'b1xxxxx, calculated by averaging 32 points cumulatively over a half-cycle; = 0x40~0x1FF, if the desired number of half-cycle cumulative averaging points is N, then NUM = N, and the software determines the number of half-cycle wave sampling points N.	RW	9'b0

5.3.1.9 Half-cycle active configuration register HWP_CFG (0x88 new)

Half-cycle active configuration register HWP_CFG

Offset address: 88H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:14	reserved	Read-only	R	0
13	P_D2F_SEL	=0: The source of calculation of active power and electrical energy for the ADC sampling channel is instantaneous power with an update rate of 7.2 KHz; = 1: ADC sampling A channel active power and electrical energy is calculated from a source of power updated at half-cycle with a typical update rate of 100 Hz.	R/W	0
12	HW_P_MODE	=0: The active power of the 2 ADC sampling channels with half-cycle updates is averaged by accumulating a fixed number of sampling points; = 1: Half-cycle updated 2-A channel DC sampling A channel active power is summed and averaged using an zero-crossing drive.	R/W	0
11:9	reserved	Read-only	R	0

8:0	HW_P_NUM	ADC sampling A channel active power accumulation averaging calculation for half-cycle updating: = 9'b0, calculated by averaging 72 points cumulatively over a half-circle wave; = 9'b1, calculated by averaging 1-point accumulations over half-cycles; = 9'b1x, calculated by averaging the 2-point cumulative half-cycle; = 9'b1xx, calculated by averaging the 4-point cumulative half-cycle; = 9'b1xxx, calculated by averaging the 8-point cumulative half-cycle; = 9'b1xxxx, calculated by averaging the 16-point cumulative half-cycle; = 9'b1xxxxx, calculated by averaging 32 points cumulatively over a half-cycle; = 0x40~0x1FF, if the desired number of half-cycle cumulative averaging points is N, then NUM = N, and the software determines the number of half-cycle wave sampling points N.	R/W	9'b0

5.3.1.10 Half-cycle fundamental active power configuration register HWFP_CFG (0x8C new)

Half-cycle fundamental active configuration register HWFP_CFG

Offset address: 8CH; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:13	reserved	Read-only	R	0
12	HW_FP_MODE	=0: The 2-channel fundamental-wave active power updated in half-cycle is averaged by accumulating a fixed number of sampling points; = 1: The 2-channel fundamental-wave active power updated at half-cycle is summed and averaged using an zero-crossing drive.	R/W	0
11:9	reserved	Read-only	R	0
8:0	HW_FP_NUM	Fundamental-wave active power accumulation averaging calculation for half-cycle updating: = 9'b0, calculated by averaging 72 points cumulatively over a half-circle wave; = 9'b1, calculated by averaging 1-point accumulations over half-cycles; = 9'b1x, calculated by averaging the 2-point cumulative half-cycle;	R/W	9'b0

		= 9'b1xx, calculated by averaging the 4-point cumulative half-cycle; = 9'b1xxx, calculated by averaging the 8-point cumulative half-cycle; = 9'b1xxxx, calculated by averaging the 16-point cumulative half-cycle; = 9'b1xxxxx, calculated by averaging 32 points cumulatively over a half-cycle; = 0x40~0x1FF, if the desired number of half-cycle cumulative averaging points is N, then NUM = N, and the software determines the number of half-cycle wave sampling points N.		

5.3.1.11 Half-cycle reactive power configuration register HWQ_CFG (0x90 new)

Half-cycle reactive power configuration register HWQ_CFG

Offset address: 90H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	reserved	Read-only	R	0
14	Q_SEL	=0: Reactive power of A and B channels is ADC sampling channel reactive power; = 1: The reactive power of channel A and B is fundamental wave reactive power.		
13	Q_D2F_SEL	=0: The source of calculation of reactive power and electrical energy is instantaneous power with an update rate of 7.2 KHz; = 1: The source of calculation of reactive and electric power is the power updated at half-cycle with a typical update rate of 100 Hz.	R/W	0
12	HW_Q_MODE	=0: The 2 reactive powers updated in half-cycle are averaged using a fixed number of sampling points for accumulation; = 1: The 2 reactive powers of the half-cycle update are summed and averaged using an zero-crossing drive.	R/W	0
11:9	reserved	Read-only	R	0
8:0	HW_Q_NUM	Reactive power accumulation averaging calculation for half-cycle updating: = 9'b0, calculated by averaging 72 points cumulatively over a half-circle wave; = 9'b1, calculated by averaging 1-point accumulations over half-cycles; = 9'b1x, calculated by averaging the 2-point cu	R/W	9'b0

		mulative half-cycle; = 9'b1xx, calculated by averaging the 4-point c umulative half-cycle; = 9'b1xxx, calculated by averaging the 8-point cumulative half-cycle; = 9'b1xxxx, calculated by averaging the 16-poi nt cumulative half-cycle; = 9'b1xxxxx, calculated by averaging 32 points cumulatively over a half-cycle; = 0x40~0x1FF, if the desired number of half-c ycle cumulative averaging points is N, then N UM = N, and the software determines the nu mber of half-cycle wave sampling points N.		

5.3.1.12 Pulse frequency register HFConst(0x8)

Pulse frequency register **HFConst**

Offset address: 08H; Word length: 2 bytes; Default value: 0x1000

Bit	Name	Description	R/W	reset value
31:16	---	reserved	R	0
15:0	HFConst	HFConst is a 16-bit unsigned number. When two times the absolute value of the count value of FCntx in the Fast Pulse Counter Register is greater than or equal to HFConst, i.e., 2*|FCntx|≥HFConst, there will be an overflow of pulses accordingly, and the value of the Energy Register will be increased by 1 accordingly. HFConst corresponds to the fast pulse register (active, reactive, apparent).	R/W	1000

5.3.1.13 Pulse frequency register HFConst2 (0x94 new)

Pulse frequency register **HFConst2**

Offset address: 94H; Word length: 2 bytes; Default value: 0x1000

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	HFConst2	HFConst2 is a 16-bit unsigned number. When two times the absolute value of the count value of FCntx in the Fast Pulse Counter Register is greater than or equal to HFConst, i.e., 2*|FCntx|≥HFConst, there will be a pulse overflow accordingly, and the value of the Energy Register will be increased by 1 accordingly. HFConst2 corresponds to fast pulse register 2 (active 2, reactive 2);	R/W	1000

5.3.1.14 Pulse frequency register HFConst3 (0x98 new)

Pulse frequency register **HFConst3**

Offset address: 98H; Word length: 2 bytes; Default value: 0x1000

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	HFConst3	HFConst3 is a 16-bit unsigned number. When two times the absolute value of the count value of FCntx in the Fast Pulse Counter Register is greater than or equal to HFConst, i.e., 2*|FCntx|≥HFConst, there will be an overflow of pulses accordingly, and the value of the Energy Register will be increased by 1 accordingly. HFConst3 corresponds to fast pulse register 3 (active 3, reactive 3);	R/W	1000

5.3.1.15 ADC input reverse enable register ADCNEG_EN (0x9C new)

ADC input reverse enable register.

Offset address: 9CH; default value: 0x0

Bit	Name	Description	R/W	reset value
31:24	WKEY	Write password register: = 0xEA, lower 24 bits writable; = other values, lower 24 bits are not writable.	WO	0
23:6	--	Read only.	R	
5	U_ADCCLK	U-A channel DC_CLK channel sample edge selection register: = 0, rising edge; = 1, falling edge.	R/W	0
4	IB_ADCCLK	IB A channel DC_CLK Channel Sample Edge Select Register: = 0, rising edge; = 1, falling edge.	R/W	0
3	IA_ADCCLK	IA A channel DC_CLK channel sample edge selection register: = 0, rising edge; = 1, falling edge.	R/W	0
2	U_Neg_EN	U-A channel DC input reverse enable register: = 0, no operation; = 1, reverse.	R/W	0

1	IB_Neg_EN	IB A channel DC input inverse enable register: = 0, no operation; = 1, reverse.	R/W	0
0	IA_Neg_EN	IA A channel DC input reverse enable register: = 0, no operation; = 1, reverse. Remarks: Used in case the ADC input is inverted. If the ADC input is inverted, configuring the ADC input inverted will make the sampled signal sign calibration and offset the error of ADC input inverted.	R/W	0

5.3.1.16 Metering Mode EMUMODE (0xA0 new)

Metering Mode Configuration Register, default value: 0x0

Bit	seat Name	Description	R/W	reset value
31:24	WKEY	Write password register: = 0xEA, lower 24 bits writable; = other values, lower 24 bits are not writable.	WO	0
23:2	--	Read only.	R	0
1	DC_SEL	DC metering data source selection register: = 0, selects the 14.4KHz updated waveform; = 1, selects the 7.2KHz updated waveform.	R/W	0
0	EMUMODE	Metering Mode Configuration Register: = 0, AC metering mode; = 1, DC metering mode.	R/W	0

5.3.1.17 Automatic DC metering mode configuration ATCP_CFG (0xA4 new)

Auto Mode Configuration Register, default value: 0x50

Bit	seat Name	Description	R/W	reset value
31:10	--	Read only.	R	0
9:4	Del_Num	Deletes the point Del_Num when the ADC input signal is switched between positive and reverse sampling: = 0, not deleted; = 1 to 63, delete points 1 to 63. Note: Del_Num ≥ 5 is recommended, and Del_Num sampling points are deleted in both	R/W	5

		positive tangent reverse and reverse tangent positive. For example: configure DC_SEL=0, chop_div=2048, Ave_Num=16, at this time to ensure that Ave_Num is the whole cycle of the chop_div, it is appropriate to configure Del_Num=6. (At this time, each chop_div cycle remaining 4 points to do averaging, every 4 cycles metering sampling channel to update the SPL_Px once, the update speed 225Hz)		
3	--	Read only.	R	0
2:0	Ave_Num	DC Metering Sample A channel verage Points Configuration Register: = 0, not average; = 1, 16-point average; = 2, 32-point average; = 3, 64-point average; = 4, 128-point average; = 5, 256-point average; = 6,512-point average; = 7, 1024-point average.	R/W	0

5.3.1.18 Creeping and startup threshold registers (0x0C/0x10)

Active Creeping and Startup Threshold Register PStart

Offset address: 0CH; Word length: 2 bytes; Default value: 0x0060

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	PStart	Active Creeping and Startup Threshold Registers	R/W	0060

Reactive Creeping and Start Threshold Register QStart

Offset address: 10H; Word length: 2 bytes; Default value: 0x0120

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	QStart	Reactive Creeping and Startup Threshold Registers	R/W	0120

The start thresholds are configurable from the PStart and QStart registers. They are 16-bit unsigned numbers that are compared to the absolute value of the higher 24 bits of PowerP and PowerQ (which are 32-bit signed numbers), respectively, for startup determination.

|PowerP|<PStart when PF does not output pulse.

|PowerQ|<QStart, QF does not output pulse.

When |PowerP|<PStart and |PowerQ|<QStart, SF also does not output pulses.

5.3.1.19 Power gain calibration register (0x14/0x18)

A channel power gain calibration register GPQA

Offset Address: 14H; Word Length: 2 bytes; Default Value: 0x0000

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	GPQA	A-channel power gain calibration registers	R/W	0

B channel power gain calibration register GPQB

Offset address: 18H; Word length: 2 bytes; Default value: 0x0000

Bit	Name	Description	R/W	reset value
31:16	---	reserve	R	0
15:0	GPQB	B-channel power gain calibration registers	R/W	0

The A channel power gain calibration register, GPQA, and the B channel power gain calibration register, GPQB, are in 16-bit binary complement format with the highest bit being the sign bit.

GPQA is used for active/reactive/apparent power calibration of current channel IA and voltage channel. GPQB is used for gain calibration of active/reactive power of current channel IB and voltage channel.

The calibration formula is: P1=P0(1+GPQA)

Q1=Q0(1+GPQA)

S1=S0(1+GPQA)

Where GPQA is the normalized value of the gain calibration register, the calibration range is ±1. So the calibration range of the gain calibration is: for power amplification up to 2 times (*2), and reduction can be reduced to 0 (*0).

5.3.1.20 Channel phase calibration register (0x1C/0x20 modified)

A channel Phase calibration Register PhsA

Offset address: 1CH; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:9	---	reserve	R	0
8:0	PhsA	A channel Phase calibration Register	R/W	0

B channel Phase calibration Register PhsB

Offset address: 20H; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:9	---	reserve	R	0
8:0	PhsB	B channel Phase calibration Register	R/W	0

The phase calibration registers include phase calibration PhsA for the IA and U channels and phase calibration PhsB for the IB and U channels. both registers are signed binary complementary codes, valid from bit0 to bit8, where bit8 is the sign bit.

Phase calibration scale: 1 LSB represents 0.009766° phase calibration at 50Hz

Phase calibration range: ±2.5° at 50Hz

New features in V2:

When the high 8 bits of PhsA[31:24] of PhsA[31:0] (0x30) are written to 0xE5, the significance of all the channel phase calibration registers is changed, the phase calibration scale remains unchanged, and the phase calibration range is improved from ±2.5 º to ±10º .

Specific definitions are given below:

PhsA is the IA and U channel phase calibration, whenever PhsA[31:24] is written to 0xE5, PhsA[8:0] is valid (bit8 is the sign bit) becomes PhsA[9:0] is valid (bit9 is the sign bit), and the low 3-byte bit[23:0] default value remains unchanged and does not affect the checksum.

Operation steps: first write PhsA[31:24] to 0xE5, at this time read PhsA[31:24] register value is 0xA5, which means the expansion is successful; and then write the phase calibration value (e.g., PhsA[31:0]=0xE5000215), and note that it is necessary to split the operation into two times. In the new mode, it should be ensured that the PhsA[31:24] write value is alchannels 0xE5.

PhsB is the IB and U channel phase calibration, PhsA[31:24] has been written to the case of 0xE5, PhsB[8:0] is valid (bit8 is the sign bit) becomes PhsB[10:0] is valid (bit10 is the sign bit), the lower 3 bytes bit[23:0] default value is unchanged, does not affect the checksum.

Operation procedure: first write PhsA[31:24] to 0xE5; then write the phase calibration value (e.g. PhsB[9:0]=0x215), and pay attention to split the operation into two times.

The phase calibration is in two steps, and the combination realizes ±10° calibration:

Phase calibration1 calibration source is 1bit data, 1 LSB at 50Hz represents 0.009766° phase calibration and can be calibrated over ±2.5°;

Phase calibration2 calibration the source to a 14.4 KHz updated waveform with a calibration range of ±7.5°.

5.3.1.21 Reactive power phase calibration register QPhsCal (0x24)

Reactive power Phase Calibration Register QPhsCal

Offset Address: 24H; Word Length: 2 bytes; Default Value: 0x0000

Bit	Name	Description	R/W	reset value
31:16	---	reserved	R	0
15:0	QPhsCal	Reactive Phase Calibration Register	R/W	0

The reactive phase calibration register is used for phase calibration of the U-channel 90° phase Hilbert filter in the reactive power calculation. The reactive phase calibration register is in the form of a hexadecimal binary complement with the highest bit being the sign bit.

Calibration formula: Q2 = Q1-QPhs*P1

Where P1 is the active power, Q1 is the reactive power before calibration and Q2 is the reactive power after calibration.

The same phase calibration register is used for both reactive powers and the calibration is multiplied by the corresponding active power respectively.

5.3.1.22 Power Offset calibration register (0x28 0x2C/0x30 0x34/0xAC 0xB0 new)

offset address	28H	2CH	30H	34H	ACH	B0H
register	APOSA	APOSB	RPOSA	RPOSB	APOSFA	APOSFB
default value	0	0	0	0	0	0

Power Offset calibration is suitable for accuracy calibration of small signals.

Power Offset calibration registers are divided into three categories: active power OFFSET calibration registers, reactive power OFFSET calibration registers, and fundamental-wave active power OFFSET calibration registers.

The APOSA register is the active power Offset calibration value of the A channel; the APOSB register is the active power Offset calibration value of the B channel.

The RPOSA register is the reactive power Offset calibration value of the A channel; the RPOSB register is the reactive power Offset calibration value of the B channel.

The APOSFA register is the fundamental-wave active power Offset calibration value for the A channel; the APOSFB register is the fundamental-wave active power Offset calibration value for the B channel.

The registers are all in 16-bit binary complement format, with the highest bit being the sign bit.

Calibration formula:

As an example, assuming that PA is A channel the active power before calibration and PA' is active power after calibration, there is:

PA'=PA+ PA_OS.

5.3.1.23 RMS Offset calibration Register (0x38~40/0xB4~BC new)

offset address	38H	3CH	40H	B4H	B8H	BCH
register	IARMSOS	IBRMSOS	URMSOS	IAHWRMSOS	IBHWRMSOS	UHWRMSOS
default value	0	0	0	0	0	0

The RMS Offset calibration Register is used for RMS small signal accuracy calibration.

The IARMSOS register is the current A channel RMS Offset value, the IBRMSOS register is the current B channel RMS Offset value, and the URMSOS register is the voltage channel RMS Offset value.

IAHWRMSOS, IBHWRMSOS, and UHWRMSOS are half-cycle updated RMS Offset calibration registers.

The registers are all in 16-bit binary complement format, with the highest bit being the sign bit.

Calibration formula:

Taking current A channel as an example, assuming that IARMS is the RMS before calibration and IARMS' is the RMS after calibration, there is:

IARMS'=Sqrt(Abs(IARMS^2+IARMS_OS*2^8)).

5.3.1.24 Channel gain calibration register (0x44~4C/0xA8 new)

offset address	44H	48H	4CH	A8H
register	IAGain	IBGain	UGain	FGain
default	0	0	0	0

value				

IAGain, IBGain, and UGain are the IA, IB, and U ADC channel gain calibration registers, respectively, and have impact on RMS, power, and electrical energy.

FGain is the IA, IB, and U fundamental channel gain register, which mainly compensates for 60 Hz applications and have impact on fundamental-wave RMS and fundamental -wave active power.

The channel gain registers are all in 16-bit binary complement format, with the highest bit being a sign bit indicating the range (-1,+1).

If RegGain>=2^{15} , then $Gain=(RegGain-2^{16})/2^{15}$; otherwise $Gain=RegGain/2^{15}$; where RegGain is the channel gain register value.

Taking the IB A channel s an example, assuming the RMS of the B channel current IB before calibration and IB' after calibration, the relationship is: $IB'=IB+IB*Gain$

Note the effective range of the formula: it is guaranteed that the signal remains within the full scale range of the ADC after multiplying by the channel gain.

The fundamental-wave channel gain calibration function can be configured register EMUCON3.FGain_CalcAutoDis to select automatic calibration or software manual calibration:

EMUCON3.FGain_CalcAutoDis=0 to enable the fundamental-wave A channel auto gain calibration function, at this time the fundamental-wave channel gain calibration register is not writable;

EMUCON3.FGain_CalcAutoDis=1, to de-energize the automatic gain calibration function of the fundamental channel, the user software calculates the fundamental channel gain calibration value by itself and fills in the fundamental-wave channel gain calibration register.

Note: The 0x9C register is not involved in the checksum calculation and is managed by the user's software.

5.3.1.25 Channel DC Offset calibration Register (0x50~58 /0x258~260 new)

offset address	50H	54H	58H
register	IADCOS	IBDCOS	UDCOS
default value	0	0	0

The channel DC Offset calibration and parameter registers are 24bit signed numbers with the highest bit is a signed bit.

Supports DC Offset calibration (0x50~0x58) for three channels for applications that do not require a high-pass filter or need to improve small-signal accuracy or Rogowski Current Coil.

offset address	258H	25CH	260H
register	IADCOS_Calc	IBDCOS_Calc	ICDCOS_Calc
default value	0	0	0

IADCOS_Calc, IBDCOS_Calc, and UDCOS_Calc are read-only AUTO DC DC Offset measurement value registers.

5.3.1.26 Voltage offset register UADD (0x5C)

Voltage B channelias register UADD

Offset address: 5CH; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:24	---	reserve	R	0
23:0	UADD	Voltage B channelias register	R/W	0

Voltage offset register, 24-bit binary complement format, highest bit is the sign bit.

Usage Scenario: The voltage is written to a fixed value for apparent energy metering, which only has an effect on apparent energy. It has no effect on active, reactive and RMSs.

The minimum scale of the UADD is 1.414 times the RMS register.

5.3.1.27 Event threshold register (0x60~6C)

offset address	60H	64H	68H	6CH
register	USAG	IAPEAK	IBPEAK	UPEAK
default value	0	0	0	0

The event threshold registers include: voltage sag threshold register USAG, current A channel peak detection threshold register, current B channel peak detection threshold register, and voltage channel peak detection threshold register.

Voltage sag threshold register, 16-bit unsigned number. The function is not enabled when the value is 0; when a value that is not 0 is written to start the sag detection, the threshold value is compared with the high 16 bits of the 24-bit waveform sampling value of the U-A channel DC, and the number of half-cycles of the detection is determined by EMUCON2.usag_cfg[7:0], EMUCON.Sag_Freq_sel=0, sag is for the period 50Hz application, and the 1 half-cycle time is fixed to 10ms; EMUCON.Sag_Freq_sel=1, sag is for the period 60Hz application, and the 1 half-cycle time is fixed to 10ms; EMUCON. Cycle time is fixed at 10ms; EMUCON.Sag_Freq_sel=1, sag is for cycle 60Hz application, 1 half cycle time is fixed at 8.333ms. when the duration of the sag exceeds usag_cfg, the voltage sag event is triggered, and the detection result is reported with an interrupt.

Peak detection threshold register, 16-bit unsigned number. The function is not enabled when the value is 0; when a value other than 0 is written to start the drop detection, the threshold value is compared with the high 16 bits of the 24-bit waveform sampling value of the ADC, and when the waveform sampling value is detected to be larger than the threshold value, the overload event is triggered, and the result of the detection is reported with an interrupt.

5.3.1.28 Custom power register D2FP (0x70)

Custom Power Register D2FP

Offset address: 70H; Word length: 4 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:0	D2FP	Customized power registers	R/W	0

D2FP is a 32bit signed number with the highest bit being the sign bit.

When EMUCON2.SADD=011, the power value is written to this register, and the power can be calculated by integrating the written power value through the apparent energy channel.

5.3.1.29 Zero-crossing configuration and flag register ZXOTCFG (0x300 new)

Zero-crossing configuration and flag register ZXOTCFG

Offset address: 300H; Word length: 2 bytes; Default value: 0x1C

Bit	Name	Description	R/W	reset value
31:5	reserved	reserved	R	0
4:2	ZXFLAG	Read-only bit that holds the threshold comparison flags for each channel. ZXOTCFG=0,Flag is 1, no comparison of RMS with zero-crossing threshold; ZXOTCFG=1, ZXFLAG indicates the result of comparing the RMS to the zero-crossing threshold. zxflag=1 indicates that the channel is greater than the zero-crossing calculation threshold; zxflag=0 indicates that it is less than the threshold. ZXFLAG channel order is {IB/IA/UA}.	R	7
1	ZXOT_CFG	ZXIA/ZXIB/ZXU channel zero-crossing output control register: When = 0, the zero-crossing judgment is alchannels performed, and the sign of the waveform of the metering sampling channel is changed, i.e., the zero-crossing signal is generated; When = 1, the threshold comparison result is used to select whether or not to carry out zero-crossing judgment, and an zero-crossing signal is output.	R/W	0
0	ZXOTU_CFG	ZX zero-crossing (including frequency measurement and clamping angle) output control register: = 0, backwards compatible, voltage RMS register URMS < 2^16 (normalized value 7.813mV), does not output zero-crossing ZX_OUT, does not generate ZX zero-crossing interrupt, does not measure frequency, does not calculate phase angle. = 1, the result of comparing threshold ZXOTU and voltage RMS URMS is used to select whether the current channel outputs the zero-crossing signal or not.	R/W	0

Note: This register is not involved in the checksum calculation and is managed by the user's software.

5.3.1.30 Zero-crossing threshold register ZXOT (0x304/0x308 new)

Zero-crossing threshold register ZXOTI

Offset Address: 304H; Word Length: 2 bytes; Default Value: 34

Bit	Name	Description	R/W	reset value

15:0	ZXOTI	Current channels (including 2) zero-crossing threshold registers	R/W	34

Zero-crossing threshold register ZXOTU

Offset address: 308H; Word length: 2 bytes; Default value: 0x2D0

Bit	Name	Description	R/W	reset value
15:0	ZXOTU	Voltage channel zero crossing and frequency measurement threshold registers	R/W	0x2D0

For details of the function, see the Function Description section Zero-crossing Detection.

5.3.1.31 Rogowski Current Coil control register ROS_CTRL (0x30C new)

Rogowski Current Coil control register ROS_CTRL

Offset Address: 30CH; Word Length: 2 bytes; Default Value: 0

Bit	Name	Description	R/W	reset value
31:2	--	Read-only	R	0
1	RosIB_EN	= 0, disables IB channel Rogowski Current Coil integration; = 1, enables IB channel Rogowski Current Coil integration.	R/W	0
0	RosIA_EN	= 0, disables IA channel Rogowski Current Coil integration; = 1, enables IA channel Rogowski Current Coil integration.	R/W	0

5.3.1.32 Rogowski Current Coil integral DC attenuation coefficient register ROS_DCATTC (0x310 new)

Rogowski Current Coil Integral DC Attenuation Coefficient Register ROS_DCATTC

Offset address: D0H; Word length: 2 bytes; Default value: 0x7FDF

Bit	Name	Description	R/W	reset value
15:0	Ros_DCATTC	Current Channel Rogowski Current Coil Integral DC Attenuation Coefficient Registers	R/W	7FDF

This register is only valid with Rogowski Current Coil Integral Enable.

5.3.1.33 Rogowski Current Coil Integral Conversion Factor Register ROS_TRANK (0x314 new)

Rogowski Current Coil Integral Conversion Factor Register ROS_TRANK

Offset Address: 314H; Word Length: 2 bytes; Default Value: 0x2CB

Bit	Name	Description	R/W	reset value
15:0	tran_k	This register is only valid in the case of Rogowski Current Coil Integration Enable. The customer fills this register according to the formula	R/W	2CB

		software when applying, this register does not participate in the checksum and is managed by the user software. Calculation formula: trans_k = 2*pi*freq/14400 (freq is the fundamental frequency in Hz) Default values freq=50 and trans_k=0x2CB.		

5.3.1.34 ECT to metering effective enable register ECT_EN (0x330)

Bit	Name	Description	R/W	reset value
31:0	ECT_EN_PS	ECT_EN_PS[7:0]=0x33 or ECT_EN_PS[15:8]=0x5A or ECT_EN_PS[23:16]=0x71 or ECT_EN_PS[31:24]=0xD9 Any one byte is satisfied and the ECT_GAIN value works for the measurement. Full configuration recommended,	R/W	0

5.3.1.35 ECT gain register ECT_GAIN(0x334~0x33C)

334H	338H	33CH
ECT_IAGAIN	ECT_IBGAIN	ECT_UGAIN

is in 16-bit binary complement format, with the highest bit is the sign bit.

The calibration formula is: IA'=IA(1+ECT_IAGAIN)

IB'=IB(1+ECT_IBGAIN)

U'=U(1+ECT_UGAIN)

5.3.2 Metering Parameter Register

5.3.2.1 Fast Pulse Counter Register (0xC0~C8/0x100~108/0xE0~FC new)

offset address	C0H	C4H	C8H	E0H	E4H	E8H	ECH
register	PFBCnt	QFBCnt	SFBCnt	PFBCnt2	QFBCnt2	PFBCnt3	QFBCnt3
default value	0	0	0	0	0	0	0

offset address	100H	104H	108H	F0H	F4H	F8H	FCH
register	PFACnt	QFACnt	SFACnt	PFACnt2	QFACnt2	PFACnt3	QFACnt3
default value	0	0	0	0	0	0	0

The 2 new sets of fast pulse counters for active and reactive energy fast pulse registers correspond to the 2 new sets of energy units respectively.

The fast pulse counter registers are all 2-byte signed numbers, readable and writable.

To prevent loss of power when powering down, the MCU reads back and saves the register PFCntx/QFCntx/SFCntx values when powering down, and then the MCU re-writes these values to PFCntx/QFCntx/SFCntx during the next power-up.

When two times the absolute value of the count value of the fast pulse count register PFCntx/QFCntx/SFCntx is greater than or equal to the HFConst times, there will be a pulse overflow accordingly, and the value of the energy register will be new 1 accordingly.

5.3.2.2 Valid value register (0x10C~114/0x200~208 new)

offset address	10CH	110H	114H	200H	204H	208H
register	IARMS	IBRMS	URMS	HW_RMSIA	HW_RMSIB	HW_RMSU
default value	0	0	0	0	0	0

The ADC sampling channel RMS IARMS, IBRMS, and URMS with an update rate of 14.0625 Hz and a stabilization time of about 300 ms.

New half-cycle RMSs HW_RMSIA, HW_RMS_IB, HW_RMSU.

Configure HWRMS_CFG.HW_RMS_SEL to select the source for calculating the half-cycle RMS:

= 0, 3-channel RMS calculated source for full-wave data;

= 1, 3-channel RMS calculation source for fundamental-wave data.

Configure HWRMS_CFG.HW_RMS_MODE to select the half-cycle RMS calculation mode:

= 0, 3-channel RMSs are averaged cumulatively and squared according to the fixed number of sampling points configured in HWRMS_CFG.HW_RMS_NUM;

=1, 3-channel RMSs are summed and averaged and squared using an zero-crossing drive.

The RMS registers are 24-bit signed numbers, with the highest bit 0 indicating valid data and the highest bit 1 reading zero. RMS normalized value = RegValue/2^23.

5.3.2.3 Voltage Frequency Register UFREQ (0x118 modified)

Voltage Frequency Register UFREQ

Offset address: 118H; Word length: 2 bytes; Default value: 0x2400

Offset address	Name	Description	R/W	reset value
15:0	UFreq	Voltage Frequency Register	R	0

The voltage-frequency register primarily measures the fundamental frequency, with a measurement bandwidth of about 250 Hz. the frequency value is a 16-bit unsigned number, and the parameter formatting equation is:

Freq = CLKIN/4/Reg(UFREQ), where CLKIN = 1.8432MHz and Freq units/Hz.

The voltage frequency update period is determined by EMUCON3.FreqCnt:

FreqCnt=0, frequency update period 32 cycles;

FreqCnt=1, frequency update period 1 week wave.

5.3.2.4 Active power register (0x11C~120/0x168~16C/0x174~178/0x20C~210 new)

offset address	11CH	120H	168H	16CH	174H	178H
register	PowerPA	PowerPB	PowerPA2	PowerPB2	SPL_PA	SPL_PB
default value	0	0	0	0	0	0

offset address	20CH	210H
register	HW_FPA	HW_FPB
default value	0	0

Average active power:

Average active power PowerPA, PowerPB, 4 bytes, updated at 1.7578125Hz;

Average active power PowerPA2, PowerPB2, 4 bytes, updated at 14.0625Hz, stabilization time about 300ms;

Modify the full-wave active power:

Configure HWP_CFG.P_D2F_SEL to select the full-wave active power calculation source:

= 0, backward compatible, full-wave active power and power calculation source for instantaneous power, power registers SPL_PA, SPL_PB, 3 bytes, update rate 7.2 KHz;

=1, full-wave active power and power calculation source for half-cycle updated power, power registers SPL_PA, SPL_PB, 4 bytes, typical update rate 100Hz.

Configure HWP_CFG.HW_P_MODE to select the calculation mode for the power of the half-cycle wave update:

= 0, 2-channel full-wave active power is calculated by accumulating and averaging the fixed number of sampling points configured by HWP_CFG.HW_P_NUM;

=1, 2-channel full-wave active power is calculated by summing and averaging using an zero-crossing drive.

Add new fundamental-wave active power HW_FPA, HW_FPB with a typical update rate of 100Hz.

Configure HWFP_CFG.FP_D2F_SEL to select the full-wave active power calculation source:

= 0, fundamental-wave active power and electrical energy calculation source for instantaneous power, HW_FPA, HW_FPB, 4 bytes, update rate 7.2 KHz;

=1, Fundamental-wave active power and power calculation source for half-cycle updated power, HW_FPA, HW_FPB, 4 bytes, typical update rate 100Hz.

Configure HWFP_CFG.HW_FP_MODE to select the calculation mode for the power of the half-cycle wave update:

= 0, 2-channel fundamental-wave active power is calculated by accumulating and averaging the fixed number of sampling points configured by HWP_CFG.HW_FP_NUM;

= 1, 2-channel fundamental-wave active power is calculated by summing and averaging using an zero-crossing drive.

The active power registers are all in binary complement format, where the highest bit is a sign bit and is read-only.

5.3.2.5 Reactive power register (0x124/0x128/0x17C/0x180 modified)

offset address	124H	128H	17CH	180H
register	PowerQA	PowerQB	SPL_QA	SPL_QB
default value	0	0	0	0

On the basis of the original reactive power, new functions such as reactive power type selection and reactive power calculation mode selection are new.

Reactive power type selection function, the original ADC sampling channel full-wave reactive power and the new fundamental-wave reactive power share a common set of channel and registers, only one of the two can be selected when using, configure HWQ_CFG.Q_SEL to select the source of reactive power calculation:

= 0, A and B path reactive power is ADC sampling channel full wave reactive power. Default mode, backward compatible, the input of reactive power calculation channel is the waveform SPL_U, SPL_IA and SPL_IB of the output of ADC sampling channel updated at 7.2 KHz.This mode has some attenuation for harmonics, but the attenuation is not thorough enough, and the error is about 0.8% when testing the 3rd harmonic according to IEC standard.

=1, A and B channel reactive power is fundamental wave reactive power. The input to the reactive power calculation channel is the waveforms SPL_FU, SPL_FIA and SPL_FIB output from the fundamental sampling channel updated at 7.2 KHz.This mode is more thorough for harmonic attenuation, and the error is close to 0 when the 3rd harmonic is tested according to the IEC standard.

Configure HWQ_CFG.Q_D2F_SEL to select the full-wave active power calculation source:

= 0, backward compatible, reactive power and power calculation source is instantaneous power, power registers SPL_QA, SPL_QB, 3 bytes, update rate 7.2KHz;

= 1, reactive power and power calculation source for half-cycle updated power, power registers SPL_QA, SPL_QB, 4 bytes, typical update rate 100Hz.

Configure HWQ_CFG.HW_Q_MODE to select the calculation mode of reactive power for half-cycle wave update:

= 0, 2-channel reactive power is calculated by accumulating and averaging a fixed number of sampling points as configured in EMUCON9.HW_Q_NUM;

= 1, 2-channel reactive power is calculated by summing and averaging using an zero-crossing drive.

Average reactive power PowerQA, PowerQB, 4 bytes, updated at 14.0625 Hz.

The reactive power registers are all in binary complement format, where the highest bit is a sign bit and is read-only.

5.3.2.6 Apparent power register (0x12C/0x130)

offset address	12CH	130H
register	PowerSA	PowerSB
default value	0	0

PowerSA is the A-A channel pparent power and PowerSB is the B-A channel pparent power with an update rate of

14.0625 Hz. the stabilization time is about 300 ms.

The RMS method is used for apparent power, i.e., S=Urms*Irms

The apparent power registers are all in binary-complement format, 32-bit signed numbers, where the highest bit is the sign bit, the apparent power is alchannels positive, and the sign bit is held at 0, read-only.

5.3.2.7 Power registers (0x134~144/0x170/0x238~254 new)

offset address	134H	138H	13CH	140H	144H	170H
register	EnergyPA	EnergyPB	EnergyQA	EnergyQB	EnergySA	EnergySB
default value	0	0	0	0	0	0

offset address	238H	23CH	240H	244H	248H	24CH	250H	254H
register	EnergyPA2	EnergyPB2	EnergyQA2	EnergyQB2	EnergyPA3	EnergyPB3	EnergyQA3	EnergyQB3
default value	0	0	0	0	0	0	0	0

The electrical energy registers are divided into three categories: active energy, reactive energy and apparent energy. Among them, there are three sets of active and reactive energy registers respectively, and two sets are newly new. Each set of energy unit can be independently configured with four types of algebraic sum/positive/absolute/reverse (newly new) electrical energy accumulation methods, independent HFConst control, independent electrical energy accumulation enable control bits, independent pulse and interrupt and overflow interrupt outputs.

Original set to 1 active and reactive using HFConst, new set 2 active and reactive using HFConst2, new set 3 active and reactive using HFConst3.

Configure EMUCON3. PQMOD_ABINDEP to select whether or not to independently configure the A and B A channel ctive1 and reactive1 accumulation methods:

= 0, not enabled, EMUCON.PMOD/QMOD control 2-channel active 1/reactive 1 accumulation mode;

=1, enable, EMUCON.PMOD/QMOD control A channel active1/reactive1 accumulation mode, EMUCON3.PB_MOD/QB_MOD control B channel active1/reactive1 accumulation mode.

Active 2, reactive 2, active 3, reactive 3 power unit accumulation mode and enable control register EMUCON3, sets 2 and 3 are off by default, set 2 defaults to positive accumulation mode and set 3 defaults to reverse accumulation mode.

The energy register type can be configured EMUCON.Energy_clr register is selected to be clear after read or not clear type, the default is clear after read.

The electrical energy parameter is a 24bit unsigned number, read-only, representing the number of accumulations of the corresponding pulse. The energy represented by the smallest unit of the register is 1/EC kWh, where EC is the meter constant.

An overflow flag IF is generated when the energy register overflows from 0xFFFFFF to 0x000000; if the corresponding interrupt is enabled, the corresponding interrupt is generated.

5.3.2.8 Power factor register (0x148/0x14C)

offset address	148H	14CH
register	PFA	PFB
default value	0	0

PfA is the A channel power factor and PfB is the B channel power factor.

The power factor register is in 24bit binary complement format, with the high bit being the sign bit, read-only, normalized/2^23.

The power factor is the RMS power factor, i.e. Pf = P/S.

5.3.2.9 Phase angle register (0x150/0x154)

offset address	150H	154H
register	ANGLEA	ANGLEB
default value	0	0

ANGLEA is the angle between the fundamental-wave current A channel and the fundamental-wave voltage, and ANGLEB is the angle between the fundamental-wave current B channel and the fundamental-wave voltage.

The phase angle register is a 16bit signed number, read-only.

Calculation formula: Angle value = (RegValue/2^15)*360 degrees

5.3.2.10 Waveform Sample Register (0x15C~164/0x214~234 new)

offset address	15CH	160H	164H	214H	218H	21CH
register	SPL_IA	SPL_IB	SPL_U	SPL_IA2	SPL_IB2	SPL_U2
default value	0	0	0	0	0	0

offset address	22CH	230H	234H
register	SPL_FIA	SPL_FIB	SPL_FU
default value	0	0	0

The waveform sampling registers are divided into the following categories:

SPL_IA, SPL_IB, SPL_U, high-pass filtered data, updated at 7.2 KHz, subject to channel phase calibration, DC Offset calibration, ADC channel gain calibration;

SPL_IA2, SPL_IB2, SPL_U2, High-pass pre-filtered data, updated at 14.4 KHz, subject to channel phase calibration, DC Offset calibration1, ADC channel gain calibration;

SPL_FIA, SPL_FIB , SPL_FU are the sampled values of the fundamental current A channel , current B channel and voltage channel waveforms, which are updated at a rate of 7.2KHz, and are affected by the channel phase calibration, DC Offset calibration, channel gain calibration, and fundamental channel gain calibration.

The waveform sample registers are all in binary complement format, 24bit signed numbers, normalized/2^22.

5.3.3 Status and Interrupt Registers

5.3.3.1 Metering status register EMUStatus (0x158)

Metering status register EMUStatus

Offset Address: 158H; Word Length: 4 bytes; Default Value: 0xE3EE78

Bit	Name	Description	R/W	reset value
31	NoSld	NoSld is set to 1 when the apparent power is less than the startup power; NoSLd clears to 0 when the apparent power is greater than/equal to the startup power.	R	0
30	WREN	Write enable flag: =1: Allow writing to write-protected registers; =0: Write to registers with write-protected is not allowed.	R	0
29	CHNSEL	Current channel selection status identification bit: = 0: The current channel used to calculate active/reactive energy is A channel ; = 1: The current channel used to calculate active/reactive energy is currently B channel.	R	0
28	Noqld	Noqld is set to 1 when the reactive power is less than the startup power; NoqLd clears to 0 when the active power is greater than/equal to the startup power.	R	0
27	Nopld	Nopld is set to 1 when the active power is less than the startup power; NopLd clears to 0 when the active power is greater than/equal to the startup power.	R	0
26	REVQA	A channel reverse reactive power indication identification signal: This signal is 1 when negative reactive power is detected; This signal is 0 when positive reactive power is detected again.	R	0
25	REVPA	A channel reverse active power indication marking signal: This signal is 1 when negative power is detected; This signal is 0 when positive active power is detected again.	R	0
24	Chksum1Busy	Calibration table data checksum calculation status register: = 0: Indicates that the checksum calculation of the	R	0

		calibration table data has been completed and the checksum value is available; = 1: Indicates that the checksum calculation of the calibration table data has not been completed and the checksum value is not available.		
23:0	Chksum1	checksum output	R	E3EE78

This register consists of two parts: the metering status register and the checksum register.

EMUStatus [23:0] holds the 24-bit checksum 1 of the calibration table parameter configuration register, which the CPU can detect to monitor whether the calibration table data is misaligned.

General application scenario: read the checksum after the completion of all the calibration tables, the existence of EEPROM as a benchmark, and then the CPU regularly reads the checksum register to do the comparison to monitor whether the calibration table data is messed up or not. The application can naturally avoid the problem of automatic DC_Offset calibration after the completion of the enable bit is automatically cleared and cause the checksum register to change.

The algorithm for the checksum is three-byte accumulation followed by inverse. For a double-byte register, it is expanded to three bytes and then summed, and the expanded byte is 00H.

The checksum calculated from the default value is 0xE3EE78.

A checksum calculation is restarted under the following three conditions: a system reset, a write operation to one of the registers from 00H to 6CH, or a read operation to the EMUStatus register. A checksum calculation requires 32 CPU clocks.

5.3.3.2 Metering Status Register 2 EMUStatus2 (0x188)

Metering status register 2 EMUStatus2

Offset Address: 188H; Word Length: 4 bytes; Default Value: 0

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0
14	SNegS_Flag	ADC input signal reverse sample indication flag: = 0, positive sampling; = 1, negative sampling.	R	0
13	NoSbLd	When the apparent power of B channel is less than the startup power, set to 1; Cleared when the apparent power of channel B is greater than/equal to the startup power.	R	0
12	NoQbLd	Set to 1 when the reactive power of channel B is less than the startup power; Cleared when the reactive power of channel B is greater than/equal to the startup power.	R	0
11	Nopbld	When the active power of channel B is less than the startup power, set to 1; Cleared when the active power of channel B is greater than/equal to the startup power.	R	0
10	REVQB	B channel reactive power negative indication signal:	R	0

		This signal is 1 when negative reactive power is detected; This signal is 0 when positive active power is detected again.		
9	REVPB	B channel active power negative indication signal: This signal is 1 when negative power is detected. This signal is 0 when positive active power is detected again.	R	0
8	Vref_flag	VREF flag bit: = 1: VREF is normal; = 0: VREF is below the drop threshold.	R	0
7	Ldo_flag	Metering LDO flag bit: = 1: Metering LDO is normal; = 0: The metering LDO is below the sag threshold.	R	0
6	NoSald	When the apparent power is less than the startup power, set to 1; Cleared when the apparent power is greater than/equal to the startup power.	R	0
5	WREN	Write enable flag: =1: Allow writing to write-protected registers; =0: Write to registers with write-protected is not allowed.	R	0
4	CHNSEL	Current channel selection status identification bit: = 1: The current channel used to calculate active/reactive energy is currently B channel; = 0: The current channel used to calculate active/reactive energy is currently A channel. This bit is 0 in the default state and identifies the selection of A channel for power metering.	R	0
3	NoQaLd	Set to 1 when the reactive power of channel A is less than the startup power; Cleared when the active power of channel A is greater than/equal to the startup power.	R	0
2	NoPaLd	When the active power of A channel is less than the startup power, set to 1; Cleared when the active power is greater than/equal to the startup power.	R	0
1	REVQA	A channel reverse reactive power indication identification signal: This signal is 1 when negative reactive power is detected; This signal is 0 when positive reactive power is detected again.	R	0
0	REVPA	A channel reverse active power indication marking	R	0

		signal: This signal is 1 when negative power is detected; This signal is 0 when positive active power is detected again.		

5.3.3.3 Metering Status Register 3 EMUStatus3 (0x1AC new)

Metering status register 3 EMUStatus3

Offset Address: 1ACH; Word Length: 3 bytes; Default Value: FD5361

Bit	Name	Description	R/W	reset value
31:25	--	reserved	R	0
24	Chksum2Busy	Calibration table data checksum calculation status register: = 0: Indicates that the checksum calculation of the calibration table data has been completed and the checksum value is available; = 1: Indicates that the checksum calculation of the calibration table data has not been completed and the checksum value is not available.	R	0
23:0	Chksum2	New checksum output for configuration registers	R	FD5460

Chksum2 holds the 24-bit checksum of the calibration table parameter configuration register, which the CPU can detect to monitor whether the calibration table data is misaligned.

Checksum range base address 0x50004000:

0x74~0xA4, 0xAC~0xBC, 0x304~0x310, 0x318 (PQSRUN), 0x400~0x410 (DMA general-purpose waveform buffer), and 0x420~0x42C (RCD-specific waveform buffer).

FGain(0xA8) is not counted in the checksum range because it involves the fundamental-wave auto gain calibration function and the register value is rewritten automatically.

ZXOTCFG(0x300) is not counted in the checksum range because it contains the zero-crossing flag bit.

ROS_Tran_K(0x314) is not counted in the checksum range because it needs to be adjusted in real time according to the voltage frequency.

ECT related registers are not counted in the checksum range.

Intelligent micro breaks and RCD related registers are not counted in the checksum range.

Checksum algorithm: three bytes are summed and inverted, and the high bit of the register is not enough to make up for the zero.

5.3.3.4 Interrupt enable register IE (0x18C modified)

Interrupt Enable Register IE

Offset Address: 18CH; Word Length: 4 bytes; Default Value: 0x0

The IRQ_N pin outputs low when the interrupt allow bit is configured to 1 and an interrupt is generated. Write-protect register, write enable needs to be turned on before configuring this register.

Bit	Name	Description	R/W	reset value

31:24	--	Read only.	R	0
23	IBZXIE	= 0: Disables the IB current channel zero-crossing interrupt; = 1: Enable IB current channel zero-crossing interrupt.	R/W	0
22	IAZXIE	= 0: Disables the IA current channel zero-crossing interrupt; = 1: Enable IA current channel zero-crossing interrupt.	R/W	0
21	UZXIF	= 0: Disables the voltage channel zero-crossing interrupt; = 1: Enable voltage channel zero-crossing interrupt. When the external inputs are the same, the three zero-crossing interrupts IBZX, IAZX, and UZX are in phase.	R/W	0
20	SBEOIE	= 0: Turn off the apparent power register ESB overflow interrupt; =1: Enable apparent power register ESB overflow interrupt.	R/W	0
19	QBEOIE	= 0: Turn off the reactive energy register EQB overflow interrupt; = 1: Enable reactive energy register EQB overflow interrupt.	R/W	0
18	PBEOIE	= 0: Turn off the active power register EPB overflow interrupt; = 1: Enable active power register EPB overflow interrupt.	R/W	0
17	SFBIE	=0: Turn off SFB interrupt; = 1: Turn on the SFB interrupt.	R/W	0
16	QFBIE	=0: Turn off QFB interrupt; = 1: Turn on the QFB interrupt.	R/W	0
15	PFBIE	=0: Turn off PFB interrupt; = 1: Turn on the PFB interrupt.	R/W	0
14	SFAIE	= 0: Turn off SFA interrupt; = 1: Turn on the SFA interrupt.	R/W	0
13	SEOIE	=0: Turn off apparent power register overflow interrupt; =1: Enable apparent power register overflow interrupt.	R/W	0
12	VREFIE	=0: Disable VREF fall interrupt; = 1: Enable VREF sag interrupt.	R/W	0
11	LDOIE	=0: Disable LDO sagout interrupt; = 1: Enable LDO sag interrupt.	R/W	0

10	SPLIE	=0: Turn off the 7.2KHz waveform update interrupt; = 1: Enable 7.2KHz waveform update interrupt.	R/W	0
9	USAGIE	=0: Turn off U-channel sag interrupt; = 1: Enable U channel sag interrupt.	R/W	0
8	UpeakIE	=0: Disable U-channel overload interrupt; = 1: Enable U-channel overload interrupt.	R/W	0
7	IApeakIE	=0: Disable IA channel overload interrupt; = 1: Enable IA channel overload interrupt.	R/W	0
6	IBpeakIE	=0: Disable IB channel overload interrupt; = 1: Enable IB channel overload interrupt.	R/W	0
5	ZXIE	= 0: Turn off the zero-crossing interrupt; = 1: Enable zero crossing interrupt. This zero-crossing signal and the UZX (bit21) zero-crossing both come from the voltage A channel DC, but with a phase delay.	R/W	0
4	QEOIE	=0: Disable reactive energy register overflow interrupt; =1: Enable reactive energy register overflow interrupt.	R/W	0
3	PEOIE	=0: Turn off the active power register overflow interrupt; =1: Enable active power register overflow interrupt.	R/W	0
2	QFAIE	= 0: Turn off QFA interrupt; = 1: Turn on the QFA interrupt.	R/W	0
1	PFAIE	= 0: Disable PFA interrupt; = 1: Turn on the PFA interrupt.	R/W	0
0	DUPDIE	= 0: Turn off data update interrupt; = 1: Enable data update interrupt. Flag is set when a data update occurs in the data PowerPA, PowerPB, PowerQ, IARMS, IBRMS, and URMS registers.	R/W	0

5.3.3.5 Interrupt status register IF (0x190 modified)

Interrupt Status Register IF

Offset Address: 190H; Word Length: 4 bytes; Default Value: 0x0

When an interrupt event is generated, the hardware sets the corresponding interrupt flag to 1.

The generation of the IF interrupt flag is not controlled by the interrupt allow register IE and is determined only by whether an interrupt event has occurred.

Bit	Name	Description	R/W	reset value
31:25	--	Read only.	R	0

24	DUPDIF2	= 0: New metering data update event did not occur; = 1: New metering data update events occur.	R/W	0
23	IBZXIF	= 0: Current B channel zero-crossing event did not occur; = 1: Current B channel zero-crossing event occurs.	R/W	0
22	IAZXIF	= 0: Current A channel zero crossing event did not occur; = 1: Current A channel zero-crossing event occurs.	R/W	0
21	UZXIF	= 0: Voltage channel zero-crossing event did not occur; = 1: Voltage channel zero-crossing event occurs.	R/W	0
20	SBEOIF	= 0: apparent power register ESB overflow event did not occur =1: An apparent power register ESB overflow event occurred.	R/W	0
19	QBEOIF	= 0: The reactive energy register EQB overflow event did not occur; = 1: A reactive energy register EQB overflow event occurs.	R/W	0
18	PBEOIF	= 0: Active power register EPB overflow event did not occur; =1: Active power register EPB overflow event occurred.	R/W	0
17	SFBIF	= 0: No SFB pulse output event occurred; = 1: An SFB pulse output event has occurred.	R/W	0
16	QFBIF	= 0: No QFB pulse output event occurred; = 1: A QFB pulse output event has occurred.	R/W	0
15	PFBIF	= 0: No PFB pulse output event occurred; = 1: A PFB pulse output event has occurred.	R/W	0
14	SFAIF	= 0: No SFA pulse output event occurred; = 1: An SFA pulse output event has occurred.	R/W	0
13	SEAOIF	= 0: No apparent power register ESA overflow event occurred; = 1: An apparent power register ESA overflow event occurred.	R/W	0
12	VREFIF	= 0: VREF sag event did not occur; = 1: VREF sag event occurs.	R/W	0
11	LDOIF	= 0: LDO sag event did not occur; = 1: LDO sag event occurs.	R/W	0
10	SPLIF	=0: 7.2 KHz waveform update event did not occur;	R/W	0

		= 1: 7.2 KHz waveform update event occurs.		
9	USAGIF	= 0: U-channel sag event did not occur; = 1: U-channel sag event occurs.	R/W	0
8	UpeakIF	= 0: U-channel overload event did not occur; = 1: U-channel overload event occurs.	R/W	0
7	IApeakIF	= 0: IA channel overload event did not occur; = 1: IA channel overload event occurs.	R/W	0
6	IBpeakIF	= 0: IB channel overload event did not occur; = 1: IB channel overload event occurs.	R/W	0
5	ZXIF	= 0: The zero-crossing event did not occur; = 1: An zero-crossing event occurs.	R/W	0
4	QEOIF	= 0: The reactive energy register overflow event did not occur; =1: A reactive energy register overflow event has occurred.	R/W	0
3	PEOIF	= 0: Active power register overflow event did not occur; =1: Active power register overflow event occurred.	R/W	0
2	QFAIF	= 0: QFA pulse output event did not occur; = 1: QFA pulse output event occurs.	R/W	0
1	PFAIF	= 0: PFA pulse output event did not occur; = 1: PFA pulse output event occurs.	R/W	0
0	DUPDIF	= 0: Data update event did not occur; = 1: Data update event occurs.	R/W	0

5.3.3.6 Interrupt enable register EMUIE2 (0x1A0 new)

Interrupt Enable Register EMUIE2

Offset Address: 1A0H; Word Length: 3 bytes; Default Value: 0x0

Interruption number 2.

Bit	Name	Description	R/W	reset value
31:16	--	Read only.	R	0
15	QB3EOIE	=0: Turn off reactive energy register EQB3 overflow interrupt; = 1: Enable reactive energy register EQB3 overflow interrupt.	R/W	0
14	PB3EOIE	=0: Turn off the active power register EPB3 overflow interrupt; = 1: Enable active power register EPB3 overflow interrupt.	R/W	0
13	QB2EOIE	= 0: Turn off the reactive energy register EQB2 overflow interrupt;	R/W	0

		= 1: Enable reactive energy register EQB2 overflow interrupt.		
12	PB2EOIE	= 0: Turn off the active power register EPB2 overflow interrupt; = 1: Enable active power register EPB2 overflow interrupt.	R/W	0
11	QA3EOIE	= 0: Turn off reactive energy register EQA3 overflow interrupt; = 1: Enable reactive energy register EQA3 overflow interrupt.	R/W	0
10	PA3EOIE	= 0: Turn off the active power register EPA3 overflow interrupt; = 1: Enable active power register EPA3 overflow interrupt.	R/W	0
9	QA2EOIE	= 0: Turn off the reactive energy register EQA2 overflow interrupt; = 1: Enable reactive energy register EQA2 overflow interrupt.	R/W	0
8	PA2EOIE	= 0: Turn off the active power register EPA2 overflow interrupt; = 1: Enable active power register EPA2 overflow interrupt.	R/W	0
7	QFB3IE	=0: Turn off QFB3 interrupt; = 1: Turn on QFB3 interrupt.	R/W	0
6	PFB3IE	=0: Turn off PFB3 interrupt; = 1: Turn on PFB3 interrupt.	R/W	0
5	QFB2IE	=0: Turn off QFB2 interrupt; = 1: Turn on QFB2 interrupt.	R/W	0
4	PFB2IE	=0: Turn off PFB2 interrupt; = 1: Turn on the PFB2 interrupt.	R/W	0
3	QFA3IE	=0: Turn off QFA3 interrupt; = 1: Turn on QFA3 interrupt.	R/W	0
2	PFA3IE	=0: Turn off the PFA3 interrupt; = 1: Turn on the PFA3 interrupt.	R/W	0
1	QFA2IE	=0: Turn off QFA2 interrupt; = 1: Turn on QFA2 interrupt.	R/W	0
0	PFA2IE	=0: Turn off PFA2 interrupt; = 1: Turn on the PFA2 interrupt.	R/W	0

Write-protect register, write enable needs to be turned on before configuring this register. Interrupt number 2.

5.3.3.7 Interrupt status register EMUIF2 (0x1A4 new)

Interrupt status register EMUIF2

Offset Address: 1A4H; Word Length: 3 bytes; Default Value: 0x0

Bit	Name	Description	R/W	reset value
31:16	--	Read only.	R	0
15	QB3EOIF	= 0: The reactive energy register EQB3 overflow event did not occur; =1: A reactive energy register EQB3 overflow event has occurred.	R/W	0
14	PB3EOIF	= 0: Active power register EPB3 overflow event did not occur; =1: Active power register EPB3 overflow event occurred.	R/W	0
13	QB2EOIF	= 0: The reactive energy register EQB2 overflow event did not occur; =1: A reactive energy register EQB2 overflow event has occurred.	R/W	0
12	PB2EOIF	= 0: Active power register EPB2 overflow event did not occur; =1: Active power register EPB2 overflow event occurred.	R/W	0
11	QB3EOIF	= 0: The reactive energy register EQB3 overflow event did not occur; =1: A reactive energy register EQB3 overflow event has occurred.	R/W	0
10	PA3EOIF	=0: Active power register EPA3 overflow event did not occur; =1: Active power register EPA3 overflow event occurred.	R/W	0
9	QA2EOIF	= 0: The reactive energy register EQA2 overflow event did not occur; =1: A reactive energy register EQA2 overflow event has occurred.	R/W	0
8	PA2EOIF	=0: Active power register EPA2 overflow event did not occur; =1: Active power register EPA2 overflow event occurred.	R/W	0
7	QFB3IF	= 0: No QFB3 pulse output event occurred; = 1: A QFB3 pulse output event has occurred.	R/W	0
6	PFB3IF	= 0: No PFB3 pulse output event occurred; =1: A PFB3 pulse output event has occurred.	R/W	0
5	QFB2IF	= 0: No QFB2 pulse output event occurred; = 1: A QFB2 pulse output event has occurred.	R/W	0
4	PFB2IF	= 0: No PFB2 pulse output event occurred; =1: A PFB2 pulse output event has occurred.	R/W	0
3	QFA3IF	= 0: No QFA3 pulse output event occurred;	R/W	0

		= 1: A QFA3 pulse output event has occurred.		
2	PFA3IF	= 0: No PFA3 pulse output event occurred; =1: A PFA3 pulse output event has occurred.	R/W	0
1	QFA2IF	= 0: No QFA2 pulse output event occurred; = 1: A QFA2 pulse output event has occurred.	R/W	0
0	PFA2IF	= 0: No PFA2 pulse output event occurred; =1: A PFA2 pulse output event has occurred.	R/W	0

5.3.3.8 Interrupt Enable Register EMUIE3 (0x1B0 New)

Interrupt Enable Register EMUIE3

Offset Address: 1B0H; Word Length: 3 bytes; Default Value: 0x0

Interrupt number 0.

Bit	Name	Description	R/W	reset value
31:9	--	Read only.	R	0
8	WAVEHW_IE	=0: Turn off the simultaneous sampling channel half-cycle parameter update interrupt; = 1: Enable simultaneous sampling channel half-cycle parameter update interrupt.	R/W	0
7	DMA_RCD_BUF_ErrIE	=0: Disable waveform buffer DMA RCD channel data error interrupt; =1: Enable waveform buffer DMA RCD channel data error interrupt.	R/W	0
6	DMA_RCD_BUFHF_IE	=0: Turn off the waveform buffer DMA RCD B channelUFFER half-full interrupt; =1: Enable waveform buffer DMA RCD B channelUFFER half-full interrupt.	R/W	0
5	DMA_RCD_BUFF_IE	= 0: Turn off waveform buffer DMA RCD B channelUFFER full interrupt; =1: Enable waveform buffer DMA RCD B channelUFFER full interrupt.	R/W	0
4	DMA_BUFIB_ErrIE	=0: Disable waveform buffer DMA IB channel data error interrupt; =1: Enable waveform buffer DMA IB channel data error interrupt.	R/W	0
3	DMA_BUFIA_ErrIE	=0: Disable waveform buffer DMA IA channel data error interrupt; =1: Enable waveform buffer DMA IA channel data error interrupt.	R/W	0
2	DMA_BUFUErr_IE	=0: Disable waveform buffer DMA U-channel data error interrupt; =1: Enable waveform buffer DMA U-channel data error interrupt.	R/W	0

1	DMA_BUFHF_IE	=0: Turn off the waveform buffer DMA B channelUFFER half-full interrupt; =1: Enable waveform buffer DMA B channelUFFER half-full interrupt.	R/W	0
0	DMA_BUFF_IE	= 0: Turn off the waveform buffer DMA B channelUFFER full interrupt; =1: Enable waveform buffer DMA B channelUFFER full interrupt.	R/W	0

5.3.3.9 Interrupt status register EMUIF3 (0x1B4 new)

Bit	Name	Description	R/W	reset value
31:9	--	Read only.	R	0
8	WAVEHW_IF	= 0: Simultaneous sampling channel half-cycle parameter update event did not occur; = 1: Simultaneous sampling channel half-cycle parameter update event occurs.	R/W	0
7	DMA_RCD_BUF_ErrIF	= 0: Waveform buffer DMA RCD channel data error event did not occur; =1: Waveform Buffer DMA RCD Channel Data Error event occurred.	R/W	0
6	DMA_RCD_BUFHF_IF	=0: Waveform buffer DMA RCD B channelUFFER half-full event did not occur; =1: Waveform Buffer DMA RCD B channelUFFER Half Full event occurred.	R/W	0
5	DMA_RCD_BUFF_IF	=0: Waveform buffer DMA RCD B channelUFFER full event did not occur; =1: Waveform Buffer DMA RCD B channelUFFER Full event occurred.	R/W	0
4	DMA_BUFIB_ErrIF	= 0: Waveform buffer DMA IB channel data error event did not occur; =1: Waveform Buffer DMA IB Channel Data Error event occurred.	R/W	0
3	DMA_BUFIA_ErrIF	= 0: Waveform buffer DMA IA channel data error event did not occur; =1: Waveform Buffer DMA IA Channel Data Error event occurred.	R/W	0
2	DMA_BUFUErr_IF	= 0: Waveform buffer DMA U-channel data error event did not occur; =1: Waveform Buffer DMA U-channel data error event occurred.	R/W	0
1	DMA_BUFHF_IF	=0: Waveform buffer DMA B channelUFFER half full event did not occur;	R/W	0

		=1: Waveform buffer DMA B channelUFFER half full event occurred.		
0	DMA_BUFF_IF	= 0: Waveform buffer DMA B channelUFFER full event did not occur; =1: Waveform buffer DMA B channelUFFER full event occurred.	R/W	0

5.3.4 Simultaneous Sampling Configuration and Parameter Registers (new)

Base address: 0x40040080

5.3.4.1 WAVE_WKEY(0x00 new)

Simultaneous Sample Write Password Register

Offset address: 00H; default value: 0x0

Bit	Name	Description	R/W	reset value
7:0	WKEY	Write 0xE5 to enable synchronous sampling write operation; Write 0xDC to turn off the synchronous sampling write operation.	WO	0

5.3.4.2 WAVECFG (0x04 new)

Simultaneous Sampling Channel Configuration Register

Offset address: 04H; default value: 0x0

Bit	Name	Description	R/W	reset value
31:4	--	Read only.	R	0
3:2	HW_WAVE	Half-cycle RMS and half-cycle power point count configuration registers: = 00, 128-point cumulative averaging; = 01, 64-point cumulative averaging; = 10, 32 points cumulative for averaging; = 11, 256 points cumulative averaging; Note: This number of accumulation points and the number of simultaneous sampling points need to be set independently. Note: The parameters update the interrupt allow bit ENUIE3.bit8 and the interrupt flag bit EMUIF3.bit8.	R/W	0
1	WAVE_AGC_OFF	Channel gain auto-tuning off control bit: = 0, turn on AGC;	R/W	0

		= 1, turn off AGC. Note: The gain automatic adjustment function is to solve the gain change caused by the change of DEC filter extraction multiplier. Turn on the function, the RMS of the NVM A channel nd the amplitude of the waveform obtained from the simultaneous sampling A channel re the same as that of the metering channel.		
0	MODE_SEL	Mode Selection Control Register: = 0, NVM mode; = 1, simultaneous sampling mode.	R/W	0

5.3.4.3 WAVECFG2 (0x08 new)

Simultaneous Sampling Channel Configuration Register 2

Offset address: 08H; default value: 0x0

Bit	Name	Description	R/W	reset value
31:10	--	Read only.	R	0
9:8	WAVE_DIV	The output is given to the crossover frequency of the waveform buffer: = 00, not crossover; =01, 2-channel; =10, 4-channel; =11, 8-channel.	R	0
7:5	WAVE_SR	Simultaneous Sampling Weekly Wave Points Configuration Register: = 000, 256 points of simultaneous sampling; = 001, 128-point simultaneous sampling; = 010, 64-point simultaneous sampling; = 011, 512 points of simultaneous sampling; = 100, 10-week 1024-point simultaneous sampling; = 101, 10-week 2048-point simultaneous sampling; = Other, reserved.	R/W	0
4	Bypass_WAVE_DCOS_EN	Bypass Simultaneous sampling channel DC Offset calibration enable bit: = 0, not enabled, metering channel DC	R/W	0

		Offset calibration is valid for simultaneous sampling channels; = 1, enable, metering channel DC Offset calibration is not valid for simultaneous sampling channels.		
3	WAVE_AAC_OFF	Harmonic attenuation calibration off control bit: = 0, turn on AAC; = 1, turn off AAC. Note: After this function is enabled, it is no longer necessary to do harmonic coefficient calibration when reading the buffered waveform of synchronous sampling channel to do FFT.	R/W	0
2:0	WAVE_HPFON	Simultaneous sampling channel high-pass filter enable bit: =0, off the Qualcomm; =1, enable high pass. Specific definitions are given below: bit2: WAVE_HPFON_U bit1: WAVE_HPFON_IB bit0: WAVE_HPFON_IA	R/W	0

5.3.4.4 WAVE_EN(0x0C new)

Simultaneous Sampling Enable Register

Offset address: 0CH; default value: 0x0

Bit	Name	Description	R/W	reset value
31:1	--	Read only.	R	0
0	WAVE_EN	Simultaneous Sampling Module Enable Register: = 0, not enabled; = 1, enable.	R/W	0

5.3.4.5 WAVECNT (0x10 new)

Sample Rate Control Register

Offset address: 10H; default value: 0x0

Bit	Name	Description	R/W	reset value
31:10	--	Read only.	R	0
9:0	WAVECNT	Used to change the sample rate of the simultaneous sample buffer waveform: If WAVECNT[9:0]=0, the sampling rate	R/W	0

		configured by WAVE_SR is valid; If WAVECNT[9:0]≠0, the sampling rate configured by WAVE_SR is invalid. If the desired number of peripheral sampling points is N, configure WAVECNT according to the following formula. The formula is: WAVECNT=(1.8432*10^6)/freq/N)-1; (freq is the grid frequency, generally 50Hz or 60Hz) The minimum write value supported at this point is 32. When a value less than 32 is written, the expected value is writable, but what actually works is alchannels 0x8F. WAVECNT reads as the current actual extraction multiplier used.		

5.3.4.6 WAVE_DC_EN (0x14 new)

AUTO DC enable register

Offset address: 14H; default value: 0x0

Bit	Name	Description	R/W	reset value
31:3	--	Read only.	R	0
2	waveu_dc_en	waveu_dc_en, waveib_dc_en, waveia_dc_en Write 1 enables simultaneous sampling channel DC Offset measurement, which is automatically cleared after the measurement is completed.	R/W	0
1	waveib_dc_en		R/W	0
0	waveia_dc_en		R/W	0

5.3.4.7 WAVE_Phs(0x18~20 new)

Bit	18H	1CH	20H
register	WAVE_PhsIA	WAVE_PhsIB	WAVE_PhsU
default value	0	0	0

Simultaneous sampling channel phase calibration register, 7bit signed number, highest bit is signed bit, R/W. See Function Description section 24.3.5 for specific function description.

5.3.4.8 WAVE_Gain(0x24~2C new)

Bit	1CH	20H	24H
register	WAVE_IAGain	WAVE_ IBGain	WAVE_ UGain
default value	0	0	0

Simultaneous sampling channel gain calibration register, 16bit signed number, highest bit is signed bit, R/W. See Description section 24.3.5 for a detailed description of the function.

5.3.4.9 WAVE_HW_RMS(0x50~58 new)

Bit	50H	54H	58H
register	WAVE_HW_RMSIA	WAVE_HW_RMSIB	WAVE_HW_RMSU
default value	0	0	0

Simultaneous sampling channel 3-channel RMS in accordance with the WAVECFG.HW_NUM configuration of the fixed number of sampling points to take the absolute value of the cumulative average calculation, the typical update rate of half a week wave.

The RMS register is a 24-bit signed number, with the highest bit 0 indicating valid data, R, normalized value = RegValue/2^23.

5.3.4.10 WAVE_HW_P(0x5C~60 new)

Bit	5CH	60H
register	WAVE_HW_PA	WAVE_HW_PB
default value	0	0

Simultaneous sampling channel 2 power in accordance with the WAVECFG.HW_NUM configuration of a fixed number of sampling point's cumulative average and open square calculation, typical update rate of half a week wave.

The power register is a 32-bit signed number, R. Normalized value = RegValue/2^31.

5.3.5 DMA Buffer Configuration and Parameter Registers (new)

5.3.5.1 DMA_WAVE_CFG(0x400 new)

DMA General Purpose Waveform Buffer Configuration Registers

Offset address: 400H; Word length: 2 bytes; Default value: 0x70

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0
14	EXTRACT	Interval buffer enable bit: =0, not enable; =1, enable. Two points buffer one point, i.e., halve the sampling rate of the waveform data source before caching the data.	R/W	0
13:10	DMA_BANK_CNT	With the number of circumferential blocks, data storage will follow a cyclic storage. For example, if the configuration is 2, there will be 3 blocks, the data will be stored in area A first, area A is full and area B is stored, then area C is stored, and then area A is stored	R/W	0

		again. Write n to the register to indicate that there are n+1 circumferential blocks, and the actual block range of 1~16 can be configured.		
9	CKM_EN	Checksum Enable Bit: = 0, no checksum is calculated; =1, waveform caching process, mode 0 calculates checksums by channel, mode 1 calculates checksums for each weekly block, checksum results are stored in registers.	R/W	0
8	WMCFG	DMA single mode, continuous mode selection: = 0, one-shot mode, no DMA operation is initiated after the write operation Buf is full; = 1, continuous mode, write operation Buf full, foldback to start over at start address.	R/W	0
7	DMAMODE	DMA mode selection: = 0, mode 0, different channel data stored by channel; =1, Mode 1, cross-storage of data from different channels by points (multiple circumferential blocks).	R/W	0
6	IB_SEL	IB channel DMA waveform buffer enable bit: = 0, not enabled; = 1, enabled.	R/W	1
5	IA_SEL	IA channel DMA waveform buffer enable bit: = 0, not enabled; = 1, enabled.	R/W	1
4	U_SEL	U-channel DMA waveform buffer enable bit: = 0, not enabled; = 1, enabled.	R/W	1
3:2	--	Read only.	R	0
1:0	DS_CFG	DMA waveform data source selection register: = 00, 7.2KHz updated waveform data after high-pass filter for metering sampling channel; =01, 14.4KHz updated waveform data before the high pass filter for the metering sampling channel; =10, selects the fundamental-wave data updated at 7.2 KHz after fundamental-wave gain calibration; =11 to select the simultaneous sampling waveform.	R/W	00

5.3.5.2 DMA_BUF_CTRL(0x404 new)

DMA General Purpose Waveform Buffer Enable Register

Offset address: 404H; Word length: 1 byte; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:1	Reserved	Reserved.	R	0
0	BUF_EN	Data buffer start bit: = 0, off; = 1, on. Note: Enable must be placed in the last step of the configuration and other configuration registers can be modified only when BUF_EN=0 and the data buffer is off.	R/W	0

5.3.5.3 DMA_BUF_BADDR(0x408 New)

Offset address register for the destination address of the DMA general-purpose data buffer
Offset address: 408H; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0
14:0	DMA_BUF_BASE_ADDR	The offset address of the destination address of the data buffer. Data buffer target address = this register value * 4 + ram base address, if this register value is set to 0xC00 and ram base address is 0x10000000 then data buffer target address = 0xC00*4 + 0x100000000 = 0x10003000.	R/W	0x0

5.3.5.4 DMA_BUF_DEPTH(0x40C new)

DMA General Purpose Data Buffer Depth Register
Offset address: 0xBC; Word length: 2 bytes; Default value: 0x8F

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0
14:0	DMA_BUF_DEPTH	Supports any depth configuration. Mode 0: This register is defined as the depth of a single channel with a depth of (N+1) (Word); The total depth of the waveform buffer is calculated from the channel depth and the channel gap depth, see section Function Description. Mode 1: This register is defined as the depth of a circumferential block with a depth of (N+1)(Word).	R/W	8F

5.3.5.5 DMA_GAP_CFG(0x410 new)

DMA General Purpose Waveform Buffer Channel Gap Configuration Registers

Offset address: 0x410; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:18	Reserved	reserved	R	0
17	IB_GAP_EN	Whether or not a gap is inserted behind the 2nd channel, the 0 = no insertion, 1 = gap insertion, valid only in mode 0	R/W	0
16	IA_GAP_EN	Whether or not a gap is inserted behind the first channel, the 0 = no insertion, 1 = gap insertion, valid only in mode 0	R/W	0
15	U_GAP_EN	Whether a gap is inserted behind the 0th channel, the 0 = no insertion, 1 = gap insertion, valid only in mode 0	R/W	0
14:0	DMA_GAP_DEPTH	Mode 0: Data buffer two-channel gap depth configuration with (N)(Word) depth; supports arbitrary depth configuration. When configured as 0, no gap space is inserted behind all channels. Note: The gap inserted after the valid data area is the same size for all channels. Model 1: Data buffer two perimeter block gap depth configurations with depth (N)(Word); arbitrary depth configurations are supported. When configured as 0, no gap space is inserted behind all circumferential blocks.	R/W	0

5.3.5.6 DMA_WAVE_ADDR(0x414 New)

DMA General Purpose Waveform Buffer Current DMA Pointer Address Register

Offset address: 0x414; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:14	--	Read only.	R	0
13:0	DMA_BUFF_ADDR	Software reads this register to get the current DMA pointer address	R	0

5.3.5.7 DMA_ERR_ADDR(0x418 New)

DMA General Purpose Waveform Buffer Data Error Occurrence Address Register DMAWAVE_ERR_ADDR
Offset address: 0x418; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:14	--	Read only.	R	0
13:0	DMAWAVE_ERR_ADDR	If any channel DMA operation does not respond during the ADC sampling interval, the data error occurrence address is logged and a DMA error interrupt is issued; the logged data error occurrence address is placed in the DMA_WAVE_ERR_ADDR register.	R	0

5.3.5.8 DMA_CHECKSUM(0x41C new)

DMA waveform checksum registers
Offset address: 0x41C; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:24	CKM_RCD	Dedicated waveform buffer data checksum.	R	0
23:16	CKM_IB	Mode 0: IB channel checksum Mode 1: Checksum of the IB channel of the previous perimeter block	R	0
15:8	CKM_IA	Mode 0: IA channel checksum Mode 1: Checksum of the IA channel of the previous perimeter block	R	0
7:0	CKM_U	Mode 0: U-channel checksum Mode 1: Checksum of the U-channel of the previous perimeter block	R	0

5.3.5.9 DMA_RCD_CFG(0x420) (new)

DMA Dedicated Waveform Buffer Configuration Registers
Offset address: 0x420; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:14	--	Read only.	R	0
13	RCD_EXTRACT	Dedicated Waveform Buffer II Extraction Enable	R /W	0
11:2	DMA_BANK_RCD_CNT	SPL_IB Number of DMA data buffer Bank blocks. Configurable range	R/W	0

		1~1024.		
1	RCD_CKM_EN	Dedicated waveform buffer checksum enable bit: = 0, no checksum is calculated; = 1, waveform caching process, mode 0 calculates checksums by channel, mode 1 calculates checksums for each channel of each waveform block, and the checksum results are stored in registers.	R/W	0
0	RCD_WMCFG	DMA single mode, continuous mode selection = 0, one-shot mode, no DMA operation is initiated after the write operation Buf is full; = 1, continuous mode, write operation Buf full, foldback to start over at start address.	R/W	0

5.3.5.10 DMA_RCD_CTRL(0x424) (new)

DMA Dedicated Waveform Buffer Enable Register

Offset address: 424H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:1	--	Read only.	R	0
0	BUF_RCD_EN	Data buffer startup bit: =0, off; =1, start. Note: Enable must be placed in the last step of the configuration and other configuration registers can be modified only when BUF_RCD_EN=0 and the data buffer is off.	R/W	0

5.3.5.11 DMA_RCD_BADDR(0x428) (new)

Offset address register for the destination address of the DMA-specific waveform buffer

Offset address: 428H; Word length: 3 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0

14:0	DMA_BUF_RCD_BADDR	The offset address of the data buffer target address. Data buffer target address = this register value * 4 + ram base address, if this register value is set to 0xC00 and ram base address is 0x10000000 then data buffer target address = 0xC00*4 + 0x100000000 = 0x10003000.	R/W	0x0

5.3.5.12 DMA_RCD_DEPTH(0x42C) (new)

DMA Dedicated Waveform Buffer Depth Register

Offset Address: 42CH; Word Length: 3 bytes; Default Value: 0x0

Bit	Name	Description	R/W	reset value
31:9	--	Read only.	R	0
8:0	DMA_BUF_RCD_DEPTH	SPL_IB DMA Data Buffer Bank Block Size in words, each word containing two points of 16bit waveform data.	R/W	0

5.3.5.13 DMA_RCD_DEPTH(0x430) (new)

DMA Dedicated Waveform Buffer Configuration Registers

Offset address: 0x430; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0
14:0	DMA_RCD_GAP_DEPTH	Data buffer two perimeter block gap depth configurations with depth (N)(Word); arbitrary depth configurations are supported. When configured as 0, no gap space is inserted behind all circumferential blocks.	R/W	0

5.3.5.14 DMA_RCD_ERR_ADDR (0x434) (new)

DMA Dedicated Waveform Buffer DMA Error Address Register

Offset address: 434H; default value: 0x0

Bit	Name	Description	R/W	reset value
31:15	--	Read only.	R	0

14:0	DMA_BUF_RCD_ERR_ADDR	If any channel DMA operation does not respond during the ADC sampling interval, the data error occurrence address is logged and a DMA error interrupt is issued; the logged data error occurrence address is placed in this register.	R	0

5.3.6 Intelligent Micro Breaker RCD Configuration and Parameter Registers

5.3.6.1 RCD_CTRL(0x480 new)

RCD control sends RCD_CTRL.

Bit	Name	Description	R/W	reset value
31:20	--	reserved	R	0
19:16	RCDDec_A	Residual current detection scheme A integrator decrement, signed number	R/W	0xF
15:12	--	reserved	R	0
11:8	RCDInc_A	Residual current detection scheme A integrator increment, signed number	R/W	0x2
7	--	reserved	R	0
6:4	RCDTapSel_B	Residual Current Program B Integrator Tap Selection '000': 216 '001': 198 '010': 180 '011': 144 '100': 126 '101': 108 '110': 72 '111': 36	R/W	0x3
3	--	reserved	R	0
2:1	RCDModeCntl	Residual current detection function mode selection configuration: '00': program A '01': Program B '10': Program A&B '11': Reserved	R/W	0x2

0	RCDTrigLatchEn	RCD Trig signal output latch enable '1': once the RCD Trig_ output has been switched from low to high to take effect, it remains high until the module is reset or re-enabled to start working. '0': not latched	R/W	1

5.3.6.2 RCD_EN(0x484 new)

RCD Program A Input Signal Threshold Registers

Bit	Name	Description	R/W	reset value
31:16	--	reserved	R	0
0	RCD_En	Residual current module work enable configuration: '1': module enable, all RCD digital channel and status registers except configuration registers are reset before startup work. '0': module off Module enable, when applying, write 0 then 1 to ensure calibration enable.	R/W	0

5.3.6.3 RCD_THRE (0x488 new)

RCD Program B Input Signal Threshold Registers

Bit	Name	Description	R/W	reset value
31:16	RCDIsThre_B	Input Signal Comparison Threshold unsigned number	R/W	0x6CA
15:0	RCDIsThre_A	Input Signal Comparison Threshold unsigned number	R/W	0x24F

5.3.6.4 RCD_ATTHRE(0x48C new)

RCD Program A Decoupling Threshold Register

Bit	Name	Description	R/W	reset value
31:16	RCDCntThre_A	Integral result upper limit, signed number	R/W	0xC8
15:0	RCDTrigThre_A	Integral result decoupling judgment threshold, signed number	R/W	0xC8

5.3.6.5 RCD_BTTHRE(0x490 new)

RCD Program B Decoupling Threshold Register

Bit	Name	Description	R/W	reset value
31:8	--	reserved	R	0
7:0	RCDTrigThre_B	Integral result decoupling judgment threshold, unsigned number	R/W	0x4C

5.3.6.6 RCD_ACNT(0x494 new)

RCD Program A Integrator Output Result Register

Bit	Name	Description	R/W	reset value
31:16	--	reserved	R	0
15:0	RCDCnt_A	Integral result, signed number	R	0

5.3.6.7 RCD_BCNT(0x498 new)

RCD Program B Integrator Output Result Register

Bit	Name	Description	R/W	reset value
31:8	--	reserved	R	0
7:0	RCDCnt_B	Integral result, unsigned number.	R	0

5.3.6.8 RCD_IE (0x49C new)

RCD Interrupt Enable Register

Bit	Name	Description	R/W	reset value
31:3	--	reserved	R	0
2	TrigSigHw_IE	Dedicated hardware triggers the end-of-trip signal occurrence interrupt enable, active high.	R/W	0
1	TrigSig_IE	Generic decoupling signal occurrence end interrupt enable, active high.	R/W	0
0	RCDTrig_IE	RCD Trig interrupt enable, active high.	R/W	0

5.3.6.9 RCD_IF(0x4A0 new)

RCD Interrupt Flag Register

Bit	Name	Description	R/W	reset value
31:3	--	reserved	R	0
2	TrigSigHw_IF	Dedicated hardware triggers end-of-trip signal interrupt signal, active high,	R/W	0

		write 1 to cleared		
1	TrigSig_IF	Interrupt signal for the end of general-purpose decoupling signal generation, active high, write 1 to cleared	R/W	0
0	RCDTrig_IF	RCD Trig port output trigger interrupt signal, high level active, write 1 cleared	R/W	0

5.3.6.10 RCD_STA(0x4A4 new)

RCD Status Register

Bit	Name	Description	R/W	reset value
31:3	--	reserved	R	0
2	RCDTrig_B	Trig_B Internal signal latch register, active high. Once the register output has been switched from low to high to take effect, it remains high until the module is reset or re-enabled to start operation.	R	0
1	RCDTrig_A	Trig_A Internal signal latch register, active high. Once the register output is switched from low to high to take effect, it remains high until the module is reset or re-enabled to start operation.	R	0
0	RCDTrig	RCD Trig port output signal, active high	~~R~~	0

5.3.6.11 TRIG_CTRL(0x4B0 new)

TRIG Control Register

Bit	Name	Description	R/W	reset value
31:6	--	reserved	R	0
5	RCDPostSel	Residual current detection input signal selection 0: RCD pre-latch input 1: Input after RCD latch	R/W	0
4	RcdTrigSel	Hardware decoupling signal selection 0: Dedicated hardware release signal 1: Residual current detection input signal	R/W	0
3	TrigOutSel	Trig signal output selection 0: Generation signal for general or specialized release signals 1: Universal release signal generation signal	R/W	0
2	TrigMaskHw	Universal Signal Generator Hardware Trigger Mask Control	R/W	1

		'1': blocking hardware source trigger (does not respond to residual current hardware detection trigger signal) '0': no shielding of hardware source triggering (in response to residual current hardware detection trigger signal)		
1	TrigSigVal	Trig Signal Output Effective Level Control for Off-Trigger Signal Generator '1' high level effective '0' low level active	R/W	1
0	TrigSigMode	Off-trigger Trig signal function mode selection '0': alchannels active mode '1': length-assignable mode	R/W	1

5.3.6.12 TRIG_EN(0x4B4 new)

General Trig Software Enable Control Registers

Bit	Name	Description	R/W	reset value
31:1	--	reserved	R	0
0	TrigEnSw	General trig signal generator software enable control 0: no action 1：Start the debounce signal generation Rising edge trigger, write 0 and then 1 before each configuration, the bit is valid when the release signal generation is in idle state.	R/W	0

5.3.6.13 TRIG_STOP(0x4B8 new)

Trig stop control register

Bit	Name	Description	R/W	reset value
31:2	--	reserved	R	0
1	TrigStopHw	Hardware-specific trig signal generator stop control '0': no action '1' : Stop the current trig signal generation into idle state Rising edge triggered, the register control is valid only in the working state, write 0 firstly and write 1 secondly before each configuration, the register control is valid only in the working state, the register control is valid only in the working state,	R/W	0

		write 0 firstly and write 1 secondly before each configuration. Configure this signal to turn off signaling without triggering an interrupt		
0	TrigStopSw	General trig signal generator stop control '0': no action '1' : Stop the current trig signal generation into idle state Rising edge triggered, the register control is valid only in the working state, write 0 firstly and write 1 secondly before each configuration, the register control is valid only in the working state, the register control is valid only in the working state, write 0 firstly and write 1 secondly before each configuration. Configure this signal to turn off signaling without triggering an interrupt	R/W	0

5.3.6.14 TRIG_LEN(0x4BC new)

General TRIG Signal Length Register

Bit	Name	Description	R/W	reset value
31:18	--	reserved	R	0
17:0	TrigSigLen	Trig Signal Generator Signal Length Configuration Actual length: (N+1)*542.528ns 18bit @1.84M clock The default value is 40ms	R/W	0x12001

5.3.6.15 TRIG_DLY(0x4C0 new)

General Purpose Decoupling TRIG Startup Delay Register

Bit	Name	Description	R/W	reset value
31:16	--	reserved	R	0
15:0	TrigSigStatDelay	Delayed start-up of decoupling signal When configured to 0, there is no delay. When configured to a value other than 0, the Time delay: (N+1)*542.528ns 16bit @1.84M clock	R/W	0

5.3.6.16 TRIG_STA(0x4C4 new)

General Tripping TRIG Status Register

Bit	Name	Description	R/W	reset value
31:22	--	reserved	R	0
21:4	TrigCnt	Trig internal counter	R	0
3	--	reserved	R	0
2	TrigGen	Trig signal valid status register '0': invalid state '1': valid status	R	0
1	TrigBusy	Trig signal busy status register '0': Idle state '1': working status	R	0
0	TrigOut	Trig output signal (TrigOutSel selection control)	R	0

5.3.6.17 TRIG_LEN2(0x4C8 new)

Hardware-specific trig length register

Bit	Name	Description	R/W	reset value
31:18	--	reserved	R	0
17:0	TrigSigLenHw	Hardware-specific trig signal generator signal length configuration Actual length: (N+1)*542.528ns 18bit @1.84M clock This configuration parameter needs to be greater than 0, the default value is 40ms	R/W	0x12001

5.3.6.18 TRIG_STA2(0x4CC new)

Hardware-specific trig status register

Bit	Name	Description	R/W	reset value
31:22	--	reserved	R	0
21:4	TrigCntHw	Trig internal counter	R	0
3:2	--	reserved	R	0
1	TrigBusyHw	Trig signal busy status register '0': Idle state '1': working status	R	0
0	--	reserved	R	0

5.4 special command

Command Name	Command register	Value	Description
Write Enable Command	1A8	0xE5	Enabling Metering Module Write Operations
Write Protect Command	1A8	0xDC	Turn off metering module write operations
Current A channel Select Command	1A8	0x5A	The current A channel setup command specifies that the current channel currently used to calculate active/reactive power is A channel; it has no effect on the RMS and power registers; The command is accepted by the system only after a write enable; the CHNSEL register bit in the Metering Status Register reflects the result of the command's execution.
Current B channel Select Command	1A8	0xA5	The current B channel setup command specifies that the current channel currently used to calculate active/reactive power is B channel; it has no effect on the RMS and power registers; The command is accepted by the system only after a write enable; the CHNSEL register bit in the Metering Status Register reflects the result of the command's execution.

Scope of write protection:

Original configuration register (0x00~0x6C), new configuration register (0x74~0xD0), new DMA waveform buffer configuration register (0x400~0x410, 0x420~0x42C), new RCD configuration register (0x480~0x490), original fast pulse register (0xC0~C8, 0x100~108) The new fast pulse register (0xE0~FC), the original interrupt enable register EMMIE (0x18C), the new interrupt enable register EMMIE2 (0x1A0), EMMIE3 (0x1B0) can be written and modified only after writing enable with special commands, the specific command format is shown in the above table.

5.5 Calibration method

Supported calibration methods:

- Pulse method of meter calibration
- power law meter calibration

5.5.1 Pulse method of meter calibration

Steps and algorithms:

A. Basic parameter determination (the content of this item can be fixed in the soc program)

1) Voltage and current conversion factor

Voltage conversion factor: Kv=Ra/(Rt*Upga*2^23)

Rt: Sampling resistance of the resistor divider series

Ra: Total resistance of the resistor series

Upga: voltage A channel DC gain magnification

Current conversion factor: Ki=1/(Ri*Ipga*2^23)

Ri: Manganese copper sampling resistance (in the case of transformers Ri = R0/PT, where R0 is the sampling resistance on the secondary side of the transformer and PT is the ratio of the transformer).

Ipga: current A channel DC gain magnification

2) Determine the meter pulse constant EC and HFConst register values, power conversion factor

Meter pulse constant EC: for testing and power calculations (meter type determination, e.g. 1200 imp/kwh)

Power conversion factor: Kp=Ra/[(Ri*Ipga)* (Rt*Upga)* 2^31]

Rt: Sampling resistance of the voltage divider series of the voltage sampling loop

Ra: Total resistance of voltage sampling loop divider resistor series

Ri: manganese-copper sampling resistance (in the case of transformers Ri = R0/PT, where R0 is the sampling resistance of the secondary side of the transformer and PT is the ratio of the transformer).

Upga: voltage A channel DC gain magnification

Ipga: current A channel DC gain magnification

HFConst=INT[(Ri*Ipga)*[(Rt*Upga)/Ra]*3.6*10^6*fd2f/(2*EC)]

=INT[1.8*10^6*fd2f*(Ri*Ipga* Rt*Upga)/(Ra*EC)]

fd2f is 0.9216Mhz (0.9216*10^6)

3) Active startup power, reactive startup power determination

Pstart (0CH) = 0.7*Pstart*(1/Kp)/2^8 ;

P_{start}: Power at startup Unit: w

Kp: Power conversion factor

The coefficient 0.7 is a recommended value and can be adjusted for practical applications.

The Qstart (10H) value is equal to Pstart or adjusted as needed.

B. Voltage and current RMS calibrations: station plus Un, Ib, power factor 1.0

Mainly obtain the current and voltage channel gain IAGain (44h) and UGain (4ch) values.

IAGain = ((I0/I)-1))*2^15 I0>I

(I0/I)-1))*2^15+2^16 I0<I

I0=Ib*1/Ki

I: Current RMS register (IARMS (10CH)) measured value

Ib: Standard meter display current value

Ki: Current conversion factor

UGain = ((U0/U)-1))*2^15 U0>U

(U0/U)-1))*2^15+2^16 U0<U

U0=Un*1/Kv

U: Voltage RMS register (URMS (114H)) measured value

Un: Standard meter display voltage value

Kv: voltage conversion factor

C. 1.0 Error calibration for power gain: station still adds Un, Ib, power factor 1.0

After the previous step B, the 1.0 error is basically accurate and can be ignored if the requirements are not high.

Primary determines power gain register GPQA (14H) (reactive power gain writes GPQA same value)

$$Pgain = \frac{-err}{1+err}$$ (err: table display error value)

If Pgain>=0, then GPQA=INT[Pgain*2]^{15}

Otherwise Pgain<0, then GPQA=INT[2^{16} +Pgain*2]^{15}

D. 0.5L phase calibration: the station still adds Un, Ib, power factor 0.5L

$$\theta = \text{Arcsin}\frac{-err}{\sqrt{3}}$$ (err: table display error value)

For 50 HZ, PHSA/B has a relationship of 0.0097656^0 /LSB, which gives us

If θ >= 0, PHSA/B = INT((θ *180/3.1415928)/0.0097656) ^{0}

If θ < 0, PHSA/B =INT(2^9+ θ *180/3.1415928)/0.0097656)^0

For 60Hz, the calibration scale is 0.01171875^0 /LSB

E. Active Bias OFFSET calibration: Station plus Un, 10% Ib or 5% Ib, Power Factor 1.0

APOSA (address 28H) = (P0*1/Kp)*(-err) (for err<0)

=2^16+(P0*1/Kp)*(-err) (for err>0)

P0: Standard meter display power value err: Table display error value

F. RMS Current OFFSET calibration: Table plus Un Unloaded

Reading the current RMS register 10 times (at intervals of 100ms or more) averaging, squaring and inverting the

Write bit23~bit8 to current offset register IARMSOS (38h)

IARMSOS (38H) = (2^24- Iavreg^2)/2^8

Iavreg: Average of 10 current RMS registers (IARMS (10cH)).

5.5.2 Power law meter calibration

The power meter calibration method has the advantages of being fast, simple, and efficient compared to the pulse meter calibration method, and can support a single point, but has requirements for the stability of the table.

Table body plus Un, Ib, power factor 0.5L

Steps and algorithms:

A. Basic parameter determination (this item can be fixed in the soc program, same as pulse method)

1) Voltage and current conversion factor

2) Determine meter pulse constant EC and HFConst register values, power conversion factor

3) Active startup power, reactive startup power determination

B. Voltage and current RMS calibration

Same **pulse calibration method**

C. 1.0 Error calibration for power gain: negligible

D. 0.5L phase calibration:

The calculation formula refers to the pulse accuracy calibration method, the error of the different point power method is calculated by power.

Formula err=[P-P0*(1/Kp)] / (P0*(1/Kp))

$$\theta = \text{Arcsin}\frac{-err}{\sqrt{3}}$$

P: measured power register value

For 50 HZ, PHSA/B has a relationship of 0.0097656^0 /LSB, which gives us

Ifθ >= 0, PHSA/B = INT((θ *180/3.1415928)/0.0097656) ^{0}

Ifθ < 0, PHSA/B =INT(2^9+θ *180/3.1415928)/0.0097656)^0

E. Active bias OFFSET: Same as pulse accuracy calibration method.

err=[P-P0*(1/Kp)] / (P0*(1/Kp))

P: Measured power register value (averaged over 10 readings)

P0: Power value displayed by the standard meter

APOSA (28) = (P0*1/Kp)*(-err) (for err<0)

=2^16+(P0*1/Kp)*(-err) (for err>0)

F. Current RMS OFFSET calibration: Same as pulse accuracy calibration method.

Read the current RMS register 10 times (at 100ms intervals) averaged, squared and inverted, and

Write bit23~bit8 to current offset register IARMSOS (38h)

IARMSOS (38h) = (2^24- Iavreg^2)/2^8

Iavreg: Average of 10 current RMS registers (IARMS (10cH)).

6 No-voltage measurement (NVM)

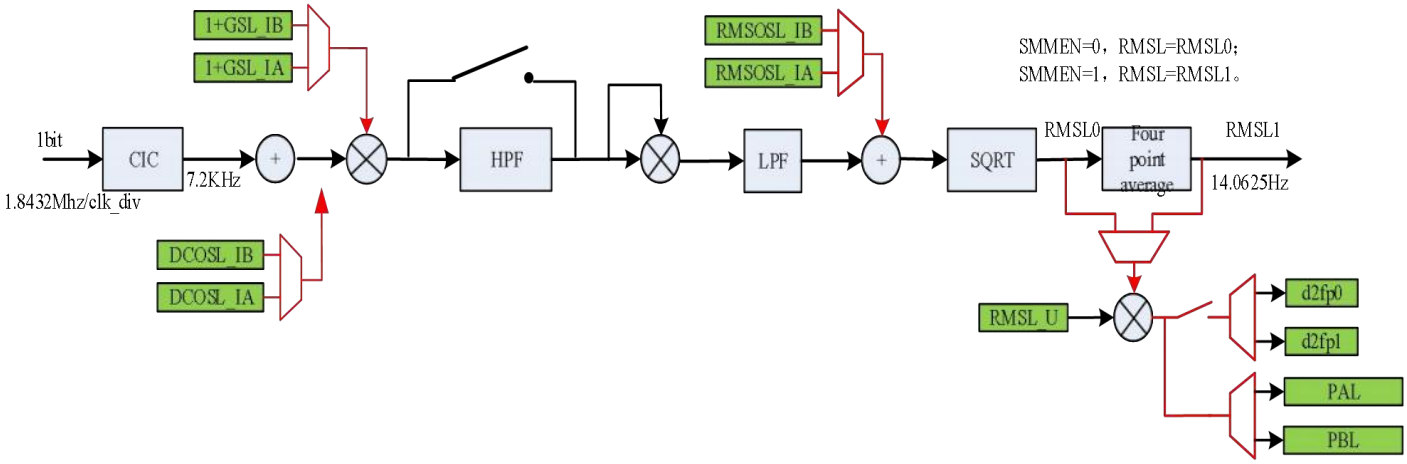
The no-voltage measurement is a low-power metering mode, when CPU work at 32K, NVM metering power consumption better than 600uA.

6.1 Main features

Base Address : 0x40040000

- 5%Ib error is less than 0.5%;
- Power consumption is less than 0.6mA;
- Supports IA/IB measurement，singal channel measurement time - 80ms;
- Very low DC offset;
- Supports IA/IB dual DC Offset correction;
- Supports IA/IB dual gain correction;
- Supports IA/IB dual AC Offset correction;
- Supports 1bit rate 1.8432MHz and its 2/4/8 divisions;
- Supports automatic filling of power values into D2F registers for integration

6.2 Functional block diagram



NVM has two power consumption modes：

When PM_SEL=0，the ADC clock source is the RCH divided clock 1.8M, which is downwardcompatible by default, NVM mode is a large power consumption mode and NVM power consumption is 1.5mA.

When PM_SEL=1, the ADC clock source is the RCM-divided clock 1.8M, NVM mode is a small power consumption mode and NVM power consumption is 600uA

.PM_SEL is described in OSC_CTL2 register bit22.

6.3 NVM measurement mode

6.3.1 Single-channel mode (downwardcompatible)

1. Enable IA channel ADC or IB channel ADC through system control (one at a time).
2. Initiate the NVM measurement.。
3. After measurement, read the current channel's RMS value from reg ,.

Both two channels use the same set of registers LS_DCOS, LS_THO, LS_RMS.

6.3.2 Dual-channel simultaneous measurement mode

1. Select the new NVM mode by configuring the registers, in which the DCOS, THO, GS, RMS of the two channels are configured in independent registers. And the RMS comparison results of IA and IB channels are output to two independent flag bits respectively, which can be out of interrupt.
2. Enable both IA channel ADC and IB channel ADC through system control
3. Initiate the NVM measurement.。
4. After measurement, getting the current RMS values of the IA and IB channels through the registers. The comparison result of the RMS values of the two channels can be obtained at the same time.

6.4 Register list

BaseAddr：0x40040000

Measurement section register list

address	name	R/W	length	reset value	Functional Description
Calibration parameters and metering control registers					
00H	NVM_IE	R/W	1	07H	NVM interrupt enable register
04H	NVM_IF	R/W	1	0	NVM interrupt flag register
08H	LSCFG	R/W	2	0	NVM configuration Register
0CH	LSDCOS	R/W	3	0	NVM DC offet correction registers
10H	LSTHO	R/W	3	0	NVM threshold setting register
14H	LSRMS	R	3	0	NVM RMS register，cycle update
18H	LSRMS1	R	3	0	NVM RMS register，update after calculation
1CH	---	R/W	1	0	reservations
20H	HFConst	R/W	2	0	Custom Pulse Frequency Register
24H	D2FP0	R/W	3	0	Custom power register 0
28H	D2FP1	R/W	3	0	Custom Power Register 1
2CH	LSMODE	R/W	2	0	NVM Mode Configuration Register
30H	LSDCOSIB	R/W	3	0	NVM mode IB channel DC Offset correction register, valid only in dual channel mode.
34H	LSTHOIB	R/W	3	0	NVM Mode IB Channel Full Loss of Voltage Threshold Register, valid only in dual channel mode
38H	LSGSIA	R/W	2	0	NVM mode IA channel gain registers
3CH	LSGSIB	R/W	2	0	NVM mode IB channel gain register, valid only in dual-channel mode.
40H	LSRMSIB	R	3	0	NVM Mode IB Channel RMS register, updated on a fixed cycle; valid only in dual-channel mode
44H	LSRMSIB1	R	3	0	NVM Mode IB Channel RMS register, updated only 1 time after calculation. Valid only in dual-channel mode.
48H	LSADCINCFG	R/W	1	0	NVM mode ADC input configuration registers
4CH	LSRMSUA	R/W	3	0	NVM Mode Custom Voltage RMS Registers
50H	LSPA	R/W	3	0	NVM mode A-way active power registers
54H	LSPB	R/W	3	0	NVM mode B-way active power registers

6.5 Register Description

6.5.1 NVM_IE (0x0)

NVM interrupt enable register

Offset address: 0x0; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	R	
9	ib_ov_ie	Full loss of voltage calculation is complete and the IB channel exceeds the set threshold interrupt enable: = 0: not enabled = 1: Enable	R/W	0
8	ia_ov_ie	Full loss of voltage calculation is complete and the IA channel exceeds the set threshold interrupt enable: = 0: not enabled = 1: Enable	R/W	0
7:6	Reserved	Reserved	R	0

5	D2F1_CF_IE	D2F1 pulse output interrupt enable = 0: not enabled = 1: Enable	R/W	0
4	D2F0_CF_IE	D2F0 pulse output interrupt enable = 0: not enabled = 1: Enable	R/W	0
3	VREF_LOW_IE	VREF reset interrupt enable occurs = 0: not enabled = 1: Enable	R/W	0
2	LDO3_LOW_IE	LDO3 reset interrupt enable occurs =0: Not enabled; = 1: Enable	R/W	0
1	NVM_DoneIE	Full loss of voltage calculation is complete and exceeds the set threshold interrupt enable: = 0: not enabled = 1: Enable	R/W	0
0	NVCAL_DoneIE	Full loss of voltage calculation completion interrupt enable = 0: not enabled = 1: Enable	R/W	0

6.5.2 NVM_IF (0x4)

NVM interrupt flag register

Offset address: 0x4; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:9	Reserved	Reserved	R	
9	ib_ov_if	Full loss of voltage calculation is complete and the IB channel exceeds the set threshold interrupt flag: = 0: not occurred = 1: occurred	R/W	0
8	ia_ov_if	Full loss of voltage calculation is complete and the IA channel exceeds the set threshold interrupt flag: = 0: not occurred = 1: occurred	R/W	0
7	nvm_bgrok_sp	BGR Work Status Flag = 0: Unnormal work = 1: Normal work	R/W	0
6	nvm_avddok_sp	AVDD Work Status Flag = 0: Unnormal work = 1: Normal work	R/W	0
5	D2F1_CF_IF	D2F1 pulse output interrupt flag = 0: not occurred = 1: occurred	R/W	0

4	D2F0_CF_IF	D2F0 pulse output interrupt flag = 0: not occurred = 1: occurred	R/W	0
3	VREF_LOW_IF	VREF reset interrupt flag occurs = 0: not occurred = 1: occurred	R/W	0
2	LDO3_LOW_IF	LDO3 reset interrupt flag occurs = 0: not occurred = 1: occurred	R/W	0
1	NVM_DoneIF	Full loss of voltage calculation completed and exceeds the set threshold interrupt flag = 0: not occurred = 1: occurred	R/W	0
0	NVCAL_DoneIF	Full loss of pressure calculation completed interrupt flag = 0: not occurred = 1: occurred	R/W	0

6.5.1 LSCFG（0x8）

NVM configuration Register

Offset address: 0x8; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:13	Reserved	Reserved	R	
12	D2F_ATMODE	D2F auto mode enable bit = 0: Does not automatically fill power into D2F; = 1: Automatically fills power into D2F; Single-channel mode: If channel A is enabled, PA fills in D2FP0; if channel B is enabled, PB fills in D2FP1. Dual-channel mode: Fill PA into D2FP0 and PB into D2FP1 at the same time. Note: When auto D2F, after the RMS value calculation is completed, need to wait for 1clk before power updating.	R/W	0
11	CIC_MODE	= 0, CIC fixed point count, 128 points per weekly wave; = 1, two internal CIC, and real-time frequency measurement for compensation;	R/W	0
10:8	RMS_DIV	Valid values RMSL_IA and RMSL_IB output value configuration: = 000, not average; = 001, 2-point average; = 010, 4-point average; = 011, 8 o'clock average;	R/W	0

		= 100, 16-point average; = 101, 32-point average; = 110, 64-point average; = 111, 128 point average.		
7:6	RMS_SP	Valid values RMSL_IA and RMSL_IB Output Value Configuration, Start Average Points Configuration Register: = 00, RMS values are averaged from the 1st point; = 01, RMS values are averaged from the 2nd point, the first 1 point is discarded; = 10, RMS values are averaged from the 3rd point and the first 2 points are discarded; = 11, RMS values are averaged from the 4th point and the first 3 points are discarded.	R/W	0
5	D2F1_CF_EN	D2F1 pulse output enable: =0, the pulse of the D2F1 module does not output to the IO, but the interrupt and the flag are all; =1, the pulse output of the D2F1 module is output to the IO port of the QF pulse (P50 or P51, depending on IO port multiplexing configuration)	R/W	0
4	D2F0_CF_EN	D2F0 pulse output enable: =0, the pulse of the D2F0 module does not output to the IO, but the interrupt and the flag are all; =1, the pulse output of the D2F0 module is output to the IO port of the PF pulse (P50 or P51, depending on IO port multiplexing configuration)	R/W	0
3	SMMEN	NVM RMS update time configuration: =0: RMS 20ms update, stabilized concurrent interrupt at 80ms = 1: RMS 80ms update, stabilized concurrent interruptions at 160ms	R/W	0
2	NVMEN	NVM Compute Enable: = 0: not enabled = 1: enable	R/W	0
1	HPFON_LS	NVM High Pass Enable: = 0: Shut down Qualcomm = 1: Turn on Qualcomm Default high pass is off, it is recommended to use the DC OFFSET auto-correction function, not high pass, in order to speed up the stabilization time.	R/W	0
0	LSDC_EN	DC OFFSET auto-correct enable: = 0: not enabled = 1: enable	R/W	0

6.5.2 LSDCOS（0xC）

NVM DC offet correction registers

Offset address: 0xC; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:24	Reserved	Reserved	R	
23:0	LS_DCOS	DC offset correction during full loss of voltage measurement, offset value is directly summed with the 24bit sampling value LS_MODE.NVM_MODE=0: Both IA channel and IB channel are configured with this register. LS_MODE.NVM_MODE=1: IA channels are configured using this register and IB channels are configured using LS_DCOSIB.	R/W	0

6.5.3 LSTHO（0x10）

NVM threshold setting register

Offset address: 0xC; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:24	Reserved	Reserved	R	
23:0	LS_THO	Full loss of voltage measurement threshold setting register, compare RMS_L with this threshold. LS_MODE.NVM_MODE=0: Both IA and IB channels use this threshold to compare registers. LS_MODE.NVM_MODE=1: The IA channel uses this threshold comparison register and the IB channel is configured using LS_THOIB.	R/W	0

6.5.4 LSRMSx（0x14~0x18/0x40/0x44，new）

NVM RMS register

offset address	14H	18H	40H	44H
register	LSRMS	LSRMS1	LSRMSIB	LSRMSIB1
default	0x0	0x0	0x0	0x0

NVM RMS registers are 24-bit signed numbers, the highest bit is 0 to indicate valid data, the reading is done zero processing when the highest bit is 1.

LS_RMSx is updated according to a fixed period, and the update time is configured according to the LS_CFG register;

LS_RMSx1 is not updated after the computation is complete, and the update time is configured according to the LS_CFG register.

LS_MODE.NVM_MODE = 0: single-channel mode, LS_RMS and LS_RMS1 output the RMS value (IA or IB) of the channel depending on which ADC is enabled by the system control SYS_PD register, LS_RMSIB and LS_RMSIB1 are invalid.

LS_MODE.NVM_MODE =1: dual-channel mode, LS_RMS and LS_RMS1 fixed output IA channel RMS, LS_RMSIB and LS_RMSIB fixed output IB channel RMS.

The RMS calculation start point and the average number of points are assignable, see descriptions of the LS_CFG registers RMS_SP and RMS_DIV

Taking the IA channel as an example, the relationship between the RMS value of the total loss of voltage measurement and the RMS value of the normal metering is: LS_RMS=(2*sqrt(2)/PI)*IARMS

6.5.5 HFConst（0x20）

Custom Pulse Frequency Register

Offset address: 0x20; default: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	
15:0	HFConst	Customized pulse frequency register, also used as clock enable signal for D2F module = 0: Clock off = Other, clock on	R/W	0

6.5.6 D2FPx（0x24~0x28）

Customized power registers

offset address	24H	28H
register	D2FP0	D2FP1
default	0x0	0x0

Custom power register, 24bit valid, highest bit is sign bit.

Users can fill in the power value, output different frequency pulses D2Fx_CF according to the configuration of HFConst. The pulse width of high level is fixed at 82ms, and when the period is less than 164ms, it outputs equal duty waveform.

6.5.7 LSMODE（0x2C，new）

NVM Mode Configuration Register

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	
15:0	NVM_MODE	NVM Mode Configuration Register: = Write 0x5901, NVM mode configured to dual-channel mode, read 1; = Write other values, downward compatible, NVM mode configured as single channel mode, read 0.	R/W	0

6.5.8 LSDCOSIB（0x30，new）

Full loss of voltage IB channel DC offset register，

valid when WAVECFG.MODE_SEL=0 and LS_MODE.NVM_MODE=1

Bit	Name	Description	R/W	Reset Value
31:24	Reserved	Reserved	R	0
23:0	LS_DCOSIB	The IB channel DC Offset correction is performed during full loss-of-voltage measurements, and the Offset value is directly summed with the 24bit sampling value. EMU_WAVECFG.MODE_SEL=0 and LS_MODE.NVM_MODE=1	R/W	0

6.5.9 LSTHOIB（0x34，new）

Full loss of voltage IB channel RMS threshold setting register,

valid when WAVECFG.MODE_SEL=0 and LS_MODE.NVM_MODE=1

Bit	Name	Description	R/W	Reset Value
31:24	Reserved	Reserved	R	0
23:0	LS_THOIB	Full Loss of Voltage Measurement IB Channel Threshold Setting Register, which compares LS_RMSIB with this threshold. EMU_WAVECFG.MODE_SEL=0 and LS_MODE.NVM_MODE=1	R/W	0

6.5.10 LSGSIx（0x38~0x3C，new）

NVM RMS Gain Register

offset address	38H	3CH
register	LSGSIA	LSGSIB
default	0x0	0x0

NVM RMS Gain Register, 16bit signed number, valid when WAVECFG.MODE_SEL=0.

Power auto integration mode is used, the hardware automatically calculates the effective value LS_RMS1*LS_GSIA and fills in D2FP0; the hardware automatically calculates the effective value LS_RMSIB1*LS_GSIB and fills in D2FP1.

6.5.11 LSADCINCFG (0x48, new)

NVM mode ADC input configuration registers

Offset address: 48H; default value: 0x0

Bit	Name	Description	R/W	Reset Value
31:24	WKEY	Write password register: = 0xEA, low 24 bits writable; = other values, low 24 bits are not writable.	WO	0
23:6	Reserved	Reserved	R	0
5	ua_smp_sel	U channel 1bit sample edge selection register: = 0, rising edge; = 1, falling edge.	R/W	0

4	ib_smp_sel	IB channel 1bit sample edge selection register: = 0, rising edge; = 1, falling edge.	R/W	0
3	ia_smp_sel	IA channel 1bit sample edge selection register: = 0, rising edge; = 1, falling edge.	R/W	0
2	ua_inv_en	U channel 1bit input reverse enable register: = 0, no operation; = 1, reverse.	R/W	0
1	ib_inv_en	IB channel 1bit input reverse enable register: = 0, no operation; = 1, reverse.	R/W	0
0	ia_inv_en	IA channel 1bit input reverse enable register: = 0, no operation; = 1, reverse. Remarks: Used in case of ADC input inversion. If the ADC input is inverted, configuring the 1bit input inverted will make the sampling signal sign correct and offset the error of the ADC input being inverted.	R/W	0

6.5.12 LSRMSU（0x4C，new）

NVM Mode Custom Voltage RMS Registers

offset address	4CH
register	RMSL_U
default	0x0

The NVM mode custom voltage RMS register is a 24-bit signed number.

This register is multiplied with RMS_L1_IA and RMS_L1_IB to get the power, then saved to the power to the power registers LS_PA and LS_PB, with configurable autofill to D2F.

6.5.13 LSPx（0x50~0x54，new）

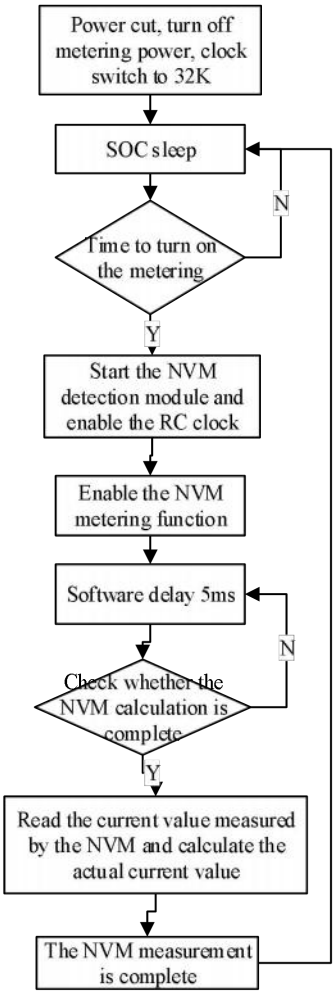
NVM Mode Active Power Registers

offset address	50H	54H
register	LSPA	LSPB
default	0x0	0x0

Custom power register, 24bit valid, highest bit is sign bit.

6.6 Implementation method

6.6.1 Realization Flowchart



6.6.2 Procedure realization steps

According to the above flowchart, the program can periodically turn on the full loss of voltage module for current measurement, the program implementation and register setting steps are as follows:

1、 The SOC is powered down and enters low-power mode, all peripheral clocks are turned off and the SOC master clock runs at 32768Hz.

2、 After the set metering interval is satisfied, the NVM module is initialized for current measurement and the initialization step:

1） Enable system control register password protection, SYSCTL->SYS_PS write to 82H.

2） Set bit0 of SYSCTL->SYS_PD register to 0, I1 channel power supply is powered up

3） If a manganese-copper shunt is used for the current measurement channel, set the SYSCTL->ADC_CTRL register to 03H, and the gain of the I1 channel to be set to 16x or 0, 1x gain if a transformer is used.

4） Set bit8 of SYSCTL->MOD1_EN to 1, turn on the APB clock of the NVM module

5） Set bit1 of SYSCTL->OSC_CTRL1, turn on the RC clock to clock the NVM module

6） Set NVM->LS_DCOS to write the corrected DC bias value

7） Clear the flag of NVM->NVM_IF.

8） Set bit2 of NVM->LS_CFG to 1, start NVM measurement

After the above steps, the initialization setup of the NVM module is complete.

3、 After the initialization is completed, soft delay, waits for the NVM measurement to be completed, during which the bit0 of NVM->NVM_IF can be queried, if it is 1, it means that the measurement is completed, and the measured value can be read. The general waiting time is about 80MS.

4、 Read the NVM->RMS_L value, which is the register value of the current measurement channel, should be related to the normal metering RMS value as follows: IARMS = RMS_L /(2*sqrt(2)/PI). If IAGain is corrected during the calibration of the meter, the effect of IAGain needs to be taken into account when calculating IARMS.

5、 Current measurement and calculation is completed, set bit0 of SYSCTL->SYS_PD to 1 to turn off the power supply of the measurement channel, set bit8 of SYSCTL->MOD1_EN to 0 to turn off the APB clock of the NVM module, and set bit1 of SYSCTL->OSC_CTRL1 to 1 to turn off the RC clock.

6、 Measurement is completed, wait for the measurement interval to expire before starting the measurement again.

6.7 DC Offset Correction Process for NVM

This step can be performed while calibration meter.

1. Only voltage is applied to the meter and no current is added，automatic offset correction of current
2. The meter needs to turn off the digital high pass filter for the measurement channel when in normal metering mode.
3. EMU->IAGAIN channel gain register is set to 0.
4. Set SYSCTL->SYS_PD to turn on the power of the full loss of voltage measurement channel only, and turn off the power of other ADC channels.
5. The bit8 of SYSCTL->MOD1_EN is set to 1, turn on the APB clock of the NVM module 。
6. The bit1 of SYSCTL->OSC_CTRL1 is set to 0, turn on the RC clock
7. Set NVM->LS_DCOS to 0 and bit2 of NVM->LS_CFG to 1，initiate NVM module measurement
8. After waiting for 80MS, read the NVM->RMS_L register value and save it in EEPROM as the DC offet calibration value for the NVM module
9. Restores each register set earlier.

Auto OFFSET calibration is complete.

6.8 Electric energy integral

Some applications measure the current loop current under battery power supply, the voltage according to the rated voltage for energy integration, according to the above steps, we can accurately get the current value, multiplied by the rated voltage to get the current power value. After calculating the power it is recommended to use the following method to perform the integration operation of energy:

1、 Set the HFConst register (20H) of this section, when the pulse power is accumulated to the HFConst value, it is accumulated to get 1/EC Kwh of power. The HFConst register size can be adjusted as needed to ensure accurate pulse output at a certain power.

2、 Timed start current measurement, the current value obtained from each start measurement is multiplied by a fixed factor to obtain the power value, which is written to the D2FP0 or D2FP1 register,

3、 The soc hardware automatically completes the energy integration, and can notify the CPU to integrate to get a pulse through interrupt. It can also output a pulse signal through the IO port for accuracy checking

7 Flash FLK (new)

7.1 Main features

- Provide instantaneous voltage, which is updating in 600Hz
- The software calculates the instantaneous visual susceptibility (600Hz), the short-time flicker Pst (10 minutes) and the long-time flicker Plt (2 hours) by itself based on this voltage value.
-

7.2 Usage

The flicker calculation process：

step	data manipulation
1. Sampling	adc_in, 7.2KHz update
2. Low-pass filter	Can directly downconvert 7.2Khz to 600Hz.
3. Extraction	7.2KHz 600Hz
4. Square and calculate the RMS value	Software implementation
5. Square off DC	Software implementation
6. Normalization	Software implementation
7. Qualcomm	Software implementation
8. Butterworth Low Pass	Software implementation
9. Smoothing	Software implementation
10. Weighting	Software implementation
12. Square	Software implementation
13. Low Pass	Software implementation
14. Multiplication factor	Software implementation
15. Counting statistics	Software implementation
16. Pst calculations	Software implementation

Hardware input: instantaneous voltage value, update rate is 7.2KHz
Hardware output: FLK module hardware calculations to step 3, the 7.2Khz instantaneous sampling value through a low-pass filter, downsampling to 600Hz output 24bit instantaneous voltage value, for the 300Hz above the component has a 40dB attenuation, for low-cost flicker program, the CPU reads the instantaneous value, can be realized by the software to calculate the instantaneous visual susceptibility (600Hz), Pst (10 minutes) and Plt (2 hours).
For details, please refer to the Sharpener Microflash application notes

7.3 Register list

base address	**0x50020000**				
offset address	**name**	**R/W**	**length**	**reset value**	**Functional Description**

0x0	FLK_EN	R/W	1	0x00	The FLK module enable, and the change of the enable signal from 0 to 1 resets all the computing modules.。
0x4	FLK_IE	R/W	1	0x00	FLK Module Interrupt Enable
0x8	FLK_IF	R/W	1	0x2	FLK Module Interrupt Flag
0xC	UA_600Hz	R/W	3	0x0	Instantaneous sampling of UA channels, update rate of 600 Hz
0x10	FLK_PASS	R/W	2	0x0	module password

Note: To enable the module, you must first turn on the module's clock, the method to turn on the clock.

7.4 Register Definition

7.4.1 FLK_EN (0x00)

FLK module enable register

Offset address : 0x00; Word length: 1 byte; Default value: 0

Bit	Name	Description	R/W	Reset Value
31:01	Reserved	Reserved	R	0
0	FLK_EN	= 0: FLK modules are not counted; = 1: FLK module starts counting. Changing from 0 to 1 resets the flicker module calculation unit. This bit can only be written to 1 if the FLK_PASS password is correct.	R/W	0x0

7.4.2 FLK_IE (0x04)

FLK module interrupt enable register

Offset Address: 0x04; Word length: 1 byte; Default value:0

Bit	Name	Description	R/W	Reset Value
31:01	Reserved	Reserved	R	0
0	FLK_IE	=0：disable =1：enable	R/W	0

7.4.3 FLK_IF (0x08)

FLK module flag register

Offset address: 0x08; Word length: 1 byte; Default value:0

Bit	Name	Description	R/W	Reset Value
31:01	Reserved	Reserved	R	0
0	FLK_IF	= 0: FLK module calculations not completed = 1: FLK module calculations completed This flag bit is cleared by writing 1	R/W	0

		Whether or not this flag bit is generated has no bearing on the IE.		

7.4.4 UA_600HZ (0x0C)

Instantaneous Sample Value Register

Offset address : 0CH; Word length: 3 bytes; Default value: 0

Bit	Name	Description	R/W	Reset Value
31:24	Reserved	Reserved	R	0
23:00	UA_600hz	voltage channel instantaneous sampling value, 7.2 KHz extracted to 600 Hz by a low-pass filter, which is used to calculate the flicker value by the software itself.	R	0

7.4.5 FLK_PASS (0x10)

FLKModule Password Register

Offset address: 10H; Word length: 2 bytes; Default value: 0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	FLK_PASS	The FLK_EN register can only be written to 1 when this register is written to 0x2025; this register is read to 0.	W	0

8 RTC

8.1 Overview

The RTC module provides real-time clock, oscillator temperature compensation, calendar, alarm clock, clock pulse output and other functions.

Real-time clock tracks time with separate hour, minute, and second registers. The calendar includes year, month, day, and week registers with automatic leap year and leap month correction. Clock pulse output with multiple selectable frequencies for clock calibration. Alarm/alarm functions are provided.

Integrated temperature sensor provides digital results of temperature measurements.

8.2 Features

- Provide accurate temperature values, temperature measurement accuracy of ±1℃ in the range of -25℃～70℃.
- Initial RTC calibration at room temperature
- Automatically completes the temperature compensation operation of the RTC, without CPU involvement.
- Low Power Design
- Frequency adjustment accuracy up to 0.0339ppm
- Highly stable oscillator
- RTC does not turn off in different modes and still works properly at low power consumption

- Provides clock and calendar functions: seconds, minutes, hours, date, month, year and day of the week are included in the output registers.
- Automatic leap year and leap month adjustment with 100-year (00-99) time range
- 1 alarm interrupt function, 2 timer periodic interrupt functions, 5 time interrupt functions (seconds, minutes, hours, month, day)
- Outputs uncorrected frequencies of 4 Hz, 8 Hz, 16 Hz, 32768 Hz
- Can output corrected frequency 1Hz, 1/30Hz
- Added support for RTC quadruple-curve warming, please refer to the Reynolds Micro Application Notes for detailed instructions.
- Provides RTC secondary compensation

8.3 Register Description

Base address of the RTC module

module name	physical address	mapping address
RTC	BaseAddr is: 0x4003C000	Base1

Register offset address of the RTC module

register name	address offset	Description
RTC register set		
RTC_CTRL	Offset+0x00	RTC Control Register
RTC_SC	Offset+0x04	Seconds register, write-protected
RTC_MN	Offset+0x08	Minute Register, Write Protect
RTC_HR	Offset+0x0C	Hour Register, Write Protect
RTC_DT	Offset+0x10	Day Register, Write-Protected
RTC_MO	Offset+0x14	Month Register, Write-Protect
RTC_YR	Offset+0x18	Year Register, Write Protect
RTC_DW	Offset+0x1C	Week Register, Write Protect
RTC_CNT1	Offset+0x20	Timer 1 Register
RTC_CNT2	Offset+0x24	Timer 2 Register
RTC_SCA	Offset+0x28	Seconds Alarm Register
RTC_MNA	Offset+0x2C	Minute Alarm Register
RTC_HRA	Offset+0x30	Hourly Alarm Register
RTC_IE	Offset+0x34	RTC Interrupt Enable Register
RTC_IF	Offset+0x38	RTC Status Register
RTC_TEMP	Offset+0x3C	Current temperature register, read-write, write-protected
RTC_TEMP2 (new)	Offset+0xF8	Current temperature register 2, 12bit, read-only.
RTC_CALPS (new)	Offset+0xCC	The RTC secondary compensation registers are write-protected, write 8'hA8 for the T0~T9 registers to function.
RTC_CAL_T0 (added)	Offset+0xD0	T0~T9 are 8bit registers, which do secondary compensation for the error

		of RTC on the basis of hardware automatic temperature compensation, and the scale is 0.25ppm; Compensation temperature range: T < -30 degrees
RTC_CAL_T1 (added)	Offset+0xD4	Compensation temperature range: -30 <= T < -20 deg.
RTC_CAL_T2 (new)	Offset+0xD8	Compensation temperature range: -20 <= T < -10 degrees Celsius
RTC_CAL_T3 (new)	Offset+0xDC	Compensation temperature range: -10 <= T < 0 degrees
RTC_CAL_T4 (new)	Offset+0xE0	Compensation temperature range: 0 <= T <= 10 degrees
RTC_CAL_T5 (new)	Offset+0xE4	Compensated temperature range: 35< T <= 45 deg.
RTC_CAL_T6 (new)	Offset+0xE8	Compensated temperature range: 45< T <= 55 deg.
RTC_CAL_T7 (new)	Offset+0xEC	Compensated temperature range: 55< T <= 65 deg.
RTC_CAL_T8 (new)	Offset+0xF0	Compensated temperature range: 65 < T < = 75 deg.
RTC_CAL_T9 (new)	Offset+0xF4	Compensation temperature range: T >75 degrees

8.3.1 RTC control register RTC_CTRL (0x00)

Bit	Name	Description	Read/Write Flag	Reset Value
31:12	---	read-only, not writeable	R	0
11	---	Reserved bits, do not configure	R/W	0
10	Cal_busy	RTC calibration busy. = 1 indicates that RTC calibration is in progress; = 0 indicates that RTC calibration is complete.	R	0
9	Wr_busy	RTC register write operation is busy; version A write operation needs to wait for wr_busy=0, version B/C does not.	R	0
8	WRTC	RT Register Group Write Allowed: 0: Disable RTC register write operation; 1: Allow RTC register write operation. Attention: This bit is valid for RTC register group 00~1C/3C and also valid for RTC_CTL [7:0]. Two ways to write a perpetual calendar time register: 1） In accordance with the "year, month, day, hour, minute and second" order to write, when written to the seconds register, the time began to accumulate from the moment of writing,	R/W	0

		note that this method exists before the seconds are written to the possibility of minutes flipped, so write to read out to do the checksum; 2） Write in the order of "seconds, minutes, hours, years, months and days", the seconds register is written first, the perpetual calendar counter is cleared to zero, as long as the other values are written within one second, a successful write can be guaranteed. Note that the hardware on the "year, month and day" have to do the legitimacy of the judgment, can not be written in accordance with the "day, month and year" order, can only write the "year, month and day" in succession.		
7:6	TSE	Allowable temperature sensor position 00: Automatic warming is prohibited. 01: Start automatic warming. Cyclic warming is performed according to the TCP settings. 10: Activate user temperature compensation mode 0. The temperature register can be changed and filled in by the user with the temperature value, and the user will activate temperature compensation every time the user writes to the temperature register; 11: Activate user temperature compensation mode 1, the temperature register cannot be changed, each write to the temperature register initiates a temperature compensation operation, the value of the temperature register is measured by the SOC. Note: This register works only with power-on reset.	R/W	00
5:3	TCP	Temperature compensation cycle: 000:2S 001:10S Default 010:20s 011:30s 100:1 minute 101:2 minutes 110:5 minutes 111:10 minutes	R/W	001
02:00	FOUT	000: Output prohibited 001: 1Hz output (recommended) 010: 1/30Hz output 011: 32768Hz output 100: 16Hz output 101: 8Hz output 110: 4Hz output 111: 1Hz output Note: This register only functions with a power-on reset.	R/W	000

8.3.2 Seconds register RTC_SC (0x04)

Address: 0x4003C000+ 0x04

Bit	Name	Description	Read/Write Flag	Reset Value

31:07	---	read-only, not writeable	R	0
06:00	SC	Storing the second value of the clock BCD code format, **SC[6:4]** is the tenth bit of the second value, **SC[3:0]** is the first bit of the second value, and the range of the second value is 0~59	R/W	-

8.3.3 Minute register RTC_MN (0x8)

Bit	Name	Description	Read/Write Flag	Reset Value
31:07	---	read-only, not writeable	R	0
06:00	MN	Storing the minute value of the clock BCD code format, **MN[6:4]** is the tenth digit of the minute value, **MN[3:0]** is the first digit of the minute value, and the range of the minute value is 0~59	R/W	-

8.3.4 Hour register RTC_HR (0xC)

Bit	Name	Description	Read/Write Flag	Reset Value
31:06	---	read-only, not writeable	R	0
05:00	HR	Storing the hourly value of the clock BCD code format, **HR [5:4]** is the tenth digit of the hourly value, **HR [3:0]** is the first digit of the hourly value, and the range of the hourly value is 0 to 23.	R/W	-

8.3.5 Date register RTC_DT (0x10)

Bit	Name	Description	Read/Write Flag	Reset Value
31:06	---	read-only, not writeable	R	0
05:00	DT	Stores the date value of the clock BCD code format, **DT [5:4]** is the tenth digit of the date value, **DT [3:0]** is the first digit of the date value, and the range of the date value is from 1 to 31.	R/W	-

8.3.6 Month register RTC_MO (0x14)

Bit	Name	Description	Read/Write Flag	Reset Value
31:05	---	read-only, not writeable	R	0
04:00	MO	Storing the month value of the clock BCD code format, **MO[4]** is the tenth digit of the month value, **M0[3:0]** is the first digit of the month value, and the range of the month value is 1~12	R/W	-

8.3.7 Year Register RTC_YR (0x18)

Bit	Name	Description	Read/Write Flag	Reset Value
31:08	---	read-only, not writeable	R	0
07:00	YR	Store the year value of the clock BCD code format, **YR [7:4]** is the tenth digit of the year value, **YR [3:0]** is the first digit of the year value, and the range of the	R/W	-

		year value is 0~99.		

8.3.8 Weekly register RTC_DW (0x1C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:03	---	read-only, not writeable	R	0
02:00	DW	Stores the day of the week corresponding to the current date. The counting loop for **DW [2:0]** is 0-1-2-3-4-5-6-0-1-2-....	R/W	-

Note: 04~1CH registers do not have Reset Values, and resets due to software-induced resets do not cause time information to change.

8.3.9 RTC timing register 1RTC_CNT1 (0x20)

Bit	Name	Description	Read/Write Flag	Reset Value
31:09	---	read-only, not write-only (ROW)	R	0
08	CNT1PD	= 0: 1 second timing from perpetual calendar second interrupt. = 1: Turn off timer 1, the counter will start counting again when it is turned back on (scale 1S, not related to the perpetual calendar seconds interrupt)	R/W	0
07:00	CNT	Timer1 Counter Preset Unsigned number, counting unit is 1s. When count value = (CNT+1), set RTCCNT1F flag. (Minimum interrupt can be generated every 1 second, maximum interrupt can be generated every 256 seconds) Note 1: This timer is accurate after RTC correction. Note 2: This interrupt is not synchronized with the seconds register update, i.e., this interrupt is not necessarily generated at the start of the seconds count, but can be generated at any point in the seconds count.	R/W	0

8.3.10 RTC timing register 2RTC_CNT2 (0x24)

Bit	Name	Description	Read/Write Flag	Reset Value
31:09	---	read-only, not write-only (ROW)	R	0
08	CNT2PD	= 0: timer from internal fixed 1/256S interrupt = 1: Turns off timer 2, counter will start counting again when turned back on (scale 1/256S)	R/W	0
07:00	CNT	Timer 2 Counter Preset Unsigned number, counting unit is 1/256 s. When count value = (CNT+1), set RTCCNT2F flag. (Minimum interrupt can be generated every 1/256 s, maximum interrupt can be generated every 1 s) Note: This timer is derived from a 32768Hz crystal and is uncorrected and subject to error.	R/W	0

8.3.11 Seconds alarm register RTC_SCA (0x28)

Bit	Name	Description	Read/Write Flag	Reset Value

31:07	---	read-only, not writeable	R	0
06:00	SCA	seconds alarm value BCD code format, **SCA[6:4]** is the tenth bit of the second value, **SCA[3:0]** is the first bit of the second value, and the range of the second value is 0~59	R/W	0

8.3.12 Minute alarm register RTC_MNA (0x2C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:07	---	read-only, not writeable	R	0
06:00	MNA	Minute Alarm Value BCD code format, **MNA[6:4]** is the tenth digit of the minute value, **MNA[3:0]** is the first digit of the minute value, and the range of the minute value is 0~59	R/W	0

8.3.13 Hourly alarm register RTC_HRA (0x30)

Bit	Name	Description	Read/Write Flag	Reset Value
31:06	---	read-only, not writeable	R	0
05:00	HRA	hourly rate BCD code format, **HRA [5:4]** is the tenth digit of the hourly value, **HRA [3:0]** is the first digit of the hourly value, and the range of the hourly value is 0 to 23.	R/W	0

8.3.14 RTC interrupt enable register RTC_IE (0x34)

Bit	Name	Description	Read/Write Flag	Reset Value
31:10	---	read-only, not writeable	R	0
9	RTC_1S_SEL	Seconds interrupt (bit3 definition) source selection: =0: Select the second pulse of RTC. This option synchronizes the second interruption with the time update of the almanac, and it is recommended that customers select this option. =1: according to the system clock mode: for hcmm choose pll_1hz, for non-hcmm choose RTC second pulse, note that the seconds interrupt is not synchronized with the almanac time update.	R/W	0
8	IECLKEN	The RTC interrupt generates a clock enable; When any bit of RTC_IE[8:0] is high, the interrupt module clock turns on; The interrupt module clock is turned off only when RTC_IE[8:0] are all low;	R/W	0
7	MOIE	Monthly Interrupt Enable 0 : not enabled 1 : Enable	R/W	0
6	DTIE	Date Interrupt Enable 0 : not enabled 1 : Enable	R/W	0

5	HRIE	Hourly Interrupt Enable 0 : not enabled 1 : Enable	R/W	0
4	MNIE	Minute Interrupt Enable 0 : not enabled 1 : Enable	R/W	0
3	SCIE	Seconds Interrupt Enable 0 : not enabled 1 : Enable Notes: When RTC-IE->RTC_1S_SEL is 1 and in HCMM mode, i.e., when pll_1hz is selected as the second interrupt source, the second interrupt is not synchronized with the second register update, and the second interrupt is not necessarily generated at the start of the second count, but can be generated at any moment of the second count. When RTCIE->RTC_1S_SEL is 0, i.e., the RTC seconds pulse is selected as the seconds interrupt source, the seconds interrupt is consistent with the seconds register update. It is recommended to select RTC-IE->RTC_1S_SEL as 0.	R/W	0
2	RTCCNT2IE	RTC timer 2 interrupt enable 0 : not enabled 1 : Enable	R/W	0
1	RTCCNT1IE	RTC timer 1 interrupt enable 0 : not enabled 1 : Enable	R/W	0
0	ALMIE	Alarm event interrupt enable 0 : not enabled 1 : Enable	R/W	0

8.3.15 RTC interrupt flag register RTC_IF (0x38)

Bit	Name	Description	Read/Write Flag	Reset Value
31:8	---	read-only, not write-only (ROW)	R	0
7	MOF	Month Interrupt Flag Bit 0 : Month counter is not incremented by 1 1 : Month counter plus 1 Note: Write 1 to clear	R/W	0
6	DTF	Date Interrupt Flag Bit 0 : The date counter is not incremented by 1 1 : Date counter plus 1 Note: Write 1 to clear	R/W	0
5	HRF	Hourly Interrupt Flag Bit 0 : Hour counter not incremented by 1 1 : Hour counter plus 1	R/W	0

		Note: Write 1 to clear		
4	MNF	Minute Interrupt Flag Bit 0 : Minute counter not incremented by 1 1 : Minute counter plus 1 Note: Write 1 to clear	R/W	0
3	SCF	Seconds Interrupt Flag Bit 0 : The second counter is not incremented by 1 1 : Second counter plus 1 Note: Write 1 to clear, second interrupt position for second start	R/W	0
2	RTCCNT2F	RTC timer 2 interrupt flag bit 0 : Timer 1 interrupt not generated 1 : Timer 1 interrupt generation Note: Write 1 to clear	R/W	0
1	RTCCNT1F	RTC timer 1 interrupt flag bit 0 : Timer 1 interrupt not generated 1 : Timer 1 interrupt generation Note: Write 1 to clear	R/W	0
0	ALMF	Alarm Event Flag Bit, alarm event occurs that matches the real-time clock 0 : Alarm clock incident did not occur 1 : Alarm Clock Incident Note: Write 1 to clear	R/W	0

8.3.16 Current temperature register RTC_TEMP (0x3C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:10	---	read-only, not writeable	R	0

09:00	TEMP	Current temperature value.
		Bit9 is the sign bit; Bit8~2 are integer bits; Bit1~0 are decimal bits.
		// Temp[9] Temp[8:2] Temp[1] Temp[0]
		// Symbol -128 degrees to 127 degrees 0.5 degrees 0.25 degrees
		Expression range: -128 degrees (0x200) ~ +127.75 degrees (0x1ff)
		Temperature conversion formula: if the sign bit is 0, then temperature = TEMP/4
		If sign bit is 1, temperature = (2^10- TEMP)/4
		TSE=00: Disable automatic temperature compensation. At this time, the RTC_TEMP register is invalid and the value read out is meaningless;
		TSE=01: automatic temperature compensation according to the cycle set by RTC_CTL->TCP. At this time, the RTC_TEMP register shows the temperature value of this temperature compensation cycle, and the update period of RTC_TEMP register is the temperature compensation cycle set by
			R/W	-

		RTC_CTL->TCP; TSE=10: start user temperature compensation mode 0. At this time, the RTC_TEMP temperature register can be changed, and the temperature value is filled in by the user, and the temperature compensation is started every time the user writes the temperature register; TSE=11: start user temperature compensation mode 1. at this time, the RTC_TEMP temperature register cannot be changed, and each time the temperature register is written, a temperature compensation operation is initiated, and the value of the RTC_TEMP temperature register is measured by the SOC.		

The RTC auto warm-up requires the following registers to be defined, and these register values are obtained during the customer mass production session.

1. Initial frequency deviation register RTC_DOTA0: corrects the initial frequency deviation of the crystal; (each table needs to obtain, the library function provided by Reynolds Micro can complete the operation of this register)
2. Quadratic Vertex Temperature Register RTC_XT0 (obtains crystal batch parameters, configuration option byte, written via programming interface)
3. Crystal Temperature Coefficient Register RTC_ALPHA (get crystal batch parameters, configuration option byte, write via programming interface)

8.3.17 Current temperature register 2RTC_TEMP2 (0xF8) (new)

Bit	Name	Description	Read/Write	Reset Value
31:12	---	reserve	R	0

11:00	TEMP2	Current temperature value.
		Bit11 is the sign bit; Bit10~4 are integer bits; Bit3~0 are decimal bits.
		// Temp[11] Temp[10:4] Temp[3] Temp[2] Temp[1] Temp[0]
		// Symbol -128 degrees to 127 degrees 0.5 degrees 0.25 degrees 0.125 degrees 0.0625 degrees
		Expression range: -128 degrees ~ +127.75 degrees
			R	-

8.3.18 Temperature OS register RTC_TEMPOS (0xC4) (new)

Temperature offset register in normal mode, user software manages it by itself, please configure it to 0 when not in use.

Bit	Name	Description	Read/Write Flag	Reset Value
31:06	---	reserve	R	0
05:00	TEMPOS	When TSE is equal to 01 or 11, the temperature register TEMP readout = actual calculated value + TEMPOS/4. TEMPOS is a signed number and is used to make an OFFSET correction to the temperature.	R/W	0

		Calibration range is: ±8 degrees Note: Only power down and power up reset. Still corresponds to the 10bit temperature value, i.e. the minimum scale is still 0.25 degree.		

8.3.19 Temperature OS register 2 RTC_TEMPOS2 (0x188) (new)

Temperature offset register in low-power mode, user software manages it by itself, please configure it to 0 when not in use.

Bit	Name	Description	Read/Write Flag	Reset Value
31:06	---	reserve	R	0
05:00	TEMPOS2	When TSE is equal to 01 or 11, the temperature register TEMP readout = actual calculated value + TEMPOS2/4. TEMPOS2 is a signed number and is used to make an OFFSET correction to the temperature. Calibration range is: ±8 degrees Note: Only power down and power up reset. Still corresponds to the 10bit temperature value, i.e. the minimum scale is still 0.25 degree.	R/W	0

8.3.20 Secondary Compensation Cipher Register RTC_CALPS (0xCC) (New)

Bit	Name	Description	Read/Write Flag	Reset Value
31:8	---	reserve	R	0
7:0	CALPS	The RTC secondary compensation registers are write-protected, write 8'hA8 for the T0~T9 registers to function.	R/W	0

8.3.21 Secondary segment compensation register group RTC_CAL_T0~T9 (0xD0~0xF4) (New)

Bit	Name	Description	Read/Write Flag	Reset Value
31:8	---	reserve	R	0
7:0	CAL_T0~T9	T0~T9 are 8bit registers, which do secondary compensation for the error of RTC on the basis of hardware automatic temperature compensation, and the scale is 0.25ppm; T0 compensation temperature range: T < -30° C T1 compensation temperature range: -30° C <= T <-20° C T2 compensation temperature range: -20° C <= T < -10° C T3 compensation temperature range: -10° C <= T < 0° C	R/W	0

		T4 compensation temperature range: 0° C <= T <= 10° C T5 compensation temperature range: 35° C < T <=45° C T6 compensation temperature range: 45° C < T <= 55° C T7 compensation temperature range: 55° C < T <=65° C T8 compensation temperature range: 65° C < T <=75° C T9 compensation temperature range: T >75° C		

8.4 RTC clock read/write procedure

1、 Set RTC_EN, bit 10 of the Module Enable 1 register MOD1_EN in the System Control chapter to 1.

2、 Clock reading: reads the RTC's time registers for seconds, minutes, and hours.

3、 The clock is written:

Set bit 8 of RTC_CTL, WRTC, to 1 to turn on the write enable operation.

In accordance with the "year, month, day, hour, minute and second" order to write, when written to the seconds register, the time began to accumulate from the moment of writing, note that this method exists before the seconds are written to the possibility of minutes flipped, so write to read out to do the checksum;

Or in the order of "seconds, minutes, hours, years, months and days", the seconds register is written first, the perpetual calendar counter is cleared to zero, as long as the other values are written within one second, a successful write can be guaranteed.

Note that the hardware on the "year, month and day" have to do the legitimacy of the judgment, can not be written in accordance with the "day, month and year" order, can only write the "year, month and day" in succession.

In order to enhance the reliability of the software, it is recommended to read it out for confirmation after writing.

8.5 RTC Calibration Procedure

The user only needs to calibrate the initial deviation of 32.768 KHz. The error is written through the Reynolds Micro Programmer interface or using a library function.

8.6 RTC Timer Operation Procedure

As an example, Timer 1 generates a 1S interrupt, the procedure is as follows:

1、 Set RTC_EN, bit 10 of the Module Enable 1 register MOD1_EN in the System Control chapter to 1 Clock start.

2、 Set bit 8 of RTC_CTL, WRTC, to 1 to turn on the write enable operation.

3、 Set RTC->CNT1 = 0x00; that is, to generate 1 interrupt for 1S.

4、 Set RTC->IE = 0x02; RTC timer 1 interrupt enable.

5、 Enable RTC interrupt enable, NVIC_EnableIRQ(RTC_IRQn).

6、 Write an interrupt service program:

```
void RTC_HANDLER(void)
{
    if(RTC->IF&0x02) // Timer 1
    {
```

```
        /* Start adding user code. Do not edit comment generated here */
        }
}
```

7、 A 1S interrupt can be generated after the configuration is complete.

9 WDT

The SoC has a built-in hardware watchdog to detect abnormal program execution.

9.1 Overview

The watchdog has the following features:

◎ Overflow time can be set to: 16ms, 32ms, 128ms, 512ms, 1s, 2s, 4s, 8s;

◎ The feed dog window period can be set;

A watchdog reset is generated when any of the following conditions occur:

◎ Watchdog timer counter overflow;

◎ Write data other than 0xBB to WDT_EN;

◎ Writes data to WDT_EN during the closing of the feed dog window;

◎ Write data to WDT_EN via bitband space;

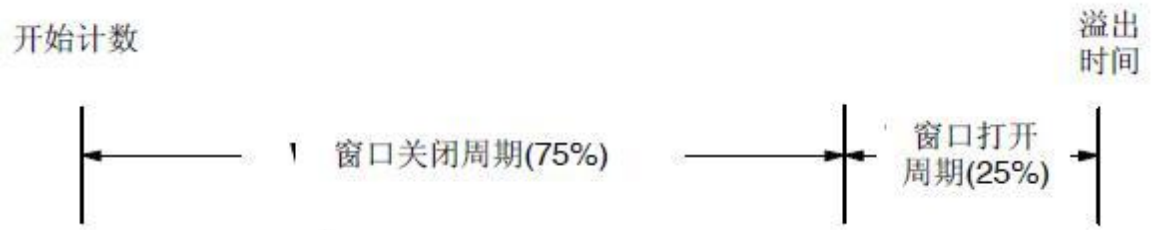
9.2 Watchdog Timer Configuration

The WDT of RN821X is a hardware watchdog, which cannot be configured directly by registers, but needs to be configured by setting "option bytes". The configuration of the watchdog has the options of interval interrupt, window open period, overflow time, CPU sleep setting, CPU debugging setting and so on.

Name	Description	Factory Default
disruption caused by an interval	0: Disable (do not enable interval interrupt) 1: Enable (generates interval interrupt when 75% of overflow events are reached)	0
Window opening cycle	0: 25% 1: 50% 2: 75% 3: 100% Write 0xBB to the WDTE register during window opening, watchdog clears and recounts; Writing 0xBB to the WDTE register during window closing generates an internal reset signal.	3
overflow time	0: 16ms 1: 32ms 2: 128ms 3: 512ms 4:1s 5:2s 6:4s 7:8s	4
CPU Sleep Setting	0: Disable (WDT is not turned on when the CPU is in sleep or deepsleep) 1: Enable (turn on WDT when CPU is in sleep or deepsleep)	0
CPU debugging	0: Disable (WDT is not enabled when the CPU is in debug state)	0

settings	1: Enable (turn on WDT when CPU is in debug state) Note: CPU in debug state means that the user stops the Cortex M0 (PC pointer stops counting) through the debug interface. It is not recommended to enable this setting if the chip is under development. If this setting is enabled, the WDT will still count when the chip is in debug state, and an interrupt will be generated when it overflows, which will cause debugging to be impossible.	

The window open period is defined as shown below, using the 25% window open period as an example:



9.3 Register Description

WDT register base address

module name	physical address	mapping address
WDT	0x40030000	0x40030000

WDT register offset address

register name	address offset	Description
WDT_EN	0x0	Enable Register

WDT_EN (0x0)

Bit	Name	Description	Read/Write Flag	Reset Value
31:9	---	read-only, not writeable	R	0
8	WR_BUSY	WDT busy Version A: WDT_EN is not writable when WR_BUSY = 1; the WDT_EN register can be written only when WR_BUSY = 0 Other versions: feeding the dog has nothing to do with the BUSY bit.	R	0
7:0	WDTE	Write 0xBB to clear the watchdog timer and start the counting operation again. Reset signal generation sets this register to 0x55	R/W	55

9.4 WDT Operating Procedure

1、 Configure bit 9 of the System Control Chapter Module Enable 1 register MOD1_EN to 1 to turn on the WDT APB clock.

2、 The WDT is configured by default to start up with a timer overflow time of 1S and a window open period of 75%. The user program may not configure the WDT initialization.

3、 Feed dog operation: WDT->EN = 0xbb;

4、 WDT default is to turn off WDT after sleep, WDT clock in MOD1_EN may not be turned off, if it is turned

off, it is necessary to wait for bit 8 WR_BUSY of WDT_EN to be 0 before turning off WDT clock.

5、 When the hardware emulation stops the program from running, the WDT counting is also suspended without affecting the hardware emulation.

6、 Done.

Suggestions for use:

Since the WDT of RN821x has very low power consumption, the additional power consumption added by turning on the WDT when the CPU is hibernating is less than 1uA. From the perspective of higher system reliability, it is recommended that customers turn on the WDT when the CPU is hibernating, and the second timer in the RTC can be used to wake up the CPU for the dog feeding operation.

10 LCD

The SoC has a built-in segmented LCD controller.

10.1 Overview

The LCD controller has the following features:

- ◎ Supports up to 4x40, 6x38, 8x36 LCD drive modes;
- ◎ Supports both Class A and Class B driver waveforms;
- ◎ Supports 1/3 and 1/4 bias ratios;
- ◎ Supports static, 1/2, 1/3, 1/4, 1/6, 1/8 duty cycles;
- ◎ Supports 16 levels of contrast drive mode;
- ◎ Supports charge pump and internal resistor series divider to realize LCD Bias voltage;

10.1.1 Scan Clock Frequency

The LCD waveform scanning frequency comes from dividing the frequency of the LOSC (which has a frequency of 32768 Hz). The crossover frequency coefficient is configured through register LCD_CLKDIV.

Generally, the frame refresh frequency of the LCD screen is required to be slightly greater than 60 Hz. The frame rate marked in green in Table 8-1 is the frame rate for normal use.

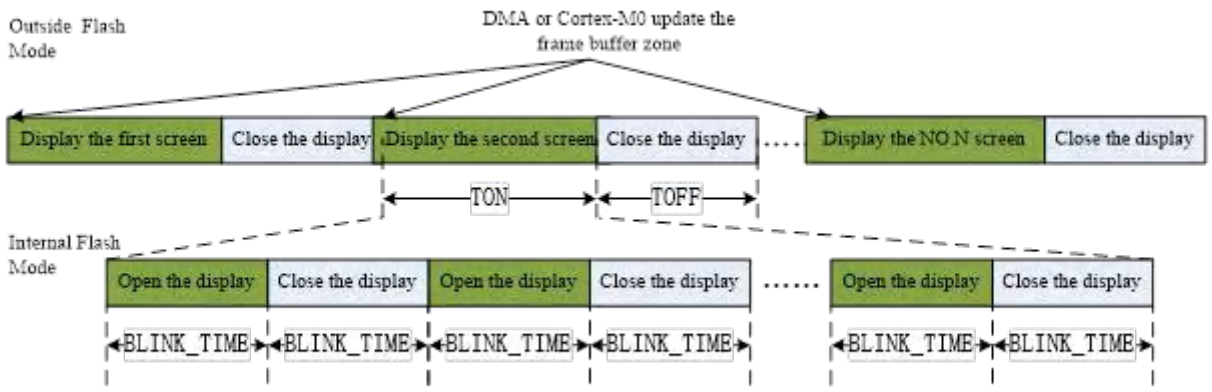
Table 8-1 LCD Scanning Frequency and Frame Rate

LCD_CLKDIV	scanning frequency	Static Duty Cycle	1/2 duty cycle	1/3 duty cycle	1/4 duty cycle	1/6 duty cycle	1/8 duty cycle
0xff	64Hz	64Hz	32Hz	21.3Hz	16Hz	10.7Hz	8Hz
0x7f	128Hz	128Hz	64Hz	42.7Hz	32Hz	21.3Hz	16Hz
0x54	192.8 Hz	192.8 Hz	96.4Hz	64.3Hz	48.2Hz	32.1Hz	24.0Hz
0x3f	256Hz	256Hz	128Hz	85.3Hz	64Hz	42.7Hz	32Hz
0x2a	381.3 Hz	381.3 Hz	190.5 Hz	127.0 Hz	95.3 Hz	63.5Hz	47.6 Hz
0x1f	512Hz	512Hz	256Hz	170.7 Hz	128Hz	85.3Hz	64Hz

10.1.2 Blink Mode

The LCD supports two blinking modes: internal blinking and external blinking. Both modes can be enabled at the same time.

Figure 8-1 LCD Blinking Method



As shown in Figure 8-1, LCD enable turns the display on for the length of time defined in the TON bit field of the LCD_BLINK register, and subsequently turns the display off for the length of time defined in the TON bit field of the LCD_BLINK register.

The LCD can issue interrupt requests or DMA requests when the display is turned on and off. The user can use these events to update the frame buffer.

In conjunction with the DMA's wrap-around feature, automatic rotation of multiple frame buffers can be realized.

10.1.2.1 Internal Blink Mode

The LCD supports insertion of a blink mode during a display of the length specified by the TON bit field of the LCD_BLINK register. The blinking interval is given by the BLINK_TIME bit field of the LCD_BLINK register. When BLINK_TIME is 0, internal blink mode is disabled; when BLINK_TIME is not 0, TON must be an even multiple of BLINK_TIME.

10.1.2.2 External Blink Mode

The blink function is enabled when TOFF in the LCD_BLINK register is not 0. When Blink Mode is enabled, the blink frequency is determined according to the values of TON and TOFF in the LCD_BLINK register.

10.1.3 LCD Driver Waveforms

The LCD drive waveform is related to the display waveform type, duty cycle and bias ratio.

Display waveform type A is line inversion drive mode, i.e., complete the alternation of positive and negative drive once in each frame; display waveform type B drive is frame inversion mode, i.e., complete the alternation of positive and negative drive once in every two frames. When the duty cycle is large, the display effect will be better with the display waveform type B drive.

The user needs to select the duty cycle of the LCD output waveform according to the number of COMs required for the application:

- 1 COM: Selects the static duty cycle, using only COM0;
- 2 COM: Select 1/2 duty cycle, use COM0, COM1;
- 3 COM: Select 1/3 duty cycle, use COM0 ~ COM2;
- 4 COM: Select 1/4 duty cycle and use COM0 ~ COM3;
- 6 COM: Select 1/6 duty cycle, use COM0 ~ COM5;
- 8 COMs: Select 1/8 duty cycle and use COM0 to COM7;

10.1.3.1 Type A drive waveform

Figure 8-2 LCD Driver Waveform (1/4 Duty, 1/3 Bias, Type A)

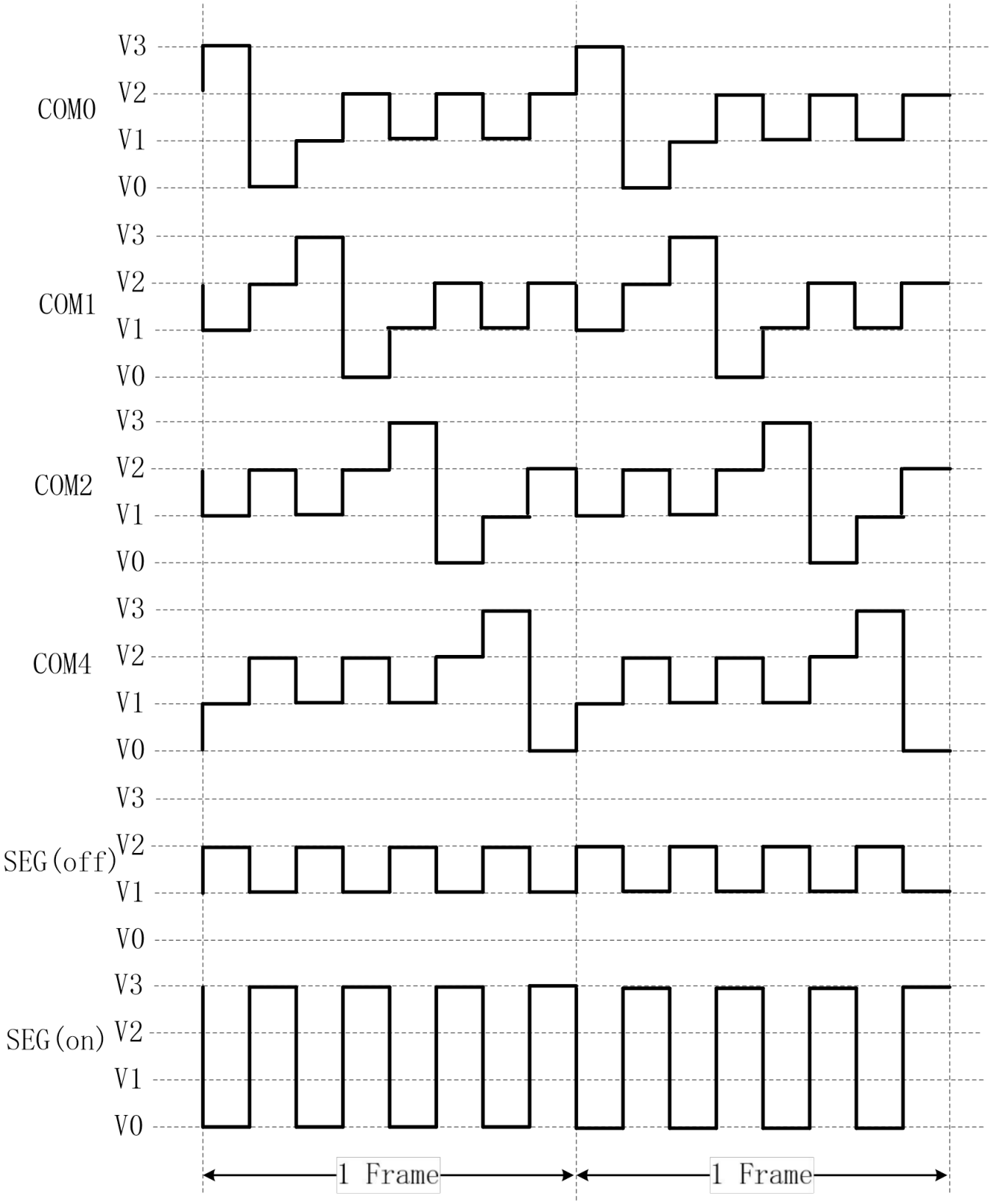
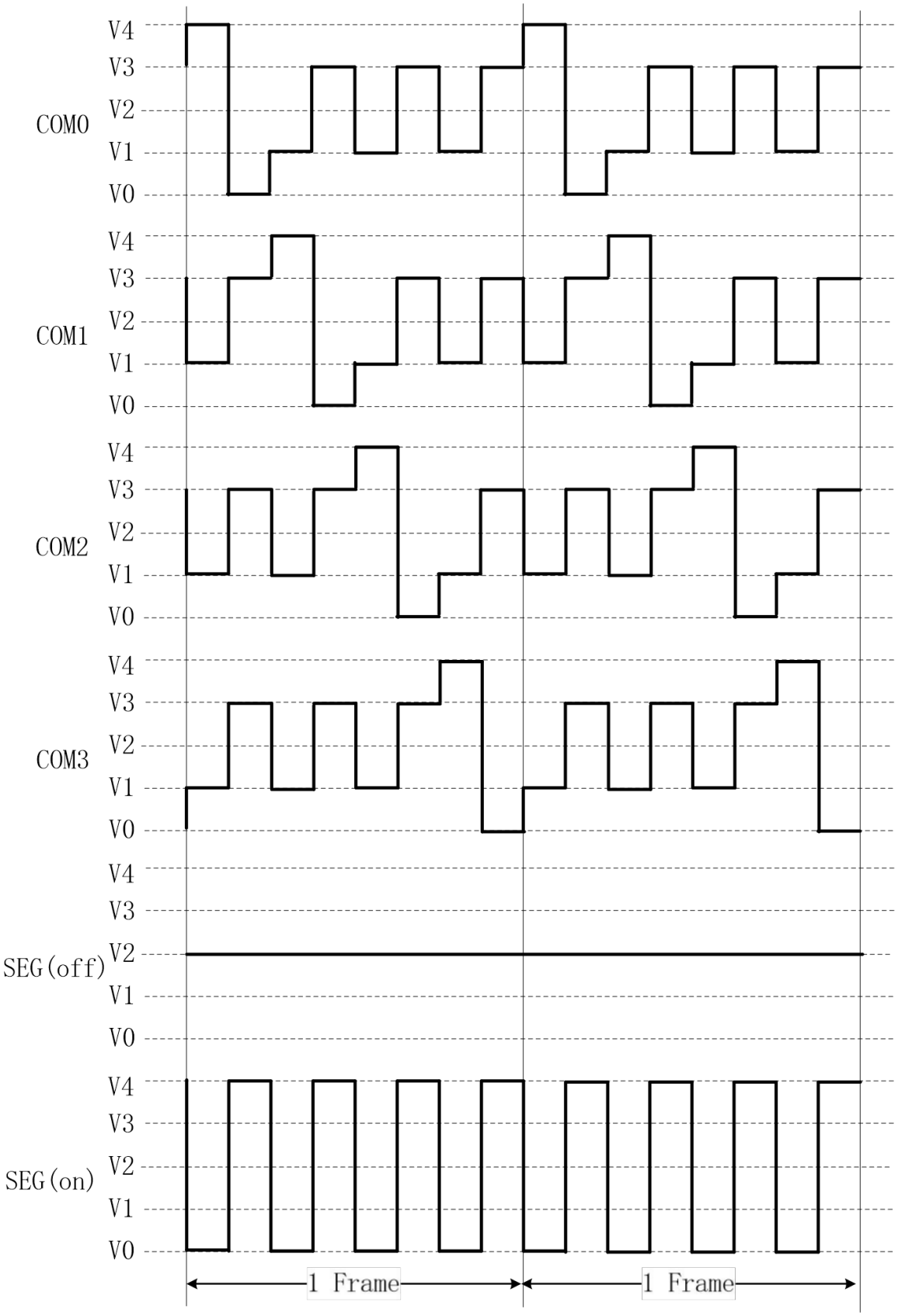


Figure 8-3 LCD Driver Waveform (1/4 Duty, 1/4 Bias, Type A)



10.1.3.2 Type B drive waveform

Figure 8-4 LCD Driver Waveform (1/4 Duty, 1/3 Bias, Type B)

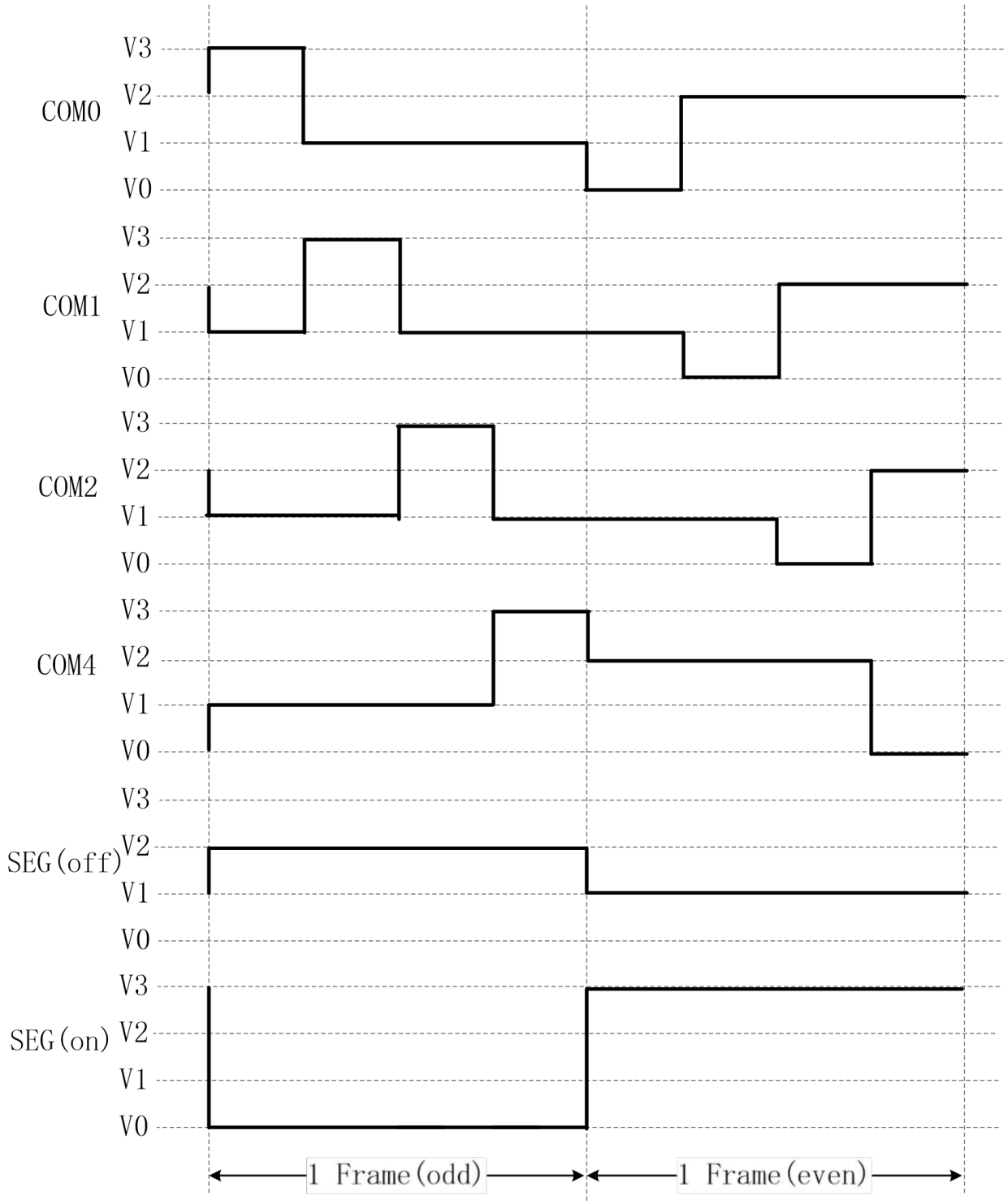
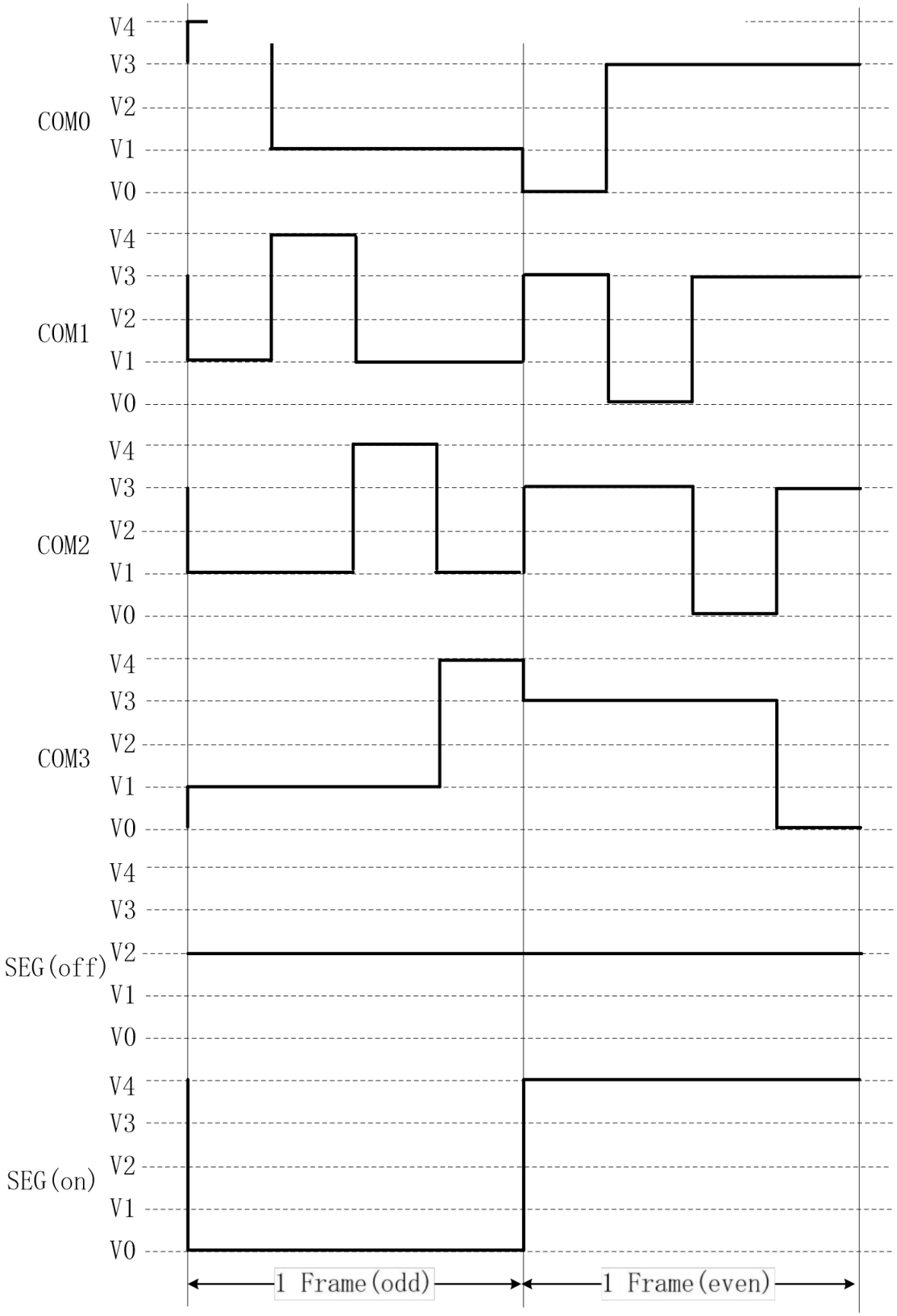


Figure 8-5 LCD Driver Waveform (1/4 Duty, 1/4 Bias, Type B)



10.1.4 LCD bias voltage - Charge pump method

The LCD bias voltage can be supplied by Charge Pump. 4 voltages (Va, Vb, Vc, Vd) need to be generated by the Charge Pump to satisfy the 1/4 bias ratio application. For different bias ratio settings, the Charge Pump outputs different voltage patterns as shown in Table 8-2.

Table 8-2 LCD drive voltage and bias ratio relationship

bias voltage ratio	Grayscale Selection	Va	Vb	Vc	Vd	Vd (MAX)
1/3 bias ratio	BIASLVL[5] = 0	Va = Vref*(32+BIASLVL[4:0])/63	Vb = Va	Vc = 2*Va	Vd = 3*Va	3.75 V
	BIASLVL[5] = 1	Va = Vref*(1 + BIASLVL[4:0]/63)	Vb = Va	Vc = 2*Va	Vd = 3*Va	5.59 V
1/4 Bias Ratio	BIASLVL[5] = 0	Va = Vref*(32+BIASLVL[4:0])/63	Vb = 2*Va	Vc = 3*Va	Vd = 4*Va	5.0 V
	BIASLVL[5] = 1	Va = Vref*(1 + BIASLVL[4:0]/63)	Vb = 2*Va	Vc = 3*Va	Vd = 4*Va	6.032V

The maximum value of Vd required for the LCD is 5.2 V. When selected as 1/4 bias ratio, the LCD controller automatically clamps BIASLVL[5:0] to 6'h2d when BIASLVL[5:0] is set greater than 6'h2d.

The LCD selects LBGR as the reference by default, and the typical value of the LBGR output is 1.27V.

The 1/3 and 1/4 bias ratio application voltage selections are shown in Figure 8-6:

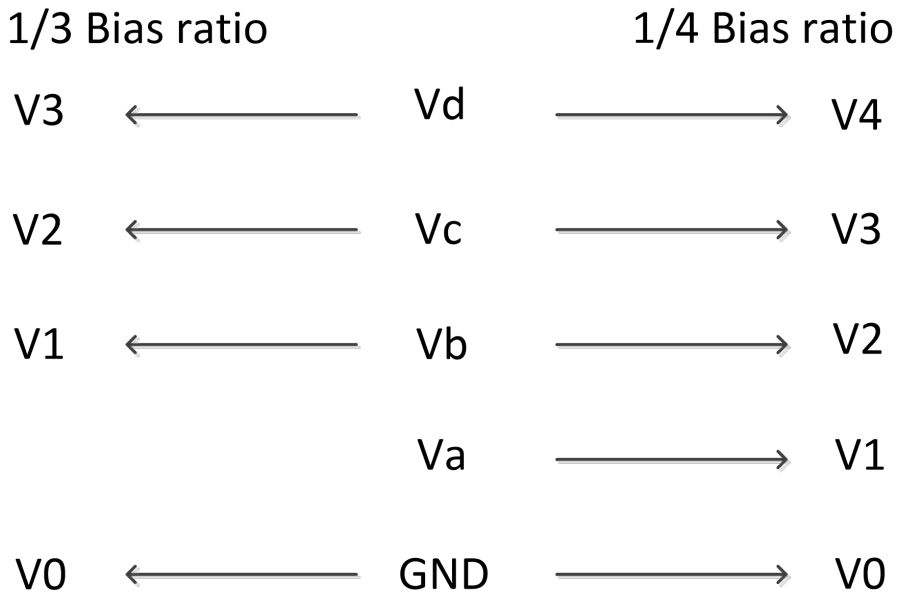


Figure 8-6 Bias Voltage Selection

10.1.5 LCD bias voltage-resistor string method

Built-in LDO, output 2.7~3.6V adjustable, step 60mV, support 3.0V and 3.3V LCD screen; internal resistor string is divided into two grades of large and small resistor strings, small resistor 20k, large resistor 220k; small resistor time-opening program, need to be connected to an external 470nf capacitor filter.

The small resistor time-sharing on and large and small resistor switching schemes are only for when the drive waveform selection is TYPE B. When the drive waveform selection is TYPE A, the selection is small resistance

always drive.

10.1.6 LCD frame buffer mapping

The LCD_BUFx register is mapped to LCD screens with different segment specifications as shown below.

i. When 8COM is used, 36 LCD_BUFs are needed to support a maximum of 8*36 LCD screens.

LCD_BUF[i] i=0~35 SEG max 36	SEG[i+4] COM7	SEG[i+4] COM6	SEG[i+4] COM5	SEG[i+4] COM4	SEG[i+4] COM3	SEG[i+4] COM2	SEG[i+4] COM1	SEG[i+4] COM0

ii. When 6COM is used, 38 LCD_BUFs are required, the maximum can support 6*38 LCD screen.

LCD_BUF[i] i=0~37 SEG Maximum 38	-	-	SEG[i+2] COM5	SEG[i+2] COM4	SEG[i+2] COM3	SEG[i+2] COM2	SEG[i+2] COM1	SEG[i+2] COM0

iii. When using 4COM/3COM/2COM/1COM, 20 LCD_BUFs are required, and can support up to 4*40 LCD screens.

LCD_BUF[i] i=0~19 SEG max 40	SEG[2*i+1] COM3	SEG[2*i+1] COM2	SEG[2*i+1] COM1	SEG[2*i+1] COM0	SEG[2*i] COM3	SEG[2*i] COM2	SEG[2*i] COM1	SEG[2*i] COM0

10.2 Register Description

LCD register base address

module name	physical address	mapping address
LCD	0x40048000	0x40048000

LCD register offset address

register name	address offset	Description
LCD_CTL	0x0	LCD Control Register
LCD_STATUS	0x4	LCD Status Register
LCD_CLKDIV	0x8	LCD Clock Control Register
LCD_BLINK	0xc	LCD blinking control register
LCD_PS (modified)	0x10	LCD PUMP Establishment Time Register
LCD_RESCTL	Offset+0x14	LCD Internal Resistor String Control Register
LCD_BUF[i]	0x20+i*1 (i=0-37)	LCD data registers (total of 38 8-bit registers)

10.2.1 LCD Control Register LCD_CTL (0x0)

Bit	Name	Description	Read/Write Flag	Reset Value
31:14	---	read-only, not writeable	R	0
13	reservations	Reserved register bits, user do not write 1.	R/W	0
12	PWD_PUMP	LCD PUMP switch:	R/W	0

		0: PUMP is turned on, LCD voltage is generated by internal PUMP. 1: Turn off the PUMP and use the resistor string voltage divider scheme		
11	TYPE	LCD Drive Type Select 0: Type A 1: Type B	R/W	0
10:5	BIASLVL	LCD Bias Voltage Regulation Controls the Charge Pump to output different amplitudes of voltage to control the contrast of the LCD.	R/W	0
4	BIAS	LCD Bias Control 0:1/3 Bias 1:1/4 Bias	R/W	0
3:1	DUTY	LCD Duty Cycle Control 000: Static output (COM0) 001: 1/2 duty cycle (COM0~1) 010: 1/3 duty cycle (COM0~2) 011: 1/4 duty cycle (COM0~3) 100: 1/6 duty cycle (COM0~5) 101: 1/8 duty cycle (COM0~7) Other:Reserved	R/W	0
0	EN	LCD module enable 0: LCD module off 1: LCD module enable	R/W	0

10.2.2 LCD Status Register LCD_STATUS (0x4)

Bit	Name	Description	Read/Write Flag	Reset Value
31:7	---	read-only, not writeable	R	0
6	LCD_BUSY	LCD Busy Bit 0: Not busy 1: Busy Note: When LCD_BUSY is 1, LCD_CTRL (except EN Bit), LCD_CLKDIV, LCD_BLINK, LCD_PS registers cannot be modified.	R	0
5	---	reservations	R/W	0
4	---	reservations	R/W	0
3	IRQOFFEN	Display Off IRQ Enble Bit 0: not enabled 1: Enabling	R/W	0
2	IRQONEN	Display On IRQ Enble Bit 0: not enabled 1: Enabling	R/W	0
1	DOFF	Display Off Pending Bit 0: No interrupt event	R/W	0

		1: Set when display goes from on to off Note: Write 1 to clear		
0	DON	Display On Pending Bit 0: No interrupt event 1: Set when the display changes from off to on Note: Write 1 to clear	R/W	0

10.2.3 LCD Clock Control Cegister LCD_CLKDIV (0x8)

Bit	Name	Description	Read/Write Flag	Reset Value
31:8	---	read-only, not writeable	R	0
7:0	CLKDIV	LCD Clock division factor LCD_CLK=fosc/(2*(CLKDIV+1)) (fosc is 32768Hz)	R/W	0

10.2.4 LCD Blink Control Register LCD_BLINK (0xC)

Bit	Name	Description	Read/Write Flag	Reset Value
31:26	---	read-only, not writeable	R	0
25:18	BLINK_TIME	The step size is 0.25s, supporting 0~63.75s Sets the time for the TON display cycle to light up and go off = 0.25*BLINK_TIME. Note: When set to 0, it means that the TON will be on for a long time during the TON display period without blinking. When set to a value greater than 0, TON must be 2n times BLINK_TIME (n is an integer greater than 0).	R/W	0
17:9	TOFF	The step size is 0.25s, supporting 0~127.5s, when using this function please set it to >>3s; the actual time is: 0.25s*TOFF	R/W	0
8:0	TON	The step size is 0.25s, supporting 0~127.5s, when using this function please set it to >>3s; the actual time is: 0.25*TON	R/W	0

10.2.5 LCD Charge Pump Build-up Time Register LCD_PS (0x10) (modified)

Bit	Name	Description	Read/Write Flag	Reset Value
31:16	---	read-only, not writeable	R	0
15:0	PS	LCD PUMP Setup time Time = Tosc * (PS+4) (Tosc is 30.5uS) Note: The user does not need to configure this register. Expanded to 16bit for V2	R/W	0xccc

10.2.6 LCD Internal Resistor String Control Register LCD_RESCTL (0x14)

Offset=0x14

Bit	Name	Description	Read/Write Flag	Reset Value
31:13	---	reserve	R	0
12:9	LDOS	LDO output level selection signal The LDO output is used as the LCDVD voltage and is divided by a resistor to produce LCDVC, LCDVB, and LCDVA;		0101

<table>
<tr><td></td><td></td><td>The LDO output level ranges from 2.7V to 3.6V in 16 steps with a step of 0.06V;
<table>
<tr><th>LDOS Configuration</th><th>LDO output voltage V</th></tr>
<tr><td>0000</td><td>2.7</td></tr>
<tr><td>0001</td><td>2.76</td></tr>
<tr><td>0010</td><td>2.82</td></tr>
<tr><td>0011</td><td>2.88</td></tr>
<tr><td>0100</td><td>2.94</td></tr>
<tr><td>0101</td><td>3</td></tr>
<tr><td>0110</td><td>3.06</td></tr>
<tr><td>0111</td><td>3.12</td></tr>
<tr><td>1000</td><td>3.18</td></tr>
<tr><td>1001</td><td>3.24</td></tr>
<tr><td>1010</td><td>3.3</td></tr>
<tr><td>1011</td><td>3.36</td></tr>
<tr><td>1100</td><td>3.42</td></tr>
<tr><td>1101</td><td>3.48</td></tr>
<tr><td>1110</td><td>3.54</td></tr>
<tr><td>1111</td><td>3.6</td></tr>
</table>
LDO output 3.0V during reset</td><td></td><td></td></tr>
<tr><td>8</td><td>FCC</td><td>Fast charging control:
0: Turn off the fast charging function
1: Turn on the fast charging function;
Internal resistor voltage divider is selected, node voltage external 470nf capacitor, when LCD module is turned on, the internal resistor is adjusted to 5k and held for 100ms to accomplish fast charging of the capacitor.</td><td></td><td>0</td></tr>
<tr><td>7</td><td>RES_AO</td><td>Resistor String Timing Drive Switch
0: Resistor series split-time drive, generate drive signal according to RES _DT and RES _FT
1: The resistor string is always driven and the RES _DT and RES _FT configurations are invalid.
When TYPE A is selected, RES _AO is constant 1.</td><td></td><td>1</td></tr>
<tr><td>6:4</td><td>RES_DT</td><td>Resistor string divider method, 20k resistor drive time configuration during swipe cycle
Drive time Td=(RES _DT[2:0]+1)* Tosc (Tosc is 30.5uS).</td><td></td><td>000</td></tr>
<tr><td>3:2</td><td>RES_FT</td><td>Resistor string divider method, 20k resistor drive count configuration during swipe cycle
00: 1 drive
01: Drive 2 times
10: Drive 3 times
11: Driven 4 times</td><td></td><td>00</td></tr>
</table>

1	RSM	Internal resistor divider resistor mode selection signal 0 Small resistor + open, 20k resistor on in minutes, 200k resistor always shorted 1 Resistor switching between large and small, 20k and 200k resistor switching in minutes		0
0	IRSN	Resistor divider mode selection 0 Internal resistor divider mode 1 Reservation Note: If resistor divider mode is used, this bit must be configured to 0, configuring it to 1 has no meaning	R/W	1

If you choose the resistor divider method, it is recommended that LCD_RESCTL be configured as follows:

Typical 3V screen, LCD->RES_CTRL register configured value is: 0xb14;

For a typical 3.3V screen, the LCD->RES_CTRL register is configured with the value: 0x1514.

10.2.7 LCD data register LCD_BUFx (x=0~34) (address 0x20- 0x41)

Bit	Name	Description	Read/Write Flag	Reset Value
31:8	---	read-only, not writeable	R	0
7:0	LCD_BUFx	The LCD screen SEG displays the data, and the physical meaning of each bit is as follows: 0: The corresponding display unit is not displayed 1: Corresponding display unit display	R/W	0

11 Timer (modified)

The SoC has two built-in 32-bit timers. Each timer can work completely independently; the timers do not share any resources with each other and can operate synchronously.

The timer is suitable for a wide range of uses and has the following features:

- ◎ interval timing
- ◎ square wave output
- ◎ External/internal event counting
- ◎ Single pulse output
- ◎ PWM output
- ◎ Pulse Width Measurement

11.1 Overview

The timer has the following features:

- ◎ 2 32-bit timers each:
  - ■ Has a 32-bit incremental auto-reload counter;
  - ■ With 16-bit programmable prescaler, the crossover coefficient is selectable from 1 to 65535;
  - ■ Supports dynamic access to count values;
  - ■ Supports free-running mode;
  - ■ Supports a single run;
- ◎ Each timer has 2 capture/compare channels, each of which can be configured independently of the other:
  - ■ Input Capture;
  - ■ Output Comparison;
  - ■ Single pulse output;
  - ■ Complementary PWM:
    - ◆ Deadband length is programmable:
      - ● The deadband lengths of the two edges can be set independently;
      - ● Output polarity is configurable;
    - ◆ Configurable failure handling:
      - ● Output Failure;
      - ● Output Clear;
      - ● Output tristate;
- ◎ from the schema support:
  - ■ External reset and restart;
  - ■ External sector control;
- ◎ Input Capture Support:
  - ■ Rising along the capture;
  - ■ Descending along the capture;
  - ■ Double-edge capture;
  - ■ Periodicity Measurement;
  - ■ Pulse width measurement;
  - ■ Optional filtering;
- ◎ The output is more supportive:

- Three-state output;
- Reverse output;
- Fixed level output;
- Pulse width configurable pulse output;
- Comparison registers are always updated;

◎ Support for interruptions:

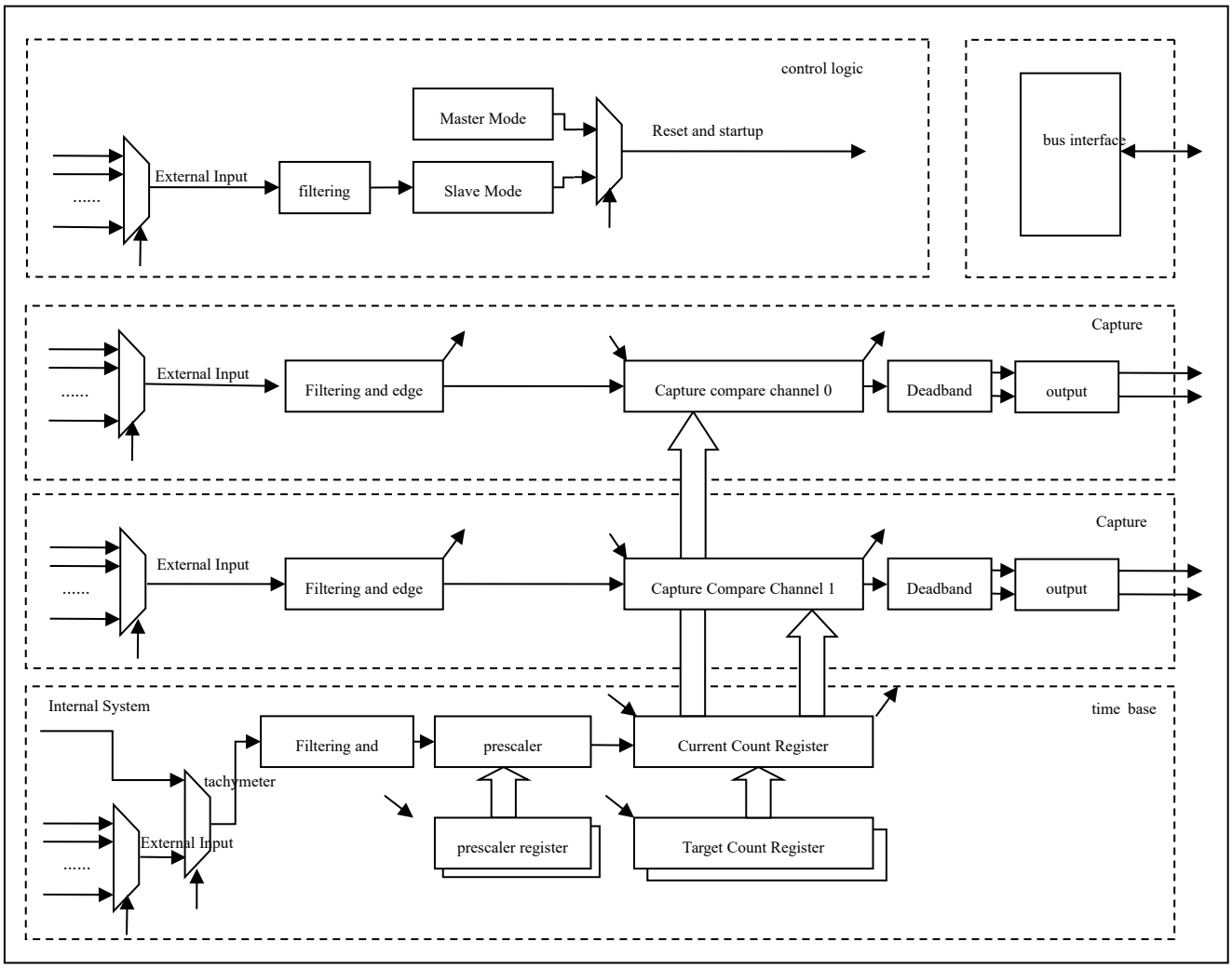
- Count overflow;
- Input Capture;
- Output Comparison;

◎ Flexible complementary PWM waveform modulation (TC1 CM1 channels only)

- The modulation period parameter is configurable;
- Supports DMA read parameters
- Complementary PWM output with configurable deadband

11.2 Functional Block Diagram

Please refer to the following diagram for the functional block diagram of the counting timer. Each counting timer contains one 32-bit counter and four 32-bit capture/compare channels.



11.3 PWM modulation control mode (new)

11.3.1.1 DMA control mode

The length of the General Control Mode PWM parameter table is K (in Word), where [31:16] denotes the number of level active cycles (N_Duty), and [15:0] denotes the number of system clock cycles corresponding to 1 PWM cycle (N_Pwm).

Waveform generation takes the waveform cycle as the cycle processing unit, each waveform cycle reads the parameter information of PWM parameter table from 0 to K-1 in sequence, and dynamically updates the configuration parameters of each PWM cycle to generate the corresponding PWM output signals, and one waveform cycle corresponds to K PWM cycles; after the end of the current waveform cycle, it will continue to generate the signal of the next waveform cycle in a cycle.

The actual count clock period is N_Pwm + 1 and the effective level count period is N_Duty +1.

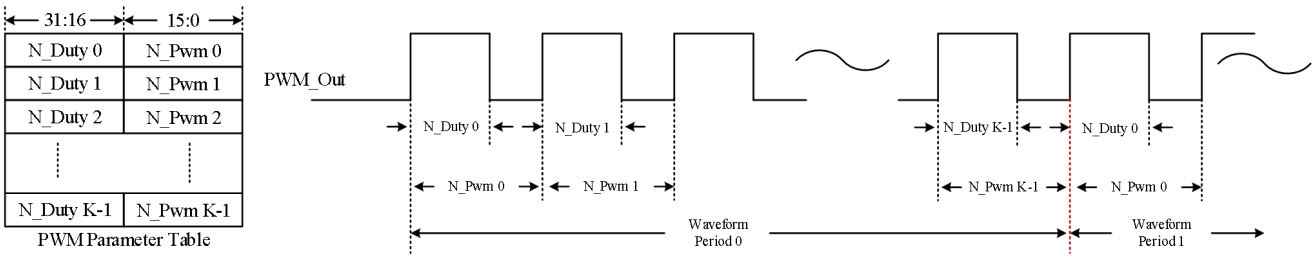


Fig. General control mode PWM parameter table vs. PWM output signal

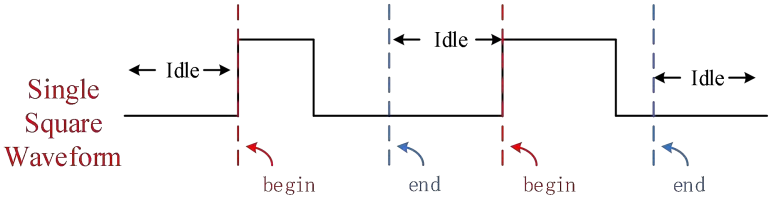
11.3.1.2 Software Control Mode

Through the registers as PWM parameter table, PWM_CNT register [15:0] indicates N_Pwm and TC1_CCD1 register indicates N_Duty.

Scenario 1: Single Square Wave

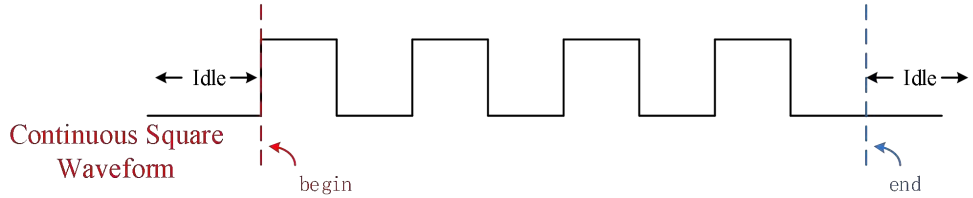
Input 1 parameter at a time and send a square wave.

First enter 1 parameter to start the module, send a square wave and turn off the module, then enter the parameter again to start.



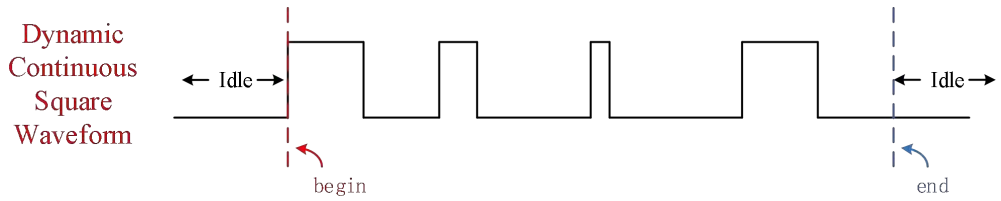
Scenario 2: Continuous Square Wave

Input 1 parameter, start, output square wave of specified length or end output by user



Scenario 3: Dynamic Continuous Square Wave

Enter 1 parameter, start, and write a new data per interrupt according to PWM_STA.BUFVLD interrupt.



11.4Register Description

Module register base address

module name	physical address	mapping address
TC0	0x40010000	0x40010000
TC1	0x40014000	0x40014000

TC module register offset address

register name	address offset	Description
TC_CNT	0x0	Current count value indication
TC_PS	0x4	prescaler register
TC_DN	0xC	Target Count Register
TC_CCD0	0x14	Capture compare channel 0 data register
TC_CCD1	0x18	Capture Compare Channel 1 Data Register
TC_CCFG	0x1C	Clock Configuration Register
TC_CTRL	0x20	control register
TC_CM0	0x24	Capture Compare Channel 0 Mode Register
TC_CM1	0x28	Capture Compare Channel 1 Mode Register
TC_IE	0x2C	Interrupt Enable Register
TC_STA	0x30	status register

11.4.1 Current count value register TC_CNT (0x00)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	CNT	Current count value	R	0

11.4.2 Prescaler register TC_PS (0x04)

Bit	Name	Description	Read/Write Flag	Reset Value
31:16	----	read-only, not writeable	R	0
15:0	PS	Crossover coefficient, crossover value (PS+1), 0 for no crossover	R/W	0

11.4.3 Target Count Value Register TC_DN (0x0C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	DN	Target count value, actual count clock period is DN+1	R/W	0

11.4.4 Capture Compare Channel 0 Data Register TC_CCD0 (0x014)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	CCD	Capture of comparison data	R/W	0

Note: When channel 0 is configured for capture function (i.e., the CCM bit field of the TC_CM0 register is 0), the TC_CCD0 register is not writable

11.4.5 Capture Compare Channel 1 Data Register TC_CCD1 (0x018)

Bit	Name	Description	Read/Write Flag	Reset Value
31:0	CCD	Capture of comparison data	R/W	0

Note: When channel 1 is configured for capture function (i.e., the CCM bit field of the TC_CM1 register is 0), the TC_CCD1 register is not writable

11.4.6 Clock Configuration Register TC_CCFG (0x01C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:24	---	read-only, not writeable	R	0
23:16	FLTOPT	External Input Clock Filter Parameter Setting sets the number of clock cycles for filtering.	R/W	0
15	---	read-only, not writeable	R	0
14:13	ECLKMODE	External input clock mode: 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved (equivalent to double border)	R/W	0
12:8	CS	External Input Clock Selection: 0: UART0 RXD 1: UART1 RXD 2: UART2 RXD 3: UART3 RXD 4: Output outn[0] of another timer (TC0 or TC1) 5: Output outp[0] of another timer (TC0 or TC1) 6: Output outn[1] of another timer (TC0 or TC1) 7: Output outp[1] of another timer (TC0 or TC1) 8: UART4 RXD 9: UART5 RXD 10:7816_0 Input P41 11:7816_1 Input P42 12:7816_1 Input P43 13 to 15: Reservations 16: sf_out 17: qf_out 18: pf_out 19: rtc_out 20: p1[0] external IO port	R/W	0

		21: p1[1] external IO port 22: p1[2], p5[2] external IO ports 23: p1[3], p5[3] external IO ports 24: p1[4], p5[4] external IO ports 25: p1[5], p5[5] external IO ports 26: p1[6], p5[6] external IO ports 27: p1[7], p5[7] External IO ports 28: p3[0] external IO port 29: p3[1] external IO port 30: p3[3] external IO port 31: p3[5] external IO port		
7:2	---	read-only, not writeable	R	0
1	FLTEN	External Input Clock Filter Enable 0: not enabled 1: Enabling	R/W	0
0	CM	Count clock source selection: 0: Internal system clock 1: External input clock (clock source selected by CS)	R/W	0

11.4.7 Control register TC_CTRL (0x020)

Bit	Name	Description	Read/Write Flag	Reset Value
31:29	---	read-only, not writeable	R	0
28	DBGSTBDIS	Counter Count Enable for debugging: 0: not enabled (counter stops counting when CPU is in debug state) 1: Enable (counter continues to count when CPU is in debug state) Note: CPU in debug state means that the user stops the Cortex M0 (PC pointer stops counting) through the debug interface.	R/W	0
27	SLVDE	Slave mode DMA request enable: 0: not enabled 1: Enabling	R/W	0
26	CC1DE	Capture Compare Channel 1 DMA Request Enable: 0: not enabled 1: Enabling	R/W	0
25	CC0DE	Capture Compare Channel 0 DMA Request Enable: 0: not enabled 1: Enabling	R/W	0
24	OVDE	Overflow DMA Request Enable: 0: not enabled 1: Enabling	R/W	0
23:21	---	read-only, not writeable	R	0
20	SLVGATELVL	Slave mode gated mode active level:	R/W	0

		0: Effective level is low 1: Effective level is high		
19:12	SLVFLTOPT	Input filter parameters from mode	R/W	0
11:10	SLVTRGMODE	Select from the Mode Control mode: 00: Rising edge clear internal counter 01: Falling edge clear internal counter 10: Double edge clear internal counter 11: Gated mode (internal counter counts when external input signal is a valid level)	R/W	0
9:5	SLVCHANSEL	Input event selection from outside the mode: Consistent with the external input clock definition defined in the CS bit field of the Clock Configuration Register (0x01C).	R/W	0
4	OPS	Single count mode selection: 0: Do not enable single count mode (count overflow does not stop and counts cyclically); 1: Enable single count mode (stop after count overflow)	R/W	0
3	SLVFLTEN	Input event filter enable from outside the mode: 0: not enabled 1: Enabling	R/W	0
2	SLVEN	Slave mode enable: 0: not enabled 1: Enabling	R/W	0
1	---	read-only, not write-only (ROW)	R	0
0	START	Timer start: 0: Stop 1: Initiation	R/W	0

11.4.8 Capture Compare Channel 0/1 Mode Register TC_CM0/1 (0x024 and 0x028)

Bit	Name	Description	Read/Write Flag	Reset Value
31:30	---	read-only, not writeable	R	0
29	DFTLVL	Compare Output Default Level: 0: low level 1: High level	R/W	0
28	EFELVL	Compare the active level of the output: 0: low level 1: High level	R/W	0
27:25	OM	Compare output modes: 000: No output (tri-state) 001: Set to active level 010: Set to invalid level 011: Flip 100: forced to active level	R/W	0

		101: Forced to invalid level 110: PWM mode 1 111: PWM mode 2		
24:20	CS	Capture external input event selection: Consistent with the external input clock definition defined in the CS bit field of the Clock Configuration Register (0x01C).	R/W	0
19	FLTEN	Capture external input event filter enable: 0: not enabled 1: Enabling	R/W	0
18:11	FLTOPT	Capture external input event filter parameters	R/W	0
10:9	CPOL	Captures external input event polarity selection: 00: Rising edge 01: Falling edge 10: Double Edge 11: Reservations	R/W	0
8:3	DL	Compare output deadband length (only supports PWM mode 1 and PWM mode 2, this bit is invalid in other modes)	R/W	0
2	DIEN	Compare Output Deadband Insertion Enable: (only support PWM Mode 1 and PWM Mode 2, this bit is invalid in other modes) 0: not enabled 1: Enabling	R/W	0
1	CCM	Capture Compare Mode Selection: 0: Capture 1: Comparison	R/W	0
0	ENABLE	Channel Enable: 0: not enabled 1: Enabling	R/W	0

11.4.9 Interrupt Enable Register TC_IE (0x2C)

Bit	Name	Description	Read/Write Flag	Reset Value
31:4	---	read-only, not writeable	R	0
3	SLVIE	Slave mode interrupt enable: 0: not enabled 1: Enabling	R/W	0
2	CC1IE	Capture compare channel 1 interrupt enable: 0: not enabled 1: Enabling	R/W	0
1	CC0IE	Capture compare channel 0 interrupt enable: 0: not enabled 1: Enabling	R/W	0
0	OVIE	Overflow interrupt enable:	R/W	0

		0: not enabled 1: Enabling		

11.4.10 Status Register TC_STA (0x30)

Bit	Name	Description	Read/Write Flag	Reset Value
31:4	---	read-only, not writeable	R	0
3	SLVF	Slave mode event flag: (write 1 clear 0) 0: No slave mode event 1: There are slave mode events	R/W	0
2	CC1F	Capture compare channel 1 event flag: (write 1 clear 0) 0: No capture or comparison events 1: With capture or comparison events	R/W	0
1	CC0F	Capture compare channel 0 event flag: (write 1 clear 0) 0: No capture or comparison events 1: With capture or comparison events	R/W	0
0	OVF	Overflow interrupt flag: (write 1 clear 0) 0: No overflow event 1: There is an overflow event	R/W	0

11.5 Typical Application

11.5.1 Automatic operation mode, timer function

Automatic operation mode i.e. interval timing function.

For the basic timing function, only the following registers need to be set:

1、 The target count value register, which is the timing duration, is counted by the count clock.

2、 Enable overflow interrupt enable in the interrupt enable register.

3、 Control register to start the timer.

The timer generates an interrupt with the target count value as the period.

Configuration description of commonly used optional features:

1、 The prescaler register value can be modified to change the frequency of the timer count clock.

2、 Configurable Clock Configuration Register, CM modifies the configuration to External Input Clock and also modifies the External Input Clock selection of the CS bit configuration. The external input clock frequency must not be higher than the bisection of the internal system clock frequency.

3、 Single count mode, the timer stops when it overflows; the OPS bit of the Configuration Control Register is 1 for single count mode.

4、 The external input clock source is the output of another timer, then it can be connected as a cascade mode of two timers whose registers can be increased in bit width.

11.5.2 Input capture mode, pulse width measurement function

The main function of the input capture mode is that the width of the pulse can be tested.

For the basic pulse width test function, only the following registers need to be set:

1、 Target count value register, counted by the count clock, can be set to the maximum value.

2、 Capture Compare Channel 0/1 Mode Register is set, ENABLE Channel 0/1 is enabled, CCM is configured for capture mode, CPOL selects capture polarity, and CS selects external input events.

3、 Enable capture compare channel 0/1 interrupt enable in the interrupt enable register.

4、 Control register to start the timer.

When the timer captures the capture polarity of an external input event, an interrupt is generated and the current count value is saved in the capture comparison channel data register. If two channels are used, one capturing the rising edge and one capturing the falling edge, the pulse width can be calculated from the data registers of both channels.

Configuration description of commonly used optional features:

1、 The prescaler register value can be modified to change the timer count clock frequency.

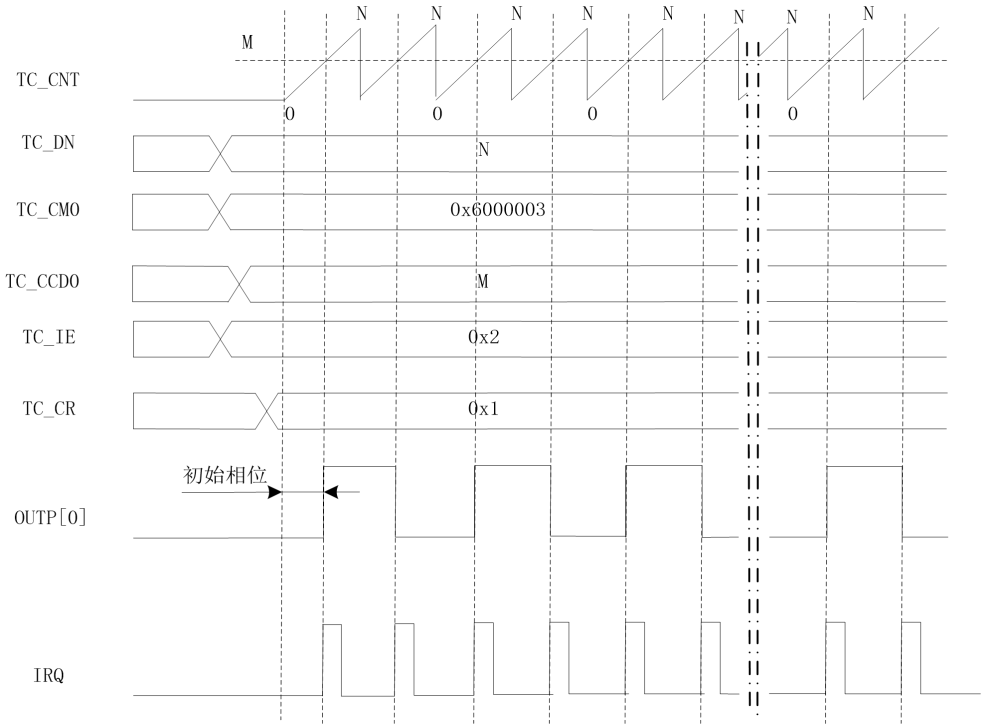
2、 Configurable Clock Configuration Register, CM modifies the configuration to external input clock and also modifies the external input clock source configured in the CS bit. The external input clock source frequency must not be higher than the bisection of the internal system clock frequency.

3、 Filtering of external input events, enabling the FLTEN filtering function in the Capture Compare Channel Mode Register, and setting the number of filtering cycles by configuring FLTOPT.

4、 If the external input event is the output of another timer, it can be connected as a cascade mode of two timers.

11.5.3 Comparison output mode, square wave output function

The square wave output function is the function of dividing the TC's count clock for output. Each timer has two output channels, each channel has two outputs P and N, where P is the forward output port and N is the reverse output port of P.



For the square wave output function, only the following registers need to be set:

1、 Target count value register, counted by the count clock, can be set to the maximum value.

2、 Capture Compare Channel 0/1 Mode Register Setting, ENABLE Channel 0/1 Enable, CCM Configured for Compare Mode, DFTLVL Configured for Default Level, EFELVL Configured for Valid Level, and OM Output Configured for Flip Function.

3、 Set the capture compare channel 0/1 data register. (set value not greater than target count value register)

4、 Enable capture compare channel 0/1 interrupt enable in the interrupt enable register.

5、 control register to start the timer.

The value of the target count value register determines the period of the output square wave, and the value of the capture compare channel 0/1 data register is the output flip point.

Configuration description of commonly used optional features:

1、 The prescaler register value can be modified to change the frequency of the timer count clock.

2、 Configurable Clock Configuration Register, CM modifies the configuration to external input clock and also modifies the external input clock source configured in the CS bit. The external input clock source frequency must not be higher than the bisection of the internal system clock frequency.

3、 The external input clock filter function enables the FLTEN filter function in the Clock Configuration Register and sets the number of filtering cycles by configuring FLTOPT.

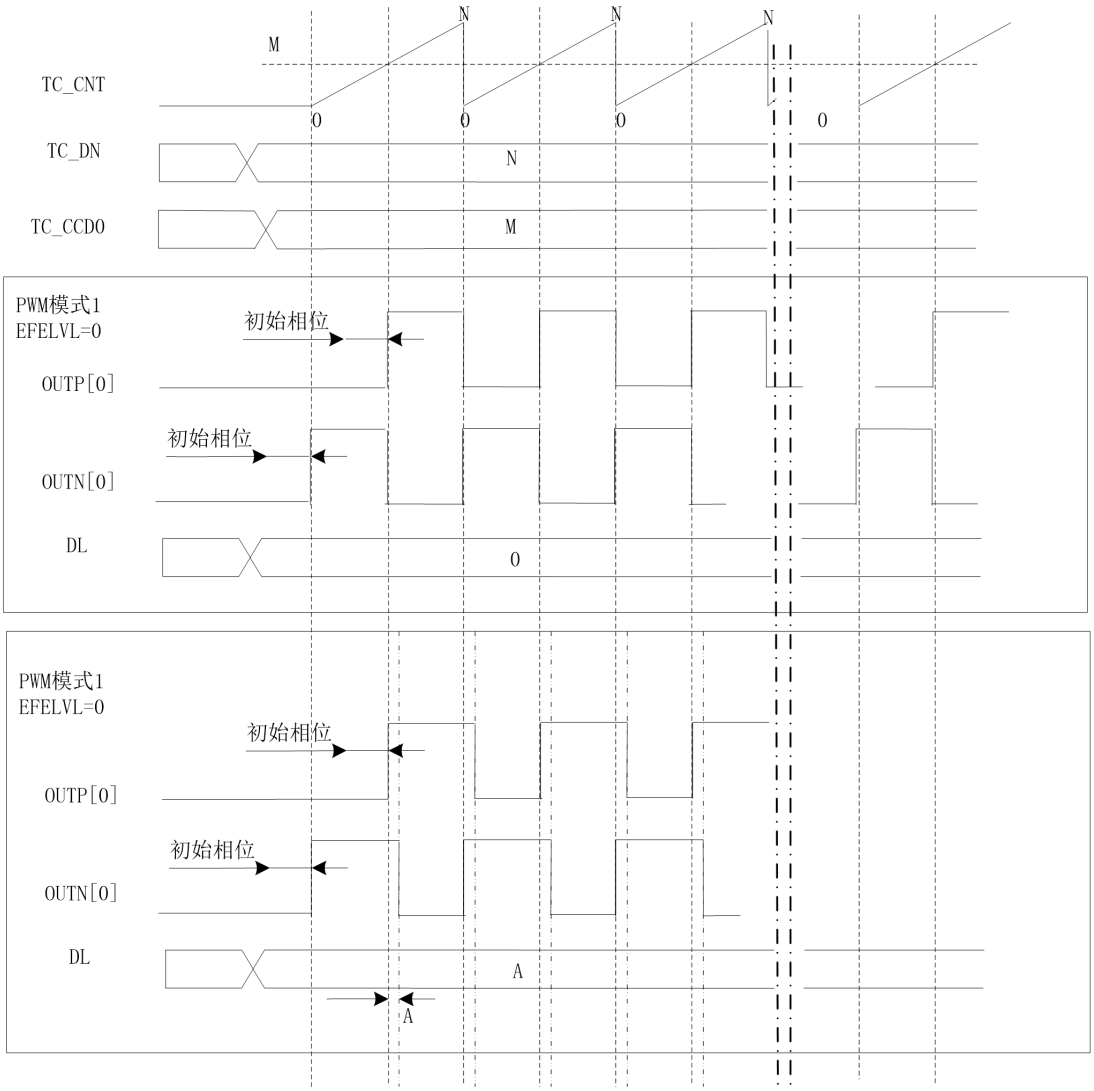
11.5.4 Comparison output mode, PWM output function

The Pulse Width Modulation (PWM) mode generates a signal with a frequency determined by the TC_DN register and a duty cycle determined by the TC_CCDx register. Two PWM modes are supported: PWM mode 1 and PWM mode 2:

PWM mode 1: If TC_CNT<TC_CCDx, the output is valid level, otherwise it is invalid level.

PWM mode 2: If TC_CNT>=TC_CCDx, the output is valid level, otherwise it is invalid level.

The following figure shows a typical application diagram for PWM mode 1.



For PWM output function, only the following registers need to be set:

1、 Target count value register, counted by the count clock.

2、 The Capture Compare Channel 0/1 Mode Register is set, ENABLE Channel 0/1 is enabled, CCM is configured for Compare Mode, DFTLVL is configured for default level, EFELVL is configured for active level, and the OM outputs are configured for PWM Mode 1 or PWM Mode 2.

3、 Set the capture compare channel 0/1 data register, which must be smaller than the target count value register.

4、 control register to start the timer.

At the P terminal of the channel, the positive waveform of PWM mode 1/PWM mode 2 is output, and at the N terminal of the channel, the waveform that is inverse to the P terminal is output.

PWM Mode 1: The period is the target count value register value plus one, and the active level period is the number of periods of the channel data register value plus one.

PWM Mode 2: The period is the target count value register value plus one, and the invalid level period is the number of periods of the channel data register value plus one.

Configuration description of commonly used optional features:

1、 The prescaler register value can be modified to change the timer count clock frequency.

2、 Configurable Clock Configuration Register, CM modifies the configuration to external input clock

and also modifies the external input clock source configured in the CS bit. The external input clock source frequency must not be higher than the bisection of the internal system clock frequency.

3、Complementary outputs for deadband insertion, DIEN deadband insertion enable, DL configure deadband insertion length. Add a delay between the two edge toggles of P and N, i.e., do not allow both edges to flip at the same time.

When the active level EFELVL is low: the falling edges of the outputs of P and N are delayed by DL cycles.

When the active level EFELVL is high: the rising edges of the outputs of P and N are delayed by DL cycles.

11.5.5 Slave mode, external clear and gating functions

The slave mode adds external input events to the original functions to control the clearing of the internal counter and gating.

For the external clear function, only the following registers need to be set:

1、Target count value register, counted by the count clock.

2、Enable overflow interrupt enable in the interrupt enable register.

3、control registers, SLVEN from mode enable, SLVTRGMODE from mode control mode selection, SLVCHANSEL from mode external input event selection, the

4、control register to start the timer.

This adds an external clearing of the internal CNT in free-run mode.

Configuration description of commonly used optional features:

1、The prescaler register value can be modified to change the timer count clock frequency.

2、Configurable Clock Configuration Register, CM modifies the configuration to external input clock and also modifies the external input clock source configured in the CS bit. The external input clock source frequency must not be higher than the bisection of the internal system clock frequency.

3、Single count mode, the timer stops when it overflows; the OPS bit of the Configuration Control Register is 1 for single count mode.

4、The external input clock source is the output of another timer, then it can be connected as a cascade mode of two timers whose registers can be increased in bit width.

5、In Slave Mode Control Mode Selection, if Gated Mode is selected, SLVGATELVL Slave Mode Gated Valid Level Configuration, the inputs of Slave Mode are counted by the internal counter only at the Gated Valid Level.

6、When the slave mode is configured as an input capture mode, and the external input event of the slave mode and the external input event of the capture are configured to be the same, the pulse width can be obtained directly from the Capture Compare Channel Data Register by selecting one edge for the capture and the other edge for the slave mode polarity.

11.6 Procedure

Briefly describes the procedure for operating as an interval timer, setting TC0 to a 1MS interval timed interrupt:

1、Configure bit 4 of Module Enable 0 register MOD0_EN in the system control chapter to start the clock of TC0. Note that to write the registers in the System Control chapter, you need to write SYS_PS to 0x82 first

to turn on the write enable, and after the operation of the system control registers that need to be written is completed, you need to write SYS_PS to 0 to turn off the write enable.

2、 Set the TC0 module registers:

Clock Configuration Register TC_CCFG is configured as internal system clock, TC0->CCFG = 0;

Configure the prescaler register TC_PS;

Configure the target notation value register TC_DN;

Configuration control register TC_CR, TC0->CTRL = 0x01; start TC0 timer

Set interrupt enable register TC_IE, TC0->IE = 0x01; configure as overflow interrupt enable;

When the system clock is 3.6864MHZ, TC0->PS = 255;TC0->DN = 13 Configured to generate 1MS interrupt. (3.6864MHZ/(255+1))/(13+1) = 1MS.

3、 Enable TC0 interrupt enable, NVIC_EnableIRQ(TC0_IRQn).

4、 Write an interrupt service program:

```
void TC0_HANDLER(void)
{
    /* Start adding user code. Do not edit comment generated here */
}
```

5. 1MS interrupt can be generated after the configuration is completed.

11.7 PWM mode register description (new)

Register list

register name	address offset	Description
PWM_CFG	Offset+0x34	PWM Configuration Register
PWM_CTL	Offset+0x38	PWM Control Register
PWM_STA	Offset+0x3C	PWM Status Register
PWM_CNT	Offset+0x40	PWM Parameter Register
PWM_DMA_BADR	Offset+0x44	PWM DMA Start Address Register
PWM_DMA_LEN	Offset+0x48	PWM DMA Data Length Register
PWM_DMA_ADR	Offset+0x4C	PWM DMA Current Address REGISTER

11.7.1 PWM_CFG (0x34)

PWM control register, support bitband operation

If you configure the control bits of the following registers during the waveform generation process, the output result will be changed accordingly, so do not configure the following registers during the waveform generation process.

Bit	Name	Description	Read/Write Flag	Reset Value
31:17	---	reserve	R	0
16:7	WL	PWM wave length, PWM output signal length configuration parameter Valid only in Length Matchable mode.	R/W	0

		Indicates the output WL+1 full signal cycle Example: In dam mode, using PWM to simulate a sine wave means outputting WL+1 sine wave period, i.e., traversing through the completed dam data table counts as one complete signal period; in software mode, outputting a square wave means outputting WL+1 square wave, i.e., counting as one complete signal period for each PWM parameter used.		
6	ORV	Output Remain Valid, output signal is always valid 0: Length-assignable mode 1: Always Effective Model The length is assignable to indicate the use of the WL parameter; always active is to keep outputting waveforms until the enable is turned off.	R/W	0
5	CSS	Complete Signal selection 0: Software shutdown of the module will stop the waveform output after completing a complete signal. In DMA mode, the end of dma length indicates a complete signal; in software mode, a pwm waveform indicates a complete signal. 1: Stop PWM output immediately after software shutdown of the module	R/W	0
4	CMS	Control mode selection, PWM modulation control mode. 0: dma mode 1: Software control mode	R/W	0
3	CYCDONEIE	Output signal cycle completion interrupt enable 0: not enabled 1: Enabling	R/W	0
2	BUFVLDIE	PWM parameter cache air-break enable (used in software mode only) 0: not enabled 1: Enabling	R/W	0
1	DATERRIE	Data error interrupt enable 0: not enabled 1: Enabling	R/W	0
0	DONEIE	PWM output completion interrupt 0: not enabled 1: Enabling	R/W	0

11.7.2 PWM_CTL (0x38)

PWM Control Register

Bit	Name	Description	Read/Wri	Reset

			te Flag	Value
31:1	---	reserve	R	0
0	EN	PWM module enable bit 0: PWM modulation off 1: PWM modulation on Closed and opened only by software. In DMA mode, when dma_len is 0, after enabling, you must remember to turn off the enable, otherwise it will affect the TC function.	R/W	0

11.7.3 PWM_STA (0x3C)

PWM Status Indicator Register

Bit	Name	Description	Read/Write Flag	Reset Value
31:4	---	reserve	R	0
4	CYCDONE	Output signal cycle completion interrupt 0: Output of one cycle signal not completed 1: Completion of one cycle of signal output Write 1 clear 0 In DMA mode, it is set up when the traversal of the DMA table is completed. For example, to simulate sine wave output, it is set up when one cycle of the sine wave is finished. In software control mode, each PWM square wave output is set up after completion, i.e., after each parameter count is finished.	R/W	0
3	BUFVLD	PWM Parameter Cache Air Break (used in software mode only) 0: PWM parameters are present in the cache in software control mode 1: New PWM parameters can be configured when in software control mode Write 1 clear 0 Set up at the beginning of the waveform output; set up at the end of each PWM parameter count.	R/W	0
2	DATERR	Data Null Error Interrupt 0: Normal read data 1: In DMA mode, data cannot be read in time due to competition; in software control mode, new data is not written in time due to the user. Write 1 clear 0 In DMA mode, when the competition time is greater than the set PWM parameter, set up. In software control mode, if no new data is written before	R/W	0

		the counting of the last PWM parameter ends, the counting will be set up at the end of the counting; if no PWM parameter is written before startup, the startup will be set up after startup.		
1	DONE	PWM output completion interrupt 0: Waveform output not completed 1: Waveform output complete Write 1 clear 0 Set up when WL counting is completed; when CSS=0, after shutdown, set up when waveform output is completed; when CSS=1, after shutdown, do not set up.	R/W	0
0	BUSY	PWM signal transmission status 0: Idle state 1: Waveform generation state	R	0

11.7.4 PWM_CNT (0x40)

PWM Parameter Register

N_Duty configuration in TC1_CCD1

Bit	Name	Description	Read/Write Flag	Reset Value
31:16	--	reservations	R/W	0
15:0	N_Pwm	Indicates the system clock cycle length for the current PWM cycle. The actual count clock period is N_Pwm+1 In software control mode, the cache is empty and configurable, and the configuration overwrites the original value when it is not empty Do not configure in DMA control mode.	R/W	0

11.7.5 PWM_DMA_BADR (0x44)

PWM DMA start address

Bit	Name	Description	Read/Write Flag	Reset Value
31:16	Reserved	Reservations.	R	0
14:0	BADR	DMA start address (Word address)	R/W	0

11.7.6 PWM_DMA_LEN (0x48)

PWM DMA data length

Bit	Name	Description	Read/Write Flag	Reset Value
31:15	Reserved	Reservations.	R	0
14:0	LEN	The DMA data length, i.e., the length of the PWM parameter table, is configured as n , length = n Word, and the table size is n	R/W	0

		It is recommended that the input length LEN>1; if LEN=1 is required it is recommended to use the software control mode. In DMA mode, when LEN=1, the final length output is WL+2 if the length configurable function is used.		

11.7.7 PWM_DMA_ADR (0x4C)

PWM DMA current address

Bit	Name	Description	Read/Write Flag	Reset Value
31:15	Reserved	Reservations.	R	0
14:0	ADR	DMA Current Address	R	0

11.8 PWM Mode Software Operation Procedure

11.8.1 Parameter constraint

Duty cycle count limit: 0<N_Duty<N_Pwm-1

When generating a dynamic continuous square wave in software mode, N_PWM is recommended to be greater than 11, and when it is less than or equal to 11, it is not possible to write new data in time (enter interrupt->write N_DUTY->write N_PWM->clear interrupt; these operations take some time).

Deadband length DL is suggested: DL<=N_Duty, DL<N_Pwm-N_Duty.

11.8.2 DMA control mode

1. MOD0_EN = 1<<5; //Turn on the clock of TC1
2. TC1_CM1 = 1 | 1<<1 | DIEN<<2 | DL<<3 | OM <<25 | EFELVL << 28 | DFTLVL <<29;
// configure channel 1 of TC1, where OM is selectable for PWM mode 1 or 2.
3. PWM_STA = 0xE; //clear all interrupt flags
4. PWM_DMA_BADR = 0xxxx; //configure DMA data start address
5. PWM_DMA_LEN = 0xxxx; // Configuration data length
6. PWM_CFG = 0xxxx; // Configuration related control
7. PWM_CTL = 0x1; //Enable

8.1 If the setup length is configurable, wait for the end of the wait, by interrupting DONE or flag BUSY

8.2 Software shutdown if continuous output is set

9. PWM_CTL = 0x0; // shutdown enable
10. PWM_STA = 0xE; //clear interrupt

11.8.3 Software Control Mode

11.8.3.1 A single square wave

1. MOD0_EN = 1<<5; //Turn on the clock of TC1
2. TC1_CM1 = 1 | 1<<1 | DIEN<<2 | DL<<3 | OM <<25 | EFELVL << 28 | DFTLVL <<29;
// configure channel 1 of TC1, where OM is selectable for PWM mode 1 or 2.
3. PWM_STA = 0xE; //clear all interrupt flags
4. TC1_CCD1 = 0xxxx; //configure the N_Duty parameter
5. PWM_CNT = 0xxxx; //configure the N_Pwm parameter

6. PWM_CFG = 0xxxx; //configure related controls, turn off DATERR, BUFVLD interrupt enable
//Use length assignable mode, set WL=0;
7. PWM_CTL = 0x1; //Enable
8. Wait for the DONE interrupt or flag BUSY=0;
9. PWM_STA = 0xE; //clear interrupt
10. PWM_CTL = 0x0; // shutdown enable
11. TC1_CCD1 = 0xxxx; //configure the N_Duty parameter
12. PWM_CNT = 0xxxx; //configure the N_Pwm parameter
13. PWM_CTL = 0x1; //Enable
14. Wait for DONE interrupt or flag BUSY=0;
15. PWM_STA = 0xE; //clear interrupt
16. PWM_CTL = 0x0; // shutdown enable

11.8.3.2 Continuous square wave

1. MOD0_EN = 1<<5; //Turn on the clock of TC1
2. TC1_CM1 = 1 | 1<<1 | DIEN<<2 | DL<<3 | OM <<25 | EFELVL << 28 | DFTLVL <<29;
// configure channel 1 of TC1, where OM is selectable for PWM mode 1 or 2.
3. PWM_STA = 0xE; //clear all interrupt flags
4. TC1_CCD1 = 0xxxx; //configure the N_Duty parameter
5. PWM_CNT = 0xxxx; //configure the N_Pwm parameter
6. PWM_CFG = 0xxxx; //configure related controls, turn off DATERR, BUFVLD interrupt enable
7. PWM_CTL = 0x1; //Enable
8.1 If the setup length is configurable, wait for the end of the wait, by interrupting DONE or flag BUSY
8.2 Software shutdown if continuous output is set
9. PWM_CTL = 0x0; // shutdown enable
10. PWM_STA = 0xE; //clear interrupt

11.8.3.3 Dynamic Continuous Square Wave

1. MOD0_EN = 1<<5; //Turn on the clock of TC1
2. TC1_CM1 = 1 | 1<<1 | DIEN<<2 | DL<<3 | OM <<25 | EFELVL << 28 | DFTLVL <<29;
// configure channel 1 of TC1, where OM is selectable for PWM mode 1 or 2.
3. PWM_STA = 0xE; //clear all interrupt flags
4. TC1_CCD1 = 0xxxx; //configure the N_Duty parameter
5. PWM_CNT = 0xxxx; //configure the N_Pwm parameter
6. PWM_CFG = 0xxxx; //configure the relevant controls to enable the BUFVLD interrupt
// If the configuration length is always valid, it is recommended to configure CSS=0;
7. PWM_CTL = 0x1; //Enable
8. Wait for BUFVLF interrupt
9. TC1_CCD1 = 0xxxx; //configure the N_Duty parameter
10. PWM_CNT = 0xxxx; //configure the N_Pwm parameter
//N_Duty, N_Pwm are configured on demand, you can configure only one.
// If neither parameter is configured, the daterr interrupt flag is triggered.
11. PWM_STA = 0xE; //clear interrupt flag

12. Cycle through steps 8 to 11;
13.1 If the configuration length is assignable mode
14.1 Wait for BUFVLF interrupt after all data has been written.
15.1 PWM_STA = 0xE; // Clear the interrupt flag.
16.1 Wait for DONE interrupt or flag BUSY=0;
17.1 PWM_CTL = 0x0; // shutdown enable
18.1 PWM_STA = 0xE; // Clear the interrupt flag.
13.2 If the configuration length is always valid mode and CSS=0;
14.2 After all data has been written, wait for the BUFVLF interrupt.
15.2 PWM_CTL = 0x0; // shutdown enable
16.2 Wait for DONE interrupt or flag BUSY=0;
17.2 PWM_STA = 0xE; // Clear the interrupt flag.

12 Analog Peripherals

12.1 Features

12bit SAR ADC；

- When the voltage input to the VBAT pin to start measuring, there are two 300K resistors inside to divide the voltage. The input voltage is reduced by half to the SAR ADC. The SAR ADC uses the 0.5x PGA to double the signal. Namely: 3.6V battery, the measured signal is about 0.9V. If the measurement is not started, the internal partial resistor will be turned off.
- If another pin (AIN) is selected for input voltage measurement, narrow down the measured voltage to the SAR ADC measurement range.
- AIN support up to 1.25V input. Gain support 0.5 times, 1 time, 1.5 times, 2 times, and add support for 0.25 times.
- Multiplexing, supports AIN0~AIN6, VBAT, and temperature sensor as inputs, of which the temperature sensor has the highest priority;
- The input impedance of AIN0~AIN6 is about 5M ohms, and an external 0.1uF capacitor needs to be connected to ground
- When the ADC is not sampling, it automatically enters the power saving mode; each sample is about 12ms from start to finish

The main features of one LVD circuit are as follows：

- The input of LVD can choose the power for the chip or an external input PIN ；
- LVD threshold is adjustable, which is from 2.3V to 4.9V ；
- When selecting an external PIN as input, the threshold value is fixed at about 1.25V, and the internal resistance is about 1M ohm；

The main features of two comparator circuit CMP1 and CMP2 are as follows：

- External PIN input, the threshold is about 1.25V
- The power consumption is better than 1uA. The comparator can be used to monitor the main power。
- ote that there are 600K pull-down resistors inside CMP1 and CMP2, and the internal resistor can be turned off by register (SYS_PD (0x08)).

12.2 Register

Base address of analog peripheral module

Module Name	Physical Address	Address Mapping
ANA	0x4002C000	0x4002C000

Register offset address of analog peripheral module

Register Name	Address Offset	Description
SAR_CTRL	Offset+0x0	SAR-ADC Control Register

SAR_START	Offset+0x4	SAR-ADC Start Register
SAR_STAT	Offset+0x8	SAR-ADC Status Register
SAR_DAT	Offset+0xC	SAR-ADC Data Register
LVD_CTRL	Offset+0x10	Comparator Control Register
LVD_STAT	Offset+0x14	Comparator Status Register
SAR_CTRL1（new）	Offset+0x18	SAR-ADC gain control register1
SAR_DATA2（new）	Offset+0x1C	SAR-ADC 12bit data register2
SAR_CTRL3（new）	Offset+0x20	SAR-ADC gain control register3
SAR_DATA3（new）	Offset+0x24	SAR-ADC 12bit data register3

12.2.1 SAR_CTRL(0x0)

ADC Control Register, Offset Address 0x00

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:12	REF_WAIT	The wait time from REF started to ADC started: The typical value of the minimum waiting time is 122us 5'd0: 122us 5'd31: (31+1)*122us That is, wait time = (REF_WAIT+1)* 976uS This wait time can be set to 0 if metering is on in run mode and REF is also on。 It is recommended to set a wait time greater than 10ms if metering is not turned on. Note: The external capacitance of the metering reference REF is 1uF + 0.1uF	R/W	0
11:7	SAR_WAIT	The wait time from SAR ADC started to sampling convert started: 5'd0: 30.5us 5'd31: (31+1)*30.5us Wait Time=(SAR_WAIT+1)*30.5us Note: Step of start ADC measuremen： 1、Start REF, wait time of REF_WAIT； 2 、 Start ADC and Temperature Sensor, wait time of SAR_WAIT； 3、nput clock and reset single, the sampling results obtained after 16 clock cycles。 The above steps are achieved from hardware automatic contro。 Note 2: It is recommended that the client application configure this register to the default value of 0xE, which is 457.5us.	R/W	0xE
6	SAR_CH3	The SAR-ADC Channel is selected to form a 4-bit register with SAR_CH [2:0].See SAR_CH definition	R/W	0
5	SAR_IE	SAR-ADC Interrupt Control:	R/W	0

		1: Enable ADC interrupt output; 0: Disable ADC interrupt output.		
4:3	SAR_PGA	SAR-ADC Gain Control: 00: 0.5 01: 1 10: 1.5 11: 2 Added support for 0.25x gain, see SAR_PGA_SEL[2:0](SAR_CTL1) definition.	R/W	0
2:0	SAR_CH	SAR-ADC Channel selection determined by {SAR_CH3,SARCH[2:0]}. 0000: Temperature measurement 0001: VBAT (for 3.6V battery, 1/2 divider gives 1.8V, PGA uses 0.5x, measuring input 0.9V) 0010: External pin input AIN0 0011: External pin input AIN1 0100: External pin input AIN2 0101: External pin input AIN3 0110: External pin input AIN4 0111: External pin input AIN5 (new) 1000: External pin input AIN6 (new) 0111: Reservations Automatic temperature measurement has the highest priority, regardless of which channel it is set to.	R/W	0
Note: The above register bits are writable only when ST=0 in SAR_START.				

12.2.2 SAR_START(0x4)

SAR-ADC Start Register, Offset Address 0x04

Bit	Name	Description	R/W	Reset Value
31:01	Reserved	Reserved	R	0
0	ST	SAR-ADC Start Bit 0: SAR-ADC No Operation; 1: Start SAR-ADC sampling one time, automatically clear after the completion of the sampling. Note： 1、Automatic temperature measurement controlled by the RTC is not controlled by the bit, and a higher priority than the configuration bits； 2、When the ADC_START bit is 1, the software is forbidden to write 1 again to start the SAR-ADC measurement; after the last SAR-ADC conversion is completed, the bit is 0 after 100us (that is, after detecting 0, then delay 100us), the new can be started. SAR-ADC measurement; recommended	R/W	0

		timeout wait time = 2* (REF_WAIT + SAR_WAIT) + 51ms。		

12.2.3 SAR_STAT(0x8)

SAR-ADC Status Register, Offset Address 0x08

Bit	Name	Description	R/W	Reset Value
31:02	Reserved	Reserved	R	0
1	TPS_BUSY	Automatical temperature measurement bit, =1:Automatical temperature measurement in process; =0: No automatical temperature measurement. When TPS_BUSY =1, software write ADC_START register, hardware operations will work after TPS_BUSY is 0.	R	0
0	DREADY	ADC Date Ready Pending Bit 0:ADC The conversion result is not completed 1:ADC The conversion result is completed Note: 1. Write 1 clear; Automatical temperature measurement controlled by the RTC is not indicated in this state;	R/W	0

12.2.4 SAR_DAT(0xC)

ADC Data Register, Offset address 0x0C

Bit	Name	Description	R/W	Reset Value
15:10	Reserved	Reserved	R	0
9:0	SAR-DAT	The conversion result of ADC	R	0

12.2.5 LVD_CTRL(0x10)

LVD Control Register, Offset address 0x10

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	R	0
9	SWHBIE	Switch to battery interrupt enable: = 0: Disable interrupts; = 1: Enable interrupt;	R/W	0
8	SWHMIE	Switch to main power interrupt enable: = 0: Disable interrupts; = 1: Enable interrupt;	R/W	0
7	CMP2IE	Comparator 2 enable interrupt: = 0: Disable interrupts; = 1: Enable interrupt;	R/W	0
6	CMP1IE	Comparator 1 enable interrupt: = 0: Disable interrupts; = 1: Enable interrupt;	R/W	0

<table>
<tr><td>5</td><td>LVDIE</td><td>LVD enable interrupt:
= 0: Disable interrupts;
= 1: Enable interrupt;</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>Reserved</td><td>Reserved</td><td>R</td><td>0</td></tr>
<tr><td>3:0</td><td>LVDS</td><td>Set LVD threshold voltage:
<table>
<tr><td>LVDS[3:0]</td><td>Vil(V)</td><td>Vih(V)</td></tr>
<tr><td>0000</td><td>2.3</td><td>2.4</td></tr>
<tr><td>0001</td><td>2.5</td><td>2.6</td></tr>
<tr><td>0010</td><td>2.7</td><td>2.8</td></tr>
<tr><td>0011</td><td>2.9</td><td>3.0</td></tr>
<tr><td>0100</td><td>3.1</td><td>3.2</td></tr>
<tr><td>0101</td><td>3.3</td><td>3.4</td></tr>
<tr><td>0110</td><td>3.5</td><td>3.6</td></tr>
<tr><td>0111</td><td>3.7</td><td>3.8</td></tr>
<tr><td>1000</td><td>3.9</td><td>4.0</td></tr>
<tr><td>1001</td><td>4.0</td><td>4.1</td></tr>
<tr><td>1010</td><td>4.2</td><td>4.3</td></tr>
<tr><td>1011</td><td>4.4</td><td>4.5</td></tr>
<tr><td>1100</td><td>4.6</td><td>4.7</td></tr>
<tr><td>1101</td><td>4.7</td><td>4.8</td></tr>
<tr><td>111x(LVDIN)</td><td>1.25</td><td>1.45</td></tr>
</table>
Note: When LVDS[3:0] = 4’b111x, the external LVDIN pin input voltage is detected. When equal to other values, the VCC input voltage is detected。</td><td>R/W</td><td>0</td></tr>
</table>

Note: LVD, Comparator 1 and Comparator 2 merge an interrupt vector; Power switching is a single interrupt vector; SAR-ADC is a single interrupt vector.

12.2.6 LVD_STAT(0x14)

LVD Status Register Offset address 0x14

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	R	0
9	SWHF	Power switching status flag: = 0: Mains power mode; =1: Battery mode. Read Only	R	0
8	SWHBIF	Switch to the battery interrupt flag: = 0: no interrupt generated; = 1: interrupt generated; An interrupt is generated when the power supply switches from mains to battery, and write 1 clears;	R/W	0
7	SWHMIF	Switch to the main power interrupt flag: = 0: no interrupt generated; = 1: interrupt generated; An interrupt is generated when the power supply switches from battery to mains, and write 1 clears;	R/W	0

6	CMP2IIF	Comparator 2 interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
5	CMP1IIF	Comparator 1 interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
4	LVDIIF	LVD interrupt flag =0:No interrupt is generated;=1:Generate an interrupt; Interrupt is generated when the input voltage is low relative to the threshold or becomes high, cleared by writing 1;	R/W	0
3	Reserved	Reserved	R	0
2	CMP2IF	Comparator 2 status flag =0:Below threshold; =1:Above threshold, only read;	R	0
1	CMP1IF	Comparator 2 status flag =0:Below threshold; =1:Above threshold; only read;	R	0
0	LVDIF	LVD status flag =0:Below threshold; =1:Above threshold, only read;	R	0

12.2.7 SAR_CTRL1(0x18)（new）

ADC Contorl Register1， Offset address 0x18

Bit	Name	Description	R/W	Reset Value
31:15	Reserved	Reserved	R	0x0
14:8	SAR_CONVERT	The waiting time for SAR ADC sampling conversion to digital sampling DOUT: 6'd0: Tsar_clk (Tsar_clk is SARInterface clock cycle, refer to ANA_ RCH register) … 6'd127: (127+1)* Tsar_clk i.e. Waiting time=(SAR_CONVERT +1)*Tsar_clk Note: SAR_CONVERT[6:0]>=(SAR_SAMPLE[2:0]*2+21)*2Tsar_clk	R/W	0x29
7	Reserved	Reserved	R	0
6:4	SAR_SAMPLE	Clock number of Sampling cycle: 000: 1 clk 001: 2 clk 010: 3 clk	R/W	0x0

		…… 111: 8 clk		
3	SAR_PGA_SEL	Selection instructions of SAR-ADC gain control register =0, choose SAR_CTL[4:3] as SAR-ADC gain control register; =1, choose SAR_CTL1[2:0] as SAR-ADC gain control register	R/W	0x0
2:0	SAR_PGA	SAR-ADC gain control bit 000: 0.5 times 001: 1 times 010: 1.5 times 011: 2 times 1xx: 0.25 times	R/W	0x0

12.2.8 SAR_DAT2(0x1C)（new）

ADC DAT register 2, Offset address 0x1C

Bit	Name	Description	R/W	Reset Value
15:12	Reserved	Reserved	R	0
11:0	SAR_DAT2	ADC converting result	R	0

12.2.9 SAR_CTRL3（0x20）（new）

SAR control register 3

Bit	Name	Description	R/W	Reset Value
31:7	Reserved	Reserved	R	0x0
14:7	SAR_NUM_CFG	SAR ADC Output Data Accumulation Points Configuration = 0, 1 point = 1, 2 points cumulative ... =N, N+1 point accumulation Supports up to 256 points of totalization	R/W	0x0
6:0	SAR_CLK_DIV	SAR_CLK interface clock division factor: (using the SAR controller working clock frequency as a reference) =0：2 frequency division =1：2 frequency division … =N：N+1 frequency division The SAR_CLK clock source comes from RCM3.6M, the output frequency is 256K after 14 divisions, and the SAR sampling clock is obtained after SAR_CLK_DIV dividing, the default sampling clock is 16KHZ.	R/W	0xf

12.2.10 SAR_DAT3（0x24）（new）

ADC DAT register 3

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	SAR_DAT3	The ADC accumulates the results, and the results are processed as shown in the following table.	R	0

totalizing point	SAR_DAT_SUM right shift	SAR_DAT3
128<(SAR_NUM_CFG+1)≤256	4	SAR_DAT_SUM[19:4]
64<(SAR_NUM_CFG+1)≤128	3	SAR_DAT_SUM[18:3]
32<(SAR_NUM_CFG+1)≤64	2	SAR_DAT_SUM[17:2]
16<(SAR_NUM_CFG+1)≤32	1	SAR_DAT_SUM[16:1]
0<(SAR_NUM_CFG+1)≤16	0	SAR_DAT_SUM[15:0]

12.3 ADC voltage detection steps

1、 Configure the system control chapter module enable 1 register MOD1_EN bit 11 to 1, turn on the SAR_EN clock.

2、 Determine whether the first bit of SAR_ADC status register SAR_STATUS is 0. No automatic temperature measurement is performed. If it is 0, it will enter the next step. If it is 1, it will wait.

3、 Configure the ADC control register SAR_CTL, configure the wait time and gain, and select the corresponding ADC channel for the channel.

4、 The SAR-ADC start register SAR_START is configured to 1 to initiate ADC conversion.

5、 Determine the 0th bit of the SAR-ADC status register SAR_STATUS and wait for the conversion to complete.

6、 Read the ADC conversion data register SAR_DAT.

7、 Calculation: The ADC reference voltage source is 1.25V, and the ADC DAT register value is 1024 when the ADC is full. The calculation formula is (ADC DAT *1.25) / 1024. When the voltage value exceeds the full scale of the ADC, the conversion value is 1024

Conversion and calculation is complete.

12.4 VBAT Voltage Detection

1、 Configure the system control chapter module enable 1 register MOD1_EN bit 11 to 1, turn on the SAR_EN clock.

2、 Determine whether the first bit of SAR_ADC status register SAR_STATUS is 0. No automatic temperature measurement is performed. If it is 0, it will enter the next step. If it is 1, it will wait.

3、 Configure the ADC control register SAR_CTL channel to be VBAT, configure the waiting time.

4、 The SAR-ADC start register SAR_START is configured to 1 to initiate ADC conversion.

5、 Determine the 0th bit of the SAR-ADC status register SAR_STATUS and wait for the conversion to complete.

6、 Read the ADC conversion data register SAR_DAT

7、 Calculation: The ADC reference voltage source is 1.25V, and the ADC DAT register value is 1024 when the ADC is full. The 3.6V battery is directly connected to the VBAT pin, and the MADC->AD_CTRL is

configured to 0x01. At this time, the gain is 0.5 times, then the voltage is the value is (ADC DAT *1.25*4) / 1024, where the gain is 0.5 times, the internal VBAT access has 1/2 partial pressure, so the actual voltage needs to be multiplied by 4.

8、 Conversion and calculation are completed.

13 GPIO (Modified)

13.1 Overview

- Contain PA,PB,PC,PD four GPIO
- PA ports include 5 P0 ports,8 P1 ports, 8 P2 ports, 8 P3 ports
- PB ports include 8 P4 ports, 8 P5 ports, 8 P6 ports, 8 P7 ports
- PC ports include 8 P8 ports, 8 P9 ports ,4 P10 ports,6 P11 ports
- PD ports include 8 P12 ports, 5 P13 ports ,8 P14 ports
- GPIO is peripheral of AHB
- Support bitband operation
- The LCD multiplexing pin is an open-drain structure when used as an IO port.

13.2 Register description

GPIO Register Base Address:

Module Name	Physical Address	Address Mapping
GPIO	0x50000000	0x50000000

GPIO Register Offset Address

PMA	0x00H	PA port mode register(input or output)
PA	0x04H	PA port data register
PCA0	0x08H	PA port reuse register 0
PCA1	0x0CH	PA port reuse register 1
PUA	0x10H	PA port pull-up selection register
PIMA	0x14H	PA port input mode configuration
PIEA	0x18H	PA port input enable selection
PMB	0x1CH	PB port mode register(input or output)
PB	0x20H	PB port data register
PCB	0x24H	PB port reuse register
PUB	0x28H	PUB port pull-up selection register
PIMB	0x2CH	PB port input mode configuration
PIEB	0x30H	PB port input enable selection
PMC	0x34H	PC port mode register(input or output)
PC	0x38H	PC port date register
PCC	0x3CH	PC port reuse register
PUC	0x40H	PUC port pull-up selection register
PIEC	0x44H	PC port input enable selection
PIMC	0x48H	PC port input mode register
PCB2	0x4CH	PB port multiplexes register 2
PMD	0x50	PD port mode register(input or output)
PD	0x54	PD port data register

PCD	0x58	PD port reuse register
PUD	0x5C	PUD port pull-up selection register
PCE	0x60H	SEGCOM port multiplexes register
PASET	0x64H	PA port data reset register, write 1 to this register, a correspond bit in PA port will be write 1;
PACLR	0x68H	PA port data clear register, write 1 to this register, a correspond bit in PA port will be cleared;
PBSET	0x6CH	PB port data reset register, write 1 to this register, a correspond bit in PB port will be write 1;
PBCLR	0x70H	PB port data clear register, write 1 to this register, a correspond bit in PB port will be cleared;
PCSET	0x74H	PC port data reset register, write 1 to this register, a correspond bit in PC port will be write 1;
PCCLR	0x78H	PC port data clear register, write 1 to this register, a correspond bit in PC port will be cleared;
PDSET	0x7C	PD port data reset register, write 1 to this register, a correspond bit in PD port will be write 1;
PDCLR	0x80	PD port data clear register, write 1 to this register, a correspond bit in PD port will be cleared;
PIED	0x84	PD port input enable selection
PIMD	0x88	PD port input mode register
PCA2	0x8C	PA port reuse register 2
PCA3	0x90	PA port reuse register 3
PCB3	0x94	PB port reuse register 3
PCC2	0x98	PC port reuse register 2
PCC3	0x98	PC port reuse register 3
PCC4	0xA0	PC port reuse register 4
PCC5	0xA4	PC port reuse register 5
PCD2	0xA8	PD port reuse register 2
PCD3	0xAC	PD port reuse register 3
PIMA2	0xB0	PA port input mode configuration 2
LURT_CFG	0x100	LPUART Configuration Register
IOCFG	0x104	IO Driver Configuration Register

Note: For IO port types, see Pin Arrangement.

It is recommended to use the bitband function to access the registers of the GPIO, which facilitates bit operations on the relevant registers of the IO port.

The SET/CLR register can also be used to write the GPIO data register;

If the IO port configuration options for the multiplexing function outside the IO port, mode register, the data register, input enable register is invalid

Pull-up enable is only supported in input mode.

13.3 PA port

13.3.1 PA port mode register(input or output)(0x00）

Bit	Name	Description	R/W Sign	Reset Value
31:24	PM37~PM30	=0 Output Mode =1 Input Mode PM37 and PM36 are read only, read 1, only can be input model;	R/W	FF
23:16	PM27~PM20	=0 Output Mode =1 Input Mode	R/W	FF
15:8	PM17~PM10	=0 Output Mode =1 Input Mode	R/W	FF
7:5	---	Reserved	R	0
4:0	PM04~PM00	=0 Output Mode =1 Input Mode	R/W	1F

13.3.2 PA port data register PA(0x04)

Bit	Name	Description	R/W Sign	Reset Value
31:30	**P37~P36**	**P36 and P37 data input register, read-only;**	**R**	**0**
29:24	P35~P30	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
23:16	P27~P20	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P17~P10	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:5	---	Reserved	R	0
4:0	P04~P00	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value If defined as an analog input, the input mode to read a value of 0.	R/W	00

13.3.3 PA port reuse 0 register PCA0 (0x08)

When selected as an analog input, the input mode is automatically selected, PMA register is invalid.

Bit	Name	Description	R/W Sign	Reset Value
31:30	UART2_SEL	By {PCA3[28],PCA0[31:30]} together define which IO is selected as UART2 configuration: =000: P24/P25 selected as UART2, see PCA0[27] for definition =001: P00/P01 is selected as UART2, see PCA0[3:0] for definition.	R/W	0

		=010: P20/P21 selected as UART2, see PCA0[25] for definition =011: P22/P23 selected as UART2, see PCA0[26] for definition =100: P26/P27 selected as UART2, see PCA0[28] for definitions. =Other: Reserved		
29	SWD_SEL	=0:P24 and P25 don't select SWD, define by PC245(bit27); =1:P24 and P25 select SWD;	R/W	1
28	PC267	Define the port P26 and P27 multiplex configuration: =0:select IO port; =1:select UART3 port. Note: When PCA3[27] = 0, this configuration is valid and backward compatible; when PCA3[27] = 1, the multiplexing of P26P27 is determined by PCA3[26:21].	R/W	00
27	PC245	Define the port P24 and P25 multiplex configuration: =0:select IO port; =1:select UART2 port. Note: When PCA3[20] = 0, this configuration is valid and backward compatible; when PCA3[20] = 1, the multiplexing of P24/P25 is determined by PCA3[19:14].	R/W	00
26	PC223	Define the port P22 and P23 multiplex configuration: =0:select IO port; =1:select UART1 port. Note: When PCA3[13] = 0, this configuration is valid and backward compatible; when PCA3[13] = 1, the multiplexing of P22/P23 is determined by PCA3[12:7].	R/W	00
25	PC201	Define the port P20 and P21 multiplex configuration: =0:select IO port; =1:select UART0 port. Note: When PCA3[6] = 0, this configuration is valid and backward compatible; when PCA3[6] = 1, the multiplexing of P20/P21 is determined by PCA3[5:0].	R/W	00
24:23	PC17	Define the port P17 multiplexing configuration by {PCA2[30:29],PCA0[24:23]}: =0000: select IO port =0001: select KEY7 =0010: select TC1_P[1] =0011: select TC input, valid for TC0/TC1 at the same time. =0100: select SPI3_MOSI =0101: select TRIG_OUT(intelligent micro break demand) =0110: select analog input AIN5 = Other: Reserved Backwards compatible by default	R/W	00
22:21	PC16	Define the port P16 multiplexing configuration by {PCA2[28:27],PCA0[22:21]}: =0000: select IO port;	R/W	00

		=0001: select KEY6 =0010: select TC1_N[1] =0011: select TC input, valid for TC0/TC1 at the same time. =0100: select SPI3_MISO =0101: select TRIG_OUT(intelligent micro break demand) = Other: Reserved Backwards compatible by default		
20:19	PC15	Define the port P15 multiplexing configuration by {PCA2[26:25],PCA0[20:19]}: =0000：select IO port =0001：select KEY5 =0010：select TC1_P[0] =0011：select TC input, valid for TC0/TC1 at the same time. =0100：select SPI3_SCLK =0101：select INT7 = Other: Reserved Note: When both P37 and P15 are selected as INT7, P37 has higher priority than P15 and P15 input is invalidated Backwards compatible by default	R/W	00
18:17	PC14	Define the port P14 multiplexing configuration by {PCA2[24:23],PCA0[18:17]}: = 0000: select IO port = 0001: select KEY4 = 0010: select TC1_N[0] = 0011: select TC input, valid for TC0/TC1 at the same time. = 0100: select SPI3_SCSN = 0101: select INT6 = Other: Reserved Note: When both P36 and P14 are selected as INT7, P36 has higher priority than P14 and P14 input is invalidated Backwards compatible by default	R/W	00
16:15	PC13	Define the port P13 multiplexing configuration by {PCA2[22:21],PCA0[16:15]}: = 0000: select IO port = 0001: select KEY3 = 0010: select TC0_P[1] = 0011: select TC input, valid for TC0/TC1 at the same time = 0100: select IOCNT_OUT2 =0101: select ADC_CLKO = 0110: select IA_IN = 0111: Reserved Other: reserved Backwards compatible by default	R/W	00
14:13	PC12	Define the port P12 multiplexing configuration by	R/W	00

		{PCA2[20:19],PCA0[14:13]}: =0000: select IO port = 0001: select KEY2 =0010: select TC0_N[1]] =0011: select TC input, valid for TC0/TC1 at the same time = 0100: select IB_IN = 0101: Reserved =0110: select CF_OUT4 =0111: select D2F_OUT4 = 1000: select IOCNT_OUT4 = 1001: select TRIG_OUT (intelligent micro break demand) = Other: Reserved Backwards compatible by default		
12:11	PC11	Define the port P11 multiplexing configuration by {PCA2[18:17],PCA0[12:10]}: =0000: select IO port = 0001: select KEY1 = 0010: select TC0_P[0] =0011: select TC input, valid for TC0/TC1 at the same time. =0100: select IA_IN = 0101: Reserved =0110: select CF_OUT3 =0111: select D2F_OUT3 = 1000: select IOCNT_OUT3 = 1001: select TC1_P[1] (Intelligent micro break demand) = Other: Reserved Backwards compatible by default	R/W	00
10:9	PC10	Define the port P10 multiplexing configuration by {PCA2[16:15],PCA0[10:9]}: =0000: select IO port = 0001: select KEY0 =0010: select TC0_N[0] =0011: select TC input, valid for TC0/TC1 at the same time =0100: select IA_IN =0101: select IB_IN =0110: select CF_OUT2 =0111: select D2F_OUT2 = 1000: select IOCNT_OUT2 = 1001: select TC1_N[1] (Intelligent micro break demand) = Other: Reserved Backwards compatible by default	R/W	00
8	KEY 4 _SEL	See bit[6] of the PCA0 register for specific definition	R/W	0
7	---	reserve	R/W	0
6	PC04	Define port P04 multiplexing configuration by	R/W	0

		{PCA2[11:10],PCA0[8],PCA0[6]}: =0000: select IO port = 0001: select analog input AIN4/LVDIN = 001x: P04 selected as KEY4 =0100: select IA_IN =0101: select IB_IN = Other: Reserved Note: When both P14 and P04 are selected as KEY4, P14 has higher priority than P04 and P04 input is invalid Backwards compatible by default		
5	PC03	The multiplexing configuration of port P03 is defined by {PCA2[9:7],PCA0[5]}: =0000: select IO port = 0001: select analog input AIN3/CMP2 = 0010: select IA_IN = 0011: Reserved = Other: Reserved		
4	PC02	The multiplexing configuration of port P02 is defined by {PCA2[6:4],PCA0[4]}: =0000: select IO port = 0001: select analog input AIN2/CMP1 = 0010: select IA_IN = 0011: select IB_IN = Other: Reserved		
3:2	PC01	Define the port P01 multiplexing configuration by {PCA2[3:2],PCA0[3:2]}: =0000: select IO port = 0001: select analog input AIN1 = 0010: select KEY3 =0011: select TX2 =0100: select IA_IN = 0101: Reserved =0110: select TC1_N[1]. = Other: Reserved Note: When P13 is selected as KEY3, P13 has higher priority than P01 and P01 input is invalid	R/W	0
1:0	PC00	Define port P00 multiplexing configuration by {PCA2[1:0],PCA0[1:0]}: =0000: select IO port = 0001: select analog input AIN0 =0010: select KEY2 =0011: select RX2 =0100: select IA_IN =0101: select IB_IN	R/W	0

		=0110: Select TC1_P[1] = Other: Reserved Note: When P12 is selected as KEY2, P12 priority is higher than P00 and P00 input is invalid		

13.3.4 PA port reuse 1 register PCA1(0x0C)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PC37_2	See bit [15:14] of the PCA1 register for specific definitions.	R/W	0
29:28	PC36_2	See bit [13:12] of the PCA1 register for specific definitions.	R/W	0
27:26	PC35_2	See bits [11:10] of the PCA1 register for specific definitions.	R/W	0
25:24	PC34_2	See bits [9:8] of the PCA1 register for specific definitions.	R/W	0
23:22	PC33_2	See bits [7:6] of the PCA1 register for specific definitions.	R/W	0
21:20	PC32_2	See bits [5:4] of the PCA1 register for specific definitions.	R/W	0
19:18	PC31_2	See bits [3:2] of the PCA1 register for specific definitions.	R/W	0
17:16	PC30_2	See bit [1:0] of the PCA1 register for specific definitions.	R/W	0
15:14	PC37[1:0]	Define the port P37 multiplexing configuration by {PCA1[31:30],PCA1[15:14]}: =0000: Selected as IO port = 0001: Reserved = 001x: Selected for high-frequency transistor pin HOSCI = 0100: Reserved = Other: Reserved Note: As long as any of PC36[1] and PC37[1] is high, then it is selected as HOSC	R/W	0
13:12	PC36[1:0]	{PCA1[29:28],PCA1[13:12]} define the port P36 multiplexing configuration: =0000: Selected as IO port = 0001: Reserved = 001x: Selected for high-frequency transistor pin HOSCO = 0100: Reserved = Other: Reserved Note: As long as any of PC36[1] and PC37[1] is high, then it is selected as HOSC	R/W	0
11:10	PC35[1:0]	{PCA1[27:26],PCA1[11:10]} define the port P35 multiplexing configuration: =0000: Selected as IO port =0001: Selected as external interrupt input port INT5 = 0010: Selected as TC input = 0011: Selected as D2F_OUT4 = 0100: Selected as IOCNT_OUT4 =0101: Selected as ADC_CLKO =0110: Selected as IA_IN =0111: Selected as IB_IN	R/W	0

		= 1000: Selected as TRIG_OUT = 1001: Selected as CF_OUT4 = Other: Reserved		
9:8	PC34[1:0]	{PCA1[25:24],PCA1[9:8]} define the port P34 multiplexing configuration: =0000: Selected as IO port =0001: Selected as external interrupt input port INT4 = 0010: Selected as apparent energy pulse output SF_OUT = 0011: Selected as D2F_OUT3 = 0100: Selected as CF_OUT3 =0101: Selected as IOCNT_OUT3 =0110: Selected as ADC_CLKO =0111: Selected as IA_IN = 1000: Selected as TRIG_OUT = Other: Reserved	R/W	0
7:6	PC33[1:0]	{PCA1[23:22],PCA1[7:6]} define the port P33 multiplexing configuration: =0000: Selected as IO port =0001: Selected as external interrupt input port INT3 = 0010: Selected as TC input =0011: Selected as ADC_CLKO = 0100: Selected as IOCNT_OUT3 =0101: Selected as IA_IN =0110: Selected as IB_IN = Other: Reserved	R/W	0
5:4	PC32[1:0]	{PCA1[21:20],PCA1[5:4]} define the port P32 multiplexing configuration: =0000: Selected as IO port =0001: Selected as external interrupt input port INT2 = 0010: Selected as RTC output RTC_OUT (default selection is RTC output) =0011: Selected as KEY5 = 0100: Selected as ADC_CLKO =0101: Selected as TRIG_OUT =0110: Selected as CF_OUT1 =0111: Selected as D2F_OUT1 =1000: selected as TC1_N[1] = 1001: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	10
3:2	PC31[1:0]	{PCA1[19:18],PCA1[3:2]} define the port P31 multiplexing configuration: =0000: Selected as IO port =0001: Selected as external interrupt input port INT1 = 0010: Selected as TC input	R/W	0

		=0011: Selected as RX4 = 0100: Selected as RTC_OUT =0101: Selected as ADC_CLKO =0110: Selected as TRIG_OUT = 0111: Reserved = 1000: Selected as CF_OUT0 = 1001: Selected as D2F_OUT0 =1010: Selected as TC1_P[1] =1011: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved		
1:0	PC30[1:0]	Define the port P30 multiplexing configuration by {PCA1[17:16],PCA1[1:0]}: =0000: Selected as IO port =0001: Selected as external interrupt input port INT0 = 0010: Selected as TC input =0011: Selected as TX4 = 0100: Selected as RTC_OUT =0101: Selected as ADC_CLKO =0110: Selected as TRIG_OUT = 0111: Reserved =1000: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	0

13.3.5 PA port reuse register 2(0x8C）(new)

Bit	Name	Description	R/W Sign	Reset Value
31	---	Reserved	R	0
30:29	PC17_2	See bits[24:23] of the PCA0 register for specific definitions	R/W	0
28:27	PC16_2	See bits[22:21] of the PCA0 register for specific definitions.	R/W	0
26:25	PC15_2	See bits[20:19] of the PCA0 register for specific definitions.	R/W	0
24:23	PC14_2	See bits[18:17] of the PCA0 register for specific definitions.	R/W	0
22:21	PC13_2	See bits[16:15] of the PCA0 register for specific definitions	R/W	0
20:19	PC12_2	See bits[14:13] of the PCA0 register for specific definitions.	R/W	0
18:17	PC11_2	See bits[12:11] of the PCA0 register for specific definitions.	R/W	0
16:15	PC10_2	See bit[10:9] of the PCA0 register for specific definitions	R/W	0
14:12	PC05_2	See bit[7] of the PCA0 register for specific definitions	R/W	0
11:10	PC04_2	See bit[6] of the PCA0 register for specific definition	R/W	0
9:7	PC03_2	See bit[5] of the PCA0 register for specific definition	R/W	0

6:4	PC02_2	See bit[4] of the PCA0 register for specific definition	R/W	0
3:2	PC01_2	See bits[3:2] of the PCA0 register for specific definitions	R/W	0
1:0	PC00_2	See bit[1:0] of the PCA0 register for specific definitions	R/W	0

13.3.6 PA port reuse register 3（0x90）(new)

Bit	Name	Description	R/W Sign	Reset Value
31:29	---	Reserved	R	0
28	UART2_SEL_2	See bits[31:30] of the PCA0 register for specific definitions.	R/W	0
27	PC267_2	=0: P26/P27 specific definition is determined by bit[28] of PCA0 register =1: P26/P27 specific definitions are determined by bit[26:21] of the PCA3 register	R/W	0
26:24	PC27_2	Define port P27 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as TX3 = 010: Selected as TX2 = 011: Selected as TRIG_OUT = 100: Reserved =101: Selected as TC1_N[1]. = Other: reserved	R/W	0
23:21	PC26_2	Define port P26 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as RX3 = 010: Selected as RX2 = 011: Selected as TRIG_OUT = 100: Reserved = 101: Selected as TC1_P[1]. = Other: reserved	R/W	0
20	PC245_2	=0: P24/P25 specific definition is determined by bit[27] of PCA0 register =1: P24/P25 specific definitions are determined by bit[19:14] of PCA3 registers	R/W	0
19:17	PC25_2	Define port P25 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as TX2 = 010: Reserved =011: Selected as TC1_N[1]. = Other: Reserved	R/W	0
16:14	PC24_2	Define port P24 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as RX2 = 010: Reserved =011: Selected as TC1_P[1].	R/W	0

		= Other: Reserved		
13	PC223_2	=0: P22/P23 specific definition is determined by bit[26] of PCA0 register =1: P22/P23 specific definitions are determined by bit[12:7] of the PCA3 register	R/W	0
12:10	PC23_2	Define port P23 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as TX1 = 010: Selected as TX2 = 011: Selected as SPI1_MOSI = 100: Selected as SPI3_MOSI = 101: Reserved = Other: reserved	R/W	0
9:7	PC22_2	Define port P22 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as RX1 = 010: Selected as RX2 = 011: Selected as SPI1_MISO = 100: Selected as SPI3_MISO = 101: Reserved = 110: Selected as TRIG_OUT = Other: Reserved	R/W	0
6	PC201_2	=0: P20/P21 specific definition is determined by bit[25] of PCA0 register =1: P20/P21 specific definitions are determined by bit[5:0] of PCA3 register	R/W	0
5:3	PC21_2	Define port P21 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as TX0 = 010: Selected as TX2 = 011: Selected as SPI1_SCLK = 100: Selected as SPI3_SCLK = 101: Reserved =110: Selected as TC1_P[1] = Other: Reserved	R/W	0
2:0	PC20_2	Define port P20 multiplexing configuration 2: = 000: Selected as GPIO = 001: Selected as RX0 = 010: Selected as RX2 = 011: Selected as SPI1_SCSN = 100: Selected as SPI3_SCSN = 101: Reserved =110: Selected as TC1_N[1] = 111: Selected as TRIG_OUT	R/W	0

13.3.7 PA port pull-up selection register (0x10)

Note: When the IO port is in output mode or analog PAD mode, the PIN pull-up is not enabled regardless of how the PU register is configured.

Bit	Name	Description	R/W Sign	Reset Value
31:24	PU37~PU30	Defines the port pull-up configuration: = 0: No pull-up selected; = 1: Select the pull-up; P30 default pull-up on	R/W	00
23:16	PU27~PU20	Defines the port pull-up configuration: = 0: No pull-up selected; = 1: Select the pull-up; Note: P24 and P25 are used as SWD default pull-up enables.	R/W	30
15:8	PU17~PU10	Defines the port pull-up configuration: = 0: No pull-up selected; = 1: Select the pull-up;	R/W	00
7:5	--	reservations	R	0
4:0	PU04~PU00	Defines the port pull-up configuration: = 0: No pull-up selected; = 1: Select the pull-up;	R/W	00H

13.3.8 PA port input mode configuration (0x14)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIL27~PIL20	Define port P20~P27 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
23:16	PIL17~PIL10	Define port P10~P17 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
15:8	PID27~PID20	Defines whether ports P20~P27 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00
7:0	PID17~PID10	Defines whether ports P10~P17 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00

13.3.9 PA port input mode configuration PIMA2 (0xB0) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:16	--	Reserved	R	0
15:8	PIL37~PIL30	Define port P30~P37 input buffer type:	R/W	00

		=0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;		
7:0	PID37~PID30	Defines whether ports P30~P37 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00

13.3.10 PA port input enable selection (0x18)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIE37~PIE30	Input Enable: = 1: Do not enable inputs; =0: Enable input; Note: BOOTROM needs to be set to input enable after the P30 is powered up to facilitate the ISP to perform detection.	R/W	FF
23:16	PIE27~PIE20	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
15:8	PIE17~PIE10	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
7:5	Reserved	reservations	R	0
4:0	PIE04~PIE00	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	3F

13.4 PB port

13.4.1 PB port mode register PMB (input or output) (0x1C)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PM77~PM70	=0 Output Mode =1 Input mode	R/W	FF
23:16	PM67~PM60	=0 Output Mode =1 Input mode	R/W	FF
15:8	PM57~PM50	=0 Output Mode =1 Input mode	R/W	FF
7:0	PM47~PM40	=0 Output Mode =1 Input mode	R/W	FF

When the IO port is set to 7816 port or SPI port, the direction register does not work and is controlled by the communication module itself.

13.4.2 PB port data register PB (0x20)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
23:16	P67~P60	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P57~P50	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:0	P47~P40	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00

13.4.3 PB port multiplexing register PCB (0x24)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PC77~PC70	PC77~PC70 define the port multiplexing configuration: = 0: Selected as IO port = 1: Selected as SEG	R/W	00
23:16	PC67~PC60	PC67~PC60 define the port multiplexing configuration: = 0: Selected as IO port = 1: Selected as SEG	R/W	00
15	PC57	Define the port P57 multiplexing configuration by {PCB3[15],PCB2[31:30],PCB[15]}: =0000: Selected as IO port = 0001: Selected as apparent energy output SF = 0010: Selected as TCIN = 0011: Selected as CF_OUT2 =0100: Selected as TC1_P[1]. =0101: Selected as IOCNT_OUT2 =0110: Selected as D2F_OUT2 =0111: Selected as ADC_CLKO = Other: Reserved	R/W	0
14	PC56	Define the port P56 multiplexing configuration by {PCB3[14],PCB2[29:28],PCB[14]}: =0000: Selected as IO port = 0001: Selected as zero crossing output ZX_OUT = 0010: Selected as TCIN =0011: Selected as INT2 =0100: Selected as TC1_N[1]. =0101: Selected as RTC_OUT	R/W	0

		=0110: Selected as IOCNT_OUT0 =0111: Selected as ADC_CLKO =1000: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved Note: When both P32 and P56 are selected as INT2, P32 has higher priority than P56 and P56 input is invalidated		
13	PC55	Define the port P55 multiplexing configuration by {PCB3[13],PCB2[27:26],PCB[13]}: =0000: Selected as IO port = 0001: Selected as TX5 = 0010: Selected as TCIN = 0011: Selected as IA_IN =0100: Selected as TC1_P[0]. =0101: Selected as IB_IN =0110: Selected as SPI1_MOSI = 0111: Reserved = Other: Reserved	R/W	0
12	PC54	Define the port P54 multiplexing configuration by {PCB3[12],PCB2[25:24],PCB[12]}: =0000: Selected as IO port = 0001: Selected as RX5 = 0010: Selected as TCIN = 0011: Selected as IA_IN =0100: Selected as TC1_N[0]. = 0101: Reserved =0110: Selected as SPI1_MISO = 0111: Reserved = Other: Reserved	R/W	0
11	PC53	Define the port P53 multiplexing configuration by {PCB3[11],PCB2[23:22],PCB[11]}: =0000: Selected as IO port = 0001: Selected as I2C_SDA = 0010: Selected as TCIN = 0011: Selected as IA_IN =0100: Selected as TC0_P[1]. =0101: Selected as IB_IN =0110: Selected as SPI1_SCLK = 0111: Reserved	R/W	0
10	PC52	Define the port P52 multiplexing configuration by {PCB3[10],PCB2[21:20],PCB[10]}: =0000: Selected as IO port = 0001: Selected as I2C_SCL = 0010: Selected as TCIN =0011: Selected as ADC_CLKO	R/W	0

		=0100: Selected as TC0_N[1]. = 0101: Reserved =0110: Selected as SPI1_SCSN = 0111: Reserved Note: PC52 is only valid in SPI slave mode, do not configure it to 1 in SPI master mode.		
9	PC51	Define the port P51 multiplexing configuration by {PCB3[9],PCB2[19:18],PCB[9]}: =0000: Selected as IO port = 0001: Selected as reactive power pulse output QF = 0010: Selected as RTC_OUT = 0011: Selected as CF_OUT1 = 0100: Selected as active power pulse output PF =0101: Selected as IOCNT_OUT1 =0110: Selected as apparent power pulse output SF =0111: Selected as D2F_OUT1 =1000: Selected as Perpetual Calendar Seconds Output RTC1S	R/W	1
8	PC50	Define the port P50 multiplexing configuration by {PCB3[8],PCB2[17:16],PCB[8]}: =0000: Selected as IO port = 0001: Selected as active power pulse output PF = 0010: Selected as RTC_OUT = 0011: Selected as CF_OUT0 = 0100: Selected as apparent power pulse output SF =0101: Selected as IOCNT_OUT0 = 0110: Selected as reactive power pulse output QF =0111: Selected as D2F_OUT0 =1000: Selected as Perpetual Calendar Seconds Output RTC1S	R/W	1
7	PC47	Define the port P47 multiplexing configuration by {PCB3[7],PCB2[15:14],PCB[7]}: =0000: Selected as IO port = 0001: Selected as SPI0_MOSI = 0010: Selected as TX4 = 0011: Reserved =0100: Selected as SPI3_MOSI = Other: Reserved	R/W	00
6	PC46	Define the port P46 multiplexing configuration by {PCB3[6],PCB2[13:12],PCB[6]}: =0000: Selected as IO port = 0001: Selected as SPI0_MISO = 0010: Selected as RX4 = 0011: Reserved =0100: Selected as SPI3_MISO = Other: Reserved	R/W	00

5	PC45	Define the port P45 multiplexing configuration by {PCB3[5],PCB2[11:10],PCB[5]}: =0000: Selected as IO port = 0001: Selected as SPI0_SCLK = 0010: Selected as KEY7 =0011: Selected as ADC_CLKO = Other: reserved Note: When both P17 and P45 are selected as KEY7, P17 has higher priority than P45 and P45 input is invalidated	R/W	00
4	PC44	Define the port P44 multiplexing configuration by {PCB3[4],PCB2[9:8],PCB[4]}: =0000: Selected as IO port = 0001: Selected as SPI0_SCSN = 0010: Selected as KEY6 =0011: Selected as ADC_CLKO = Other: reserved Note 1: PC44 is only valid in SPI slave mode, do not configure it to 1 in SPI master mode. Note 2: When both P16 and P44 are selected as KEY6, P16 has higher priority than P44 and P44 input is invalid The p44-47 are close to the analog, in principle it is not recommended to use as spi function to reduce the impact on metering, it is recommended to use the analog opposite side of the gpio as spi.	R/W	00
3	PC43	Define the port P43 multiplexing configuration by {PCB3[3],PCB2[7:6],PCB[3]}: =0000: Selected as IO port = 0001: Selected as 78161_I =0010: Selected as INT5 = 0011: Selected as SPI2_MOSI =0100: Selected as SPI1_MOSI =0101: Selected as IA_IN =0110: Selected as IB_IN = 0111: Reserved Note: When both P35 and P43 are selected as INT5, P35 has a higher priority than P43, and the P43 input is invalid	R/W	0
2	PC42	Define the port P42 multiplexing configuration by {PCB3[2],PCB2[5:4],PCB[2]}: =0000: Selected as IO port = 0001: 78161_IO =0010: Selected as INT4 = 0011: Selected as SPI2_MISO = 0100: Selected as SPI1_MISO =0101: Selected as IA_IN	R/W	0

		= 0110: Reserved = 0111: Reserved Note: When both P34 and P42 are selected as INT4, P34 has higher priority than P42 and P42 input is invalid		
1	PC41	Define the port P41 multiplexing configuration by {PCB3[1],PCB2[3:2],PCB[1]}: =0000: Selected as IO port = 0001: Selected as 78160_IO =0010: Selected as INT3 = 0011: Selected as SPI2_SCLK = 0100: Selected as SPI1_SCLK =0101: Selected as IA_IN =0110: Selected as IB_IN = 0111: Reserved Note: When both P33 and P41 are selected as INT3, P33 has higher priority than P41 and P41 input is invalid	R/W	0
0	PC40	Define the port P40 multiplexing configuration by {PCB3[0],PCB2[1:0],PCB[0]}: =0000: Selected as IO port = 0001: Selected as 7816_CLK =0010: Selected as INT1 = 0011: Selected as SPI2_SCSN = 0100: Selected as SPI1_SCSN =0101: Selected as ADC_CLKO = Other: Reserved Note 1: PC40 is only valid in SPI slave mode, do not configure it as 1 in SPI master mode. Note 2: When both P31 and P40 are selected as INT1, P31 has higher priority than P40 and P40 input is invalid		0

13.4.4 PB port multiplexes register 2(modified)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PC57_2	See bit [15] of the PCB register for specific definitions.	R/W	00
29:28	PC56_2	See bit [14] of the PCB registers for specific definitions.	R/W	00
27:26	PC55_2	See bit [13] of the PCB register for specific definitions.	R/W	00
25:24	PC54_2	See bit [12] of the PCB register for specific definitions.	R/W	00
23:22	PC53_2	See bit [11] of the PCB registers for specific definitions.	R/W	00
21:20	PC52_2	See bit [10] of the PCB register for specific definitions.	R/W	00
19:18	PC51_2	See bit [9] of the PCB registers for specific definitions.	R/W	00
17:16	PC50_2	See bit [8] of the PCB register for specific definitions.	R/W	00
15:14	PC47_2	See bit [7] of the PCB register for specific definitions.	R/W	00
13:12	PC46_2	See bit [6] of the PCB register for specific definitions.	R/W	00
11:10	PC45_2	See bit [5] of the PCB register for specific definitions.	R/W	00

9:8	PC44_2	See bit [4] of the PCB register for specific definitions.	R/W	00
7:6	PC43_2	See bit [3] of the PCB register for specific definitions.	R/W	00
5:4	PC42_2	See bit [2] of the PCB registers for specific definitions.	R/W	00
3:2	PC41_2	See bit [1] of the PCB register for specific definitions.	R/W	00
1:0	PC40_2	See bit[0] of the PCB register for specific definitions	R/W	00

13.4.5 PB port multiplexing register 3 PCB3 (0x94) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:16	--	Reserved	R	0
15	PC57_3	See bit [15] of the PCB register for specific definitions.	R/W	
14	PC56_3	See bit [14] of the PCB register for specific definitions.	R/W	0
13	PC55_3	See bit [13] of the PCB register for specific definitions.	R/W	0
12	PC54_3	See bit [12] of the PCB register for specific definitions.	R/W	0
11	PC53_3	See bit [11] of the PCB registers for specific definitions.	R/W	0
10	PC52_3	See bit [10] of the PCB register for specific definitions.	R/W	0
9	PC51_3	See bit [9] of the PCB registers for specific definitions.	R/W	0
8	PC50_3	See bit [8] of the PCB register for specific definitions.	R/W	0
7	PC47_3	See bit [7] of the PCB register for specific definitions.	R/W	0
6	PC46_3	See bit [6] of the PCB register for specific definitions.	R/W	0
5	PC45_3	See bit [5] of the PCB register for specific definitions.	R/W	0
4	PC44_3	See bit [4] of the PCB register for specific definitions.	R/W	0
3	PC43_3	See bit [3] of the PCB register for specific definitions.	R/W	0
2	PC42_3	See bit [2] of the PCB registers for specific definitions.	R/W	0
1	PC41_3	See bit [1] of the PCB register for specific definitions.	R/W	0
0	PC40_3	See bit[0] of the PCB register for specific definitions	R/W	0

13.4.6 PUB port pull-up selection register (0x28）

Bit	Name	Description	R/W Sign	Reset Value
31:24	PU77~PU70	PU77~PU70 define whether the P7 port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	00
23:16	PU67~PU60	PU67~PU60 define whether the P6 port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	00
15:8	PU57~PU50	PU57~PU50 define whether the P5 port is internally connected to pull-up: =0: Not connected to pull-up; = 1: Inside pull-up.	R/W	00
7:0	PU47~PU40	PU47~PU40 define whether the P4 port is internally connected to	R/W	00

		pull-up: =0: Not connected to pull-up; = 1: Inside pull-up.		

13.4.7 PB port input mode register PIMB (0x2C) (modified)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIL57~PIL50	Define port P50~P57 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
23:16	PIL47~PIL40	Define port P40~P47 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
15:8	PID57~PID50	Defines whether ports P50~P57 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00
7:0	PID47~PID40	Defines whether ports P40~P47 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00

13.4.8 PB port input enable register PIEB (0x30)

Bit	Name	Description	R/W Sign	Reset Value
31:24	PIE77~PIE70	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
23:16	PIE67~PIE60	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
15:8	PIE57~PIE50	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
7:0	PIE47~PIE40	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF

13.5 PC port

13.5.1 PC port mode register PMC (input or output) (0x34)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PM117~PM116	=0 Output Mode =1 Input mode	R/W	3
29:28	Reserved	Reserved, please do not configure	R/W	3

27:24	PM113~PM110	=0 Output Mode =1 Input mode	R/W	F
23:20	Reserved	Reserved, please do not configure	R/W	F
19:16	PM103~PM100	=0 Output Mode =1 Input mode	R/W	F
15:8	PM97~PM90	=0 Output Mode =1 Input mode	R/W	FF
7:0	PM87~PM80	=0 Output Mode =1 Input mode	R/W	FF

13.5.2 PC port data register PC (0x38)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PM117~PM116	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	0
29:28	Reserved	Reserved, please do not configure	R/W	0
27:24	P113~P110	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
23:20	Reserved	Reserved, please do not configure	R/W	0
19:16	P103~P100	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P97~P90	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:0	P87~P80	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00

13.5.3 PC port reuse register (0x3C) (modified)

Bit	Name	Description	R/W Sign	Reset Value
31:29	Reserved	----------	R	0
28	SPI_MUX	SPI_MUX defines whether port P11 or P4 is used as the SPI0 interface: =0: Select P44~P47 as SPI0 interface; =1: Select P110~P113 as SPI0 interface.	R/W	0
27	PC113	{PCC3[11:9],PCC[27]} define the configuration of P113 =0000: Selected as IO port = 0001: Selected as SPI0_MOSI = 0010: Selected as SPI2_MOSI = 0011: Selected as SPI3_MOSI	R/W	0

		= Other: Reserved		
26	PC112	{PCC3[8:6],PCC[26]} define the configuration of P112 =0000: Selected as IO port = 0001: Selected as SPI0_MISO = 0010: Selected as SPI2_MISO = 0011: Selected as SPI3_MISO = Other: Reserved	R/W	0
25	PC111	{PCC3[5:3],PCC[25]} define the configuration of P111 =0000: Selected as IO port = 0001: Selected as SPI0_SCLK = 0010: Selected as SPI2_SCLK = 0011: Selected as SPI3_SCLK = Other: Reserved	R/W	0
24	PC110	Define the configuration of P110 by {PCC3[2:0],PCC[24]} =0000: Selected as IO port = 0001: Selected as SPI0_SCSN = 0010: Selected as SPI2_SCSN = 0011: Selected as SPI3_SCSN = Other: Reserved Note 1: PC110 is only valid in SPI slave mode, do not configure it in SPI master mode 1. Note 2: Ports P40~P43 and P110~P113 cannot be multiplexed as SPI2 at the same time. Note 3: Ports P14~P17, P20~P23 and P110~P113 cannot be multiplexed as SPI3 at the same time.	R/W	0
23	PC107	Port P107 multiplexing configuration defined by {PCC2[23:21],PCC[23]} =0000: Retain IO function, user don't configure it = 0001: Reserved = Other: Reserved Note: Always valid as ADC analog input, no need to configure multiplexing	R/W	0
22	PC106	Port P106 multiplexing configuration defined by {PCC2[20:18],PCC[22]} =0000: Retain IO function, user don't configure it = 0001: IB_IN = Other: Reserved Note 1: As ADC analog input is always valid, no need to configure multiplexing; when used as IB_IN port, it only supports the input function, and can be externally potted with ADC 1bit signal.	R/W	0
21	PC105	Port P105 multiplexing configuration defined by {PCC2[17:15],PCC[21]} =0000: Retain IO function, user don't configure it = 0001: Reserved	R/W	0

		= Other: Reserved Note: Always valid as ADC analog input, no need to configure multiplexing		
20	PC104	Port P104 multiplexing configuration defined by {PCC2[14:12],PCC[20]} =0000: Retain IO function, user don't configure it = 0001: Reserved = Other: Reserved Note 1: Always valid as ADC analog input, no configuration multiplexing required;	R/W	0
19:16	PC103~PC100	PC103~PC100 Define the port multiplexing configuration: =0: Selected as IO port; = 1: Selected as SEG.	R/W	00
15:8	PC97~PC90	PC97~PC90 Define the port multiplexing configuration: =0: Selected as IO port; = 1: Selected as SEG.	R/W	00
7:0	PC87~PC85	PC87~PC85 define the port multiplexing configuration: =0: Selected as IO port; = 1: Selected as SEG.	R/W	0
4	PC84	Port P84 multiplexing configuration defined by {PCC4[14:12],PCC[4]} =0000: Selected as IO port = 0001: Selected as SEG = 0010: Selected as SPI3_SCLK (open drain pin) = Other: Reserved	R/W	0
3	PC83	Port P83 multiplexing configuration defined by {PCC4[11:9],PCC[3]} =0000: Selected as IO port = 0001: Selected as SEG = 0010: Selected as SPI3_SCSN (open drain pin) = Other: Reserved	R/W	0
2	PC82	PC82 Defines the port P82 multiplexing configuration: =0: Selected as IO port; = 1: Selected as SEG.	R/W	0
1	PC81	Port P81 multiplexing configuration defined by {PCC4[5:3],PCC[1]} =0000: Selected as IO port = 0001: Selected as SEG = 0010: Selected as SDA = Other: Reserved	R/W	0
0	PC80	Port P80 multiplexing configuration defined by {PCC4[2:0],PCC[0]} =0000: Selected as IO port = 0001: Selected as SEG	R/W	0

		= 0010: Selected as SCL = Other: Reserved		

13.5.4 PC port multiplexing register 2 PCC2 (0x98) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	0
23:21	PC107_2	See bit[23] of the PCC register for specific definitions	R/W	0
20:18	PC106_2	See bit[22] of the PCC register for a specific definition	R/W	0
17:15	PC105_2	See bit[21] of the PCC register for specific definitions	R/W	0
14:12	PC104_2	See bit[20] of the PCC register for the specific definition	R/W	0
11:9	PC103_2	Reserved	R	0
8:6	PC102_2	Reserved	R	0
5:3	PC101_2	Reserved	R	0
2:0	PC100_2	Reserved	R	0

13.5.5 PC port multiplexing register 3 PCC3 (0x9C) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:28	---	Reserved	R	0
27:24	PC117	PC117 Definition Port P117 Multiplexing Configuration =0000: Selected as IO port =0001: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	0
23:20	PC116	PC116 Definition Port P116 Multiplexing Configuration =0000: Selected as IO port (open drain pin, only supports open drain applications) = 0001: Selected as analog input AIN6 = Other: Reserved	R/W	0
19:16	PC115	PC115 Defined Port P115 Multiplexing Configuration =0000: Retain IO function, user don't configure it = 0001: Reserved = Other: Reserved Note: Always valid as ADC analog input, no need to configure multiplexing	R/W	0
15:12	PC114	PC114 Definition Port P114 Multiplexing Configuration =0000: Retain IO function, user don't configure it = 0001: IA_IN = Other: Reserved Note 1: As an ADC analog input is always valid and does not need to be configured for multiplexing; when used as IA_IN, only the input function is supported.	R/W	0
11:9	PC113_2	See bit[27] of the PCC register for specific definitions	R/W	0
8:6	PC112_2	See bit[26] of the PCC register for specific definitions	R/W	0

5:3	PC111_2	See bit[25] of the PCC register for specific definitions	R/W	0
2:0	PC110_2	See bit[24] of the PCC register for specific definitions	R/W	0

13.5.6 PC port multiplexing register 4 PCC4 (0xA0) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R	0
23:21	PC87_2	Reserved	R	0
20:18	PC86_2	Reserved	R	0
17:15	PC85_2	Reserved	R	0
14:12	PC84_2	See bit[4] of the PCC register for specific definitions	R/W	0
11:9	PC83_2	See bit[3] of the PCC register for specific definitions	R/W	0
8:6	PC82_2	Reserved	R	0
5:3	PC81_2	See bit[1] of the PCC register for specific definition	R/W	0
2:0	PC80_2	See bit[0] of the PCC register for specific definitions	R/W	0

13.5.7 PUC port pull-up selection register (0x40)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PU117~PU116	PU117~PU116 define whether the port is internally connected to pull-up: =0: Not connected to pull-up; = 1: Inside pull-up.	R/W	00
29:28	---	Reserved	R	00
27:24	PU113~PU110	PU113~PU110 define whether the port is internally connected to pull-up or not: =0: Not connected to pull-up; = 1: Inside pull-up.	R/W	00
23:20	Reserved	-----	R	0
19:16	PU103~PU100	PU103~PU100 define whether the port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	0
15:8	PU97~PU90	PU97~PU90 define whether the port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	00
7:0	PU87~PU80	PU87~PU80 define whether the port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	00

13.5.8 PC port input enable register PIEC (0x44) (modified)

Bit	Name	Description	R/W Sign	Reset Value
31:30	PIE117~PIE116	Input Enable: = 0: Do not enable the input; = 1: Enable input;	R/W	3
29:28	--	Reserved	R/W	3
27:24	PIE113~PIE110	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	F
23:20	Reserved	-----	R/W	F
19:16	PIE103~PIE100	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	F
15:8	PIE97~PIE90	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
7:0	PIE87~PIE80	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF

13.5.9 PC port input mode register PIMC (0x48)

Bit	Name	Description	R/W Sign	Reset Value
31:16	---	预留	R	0
15:14	PIL117~PIL116	Define port P117~P116 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	0
13:12	---	Reserved	R/W	0
11:10	---	Reserved	R/W	0
9:8	---	Reserved	R/W	0
7:4	PIL113~PIL110	Define port P113~P110 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
3:0	PID113~PID110	Defines whether ports P113~P110 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode;	R/W	00

13.6 PD port (new)

13.6.1 PD port mode register PMD (0x50) (input or output) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	FF

23:16	PM147~PM140	=0 Output Mode =1 Input mode	R/W	FF
15:8	PM137~PM130	=0 Output Mode =1 Input mode	R/W	FF
7:0	PM127~PM120	=0 Output Mode =1 Input mode	R/W	FF

13.6.2 PD port data register PD (0x54) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	00
23:16	P147~P140	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
15:8	P137~P130	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00
7:0	P127~P120	Define data needed in the chip output port. If you read in the input mode, the pin level is read. If you read in the output mode, then read the output latch value	R/W	00

13.6.3 PD port multiplexing register PCD (0x58) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:14	---	Reserved	R	0
13:8	PC135~PC130	PC137~PC130 Define the port multiplexing configuration: =0: Selected as IO port; = 1: Select LCD voltage pin P133 reserved	R/W	0x3F
7:0	PC127~PC120	PC127~PC120 define the port multiplexing configuration: =0: Selected as IO port; = 1: Selected as SEG/COM P127~P120 correspond to COM7~COM0	R/W	0xFF

13.6.4 PD port multiplexing register PCD2 (0xA8) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:28	PC147	PC147 defines the P147 port multiplexing configuration: =0000: Selected as IO port; =0001: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	00
27:24	PC146	PC146 defines the P146 port multiplexing configuration: =0000: Selected as IO port; = 0001: Selected as ADC_CLKO	R/W	00

		= 0010: Selected as intelligent micro break TRIG_OUT = 0011: Selected as SPI2_MOSI = Other: Reserved		
23:20	PC145	PC145 defines the P145 port multiplexing configuration: =0000: Selected as IO port; (open-drain pin, only supports open-drain applications) = 0001: Selected as ADC_CLKO = 0010: Selected as intelligent micro break TRIG_OUT = 0011: Selected as SPI2_MISO = Other: Reserved	R/W	00
19:16	PC144	PC144 defines the P144 port multiplexing configuration: =0000: Selected as IO port; = 0001: Selected as ADC_CLKO = 0010: Selected as intelligent micro break TRIG_OUT = 0011: Selected as SPI2_SCLK = Other: Reserved	R/W	00
15:12	PC143	PC143 defines the P143 port multiplexing configuration: =0000: Selected as IO port; = 0001: Selected as ADC_CLKO = 0010: Selected as intelligent micro break TRIG_OUT = 0011: Selected as SPI2_SCSN = Other: Reserved Note 1: PC143 is only valid in SPI slave mode, do not configure it in SPI master mode 1.	R/W	00
11:8	PC142	PC142 defines the P142 port multiplexing configuration: =0000: Selected as IO port; = 0001: Selected as ADC_CLKO = 0010: Selected as intelligent micro break TRIG_OUT =0011: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	0
7:4	PC141	Reserved	R/W	00
3:0	PC140	PC140 defines the P140 port multiplexing configuration: =0000: Selected as IO port; = 0001: Selected as ADC_CLKO = 0010: Selected as intelligent micro break TRIG_OUT =0011: Selected as Perpetual Calendar Seconds Output RTC1S = Other: Reserved	R/W	00

13.6.5 PD port pull-up/down selection register PUD (0x5C) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	00
23:16	PU147~PU140	PU147~PU140 define whether the port is internally connected to pull-up:	R/W	00

		=0: Not connected to pull-up; = 1: Inside pull-up. P141 not supported at this time		
15:8	PU137~PU130	PU137~PU130 define whether the port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down. P133/P136/P137 not supported at this time	R/W	00
7:0	PU127~PU120	PU127~PU120 define whether the port is internally connected to pull-down: = 0: Does not pick up drop-down; = 1: Inside-out drop-down.	R/W	00

13.6.6 PD port input enable PIED (0x84) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	FF
23:16	PIE147~PIE140	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF
15:8	PIE137~PIE130	Input Enable: = 1: Do not enable inputs; =0: Enable input; P133/P136/P137 not supported at this time	R/W	FF
7:0	PIE127~PIE120	Input Enable: = 1: Do not enable inputs; =0: Enable input;	R/W	FF

13.6.7 PD port input mode register PIMD (0x88) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:16	---	Reserved	R	0
15:12	PIL147~PIL144	Define port P147~P144 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC;	R/W	00
11:8	PID147~PID144	Defines whether ports P147~P144 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode; When P145 is used as an output, please configure it to be used in open-drain mode.	R/W	00
7:4	PIL143~PIL140	Define port P143~P140 input buffer type: =0: CMOS buffer, Vil=0.3VCC Vih=0.7VCC; =1: TTL buffer, Vil=0.16VCC Vih=0.4VCC; P141 not supported at this time	R/W	00

3:0	PID143~PID140	Defines whether ports P143~P140 are N-ch open drain outputs: = 0: Normal mode; = 1: N-ch open drain mode; P141 not supported at this time	R/W	00

13.7 COM port

13.7.1 SEGCOM port multiplexing register PCE (0x60)

Bit	Name	Description	R/W Sign	Reset Value
31:4	---	Reserved	R	0
3:0	SEG3/COM7~SEG0/COM4	SEG3/COM7~SEG0/COM4 Define the port multiplexing configuration: = 0: Selected as SEG; = 1: Selected as COM.	R/W	00

13.8 Set and Clear Registers

13.8.1 PA port data set register PASET (0x64)

Bit	Name	Description	R/W Sign	Reset Value
31:30	Reserved	----------	R	0
29:24	P35~P30	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
23:16	P27~P20	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
15:8	P17~P10	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
7:5	---	Reserved	R	0
4:0	P04~P00	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00

Note: The readout value is meaningless

13.8.2 PA Port Clear Setting Register PACLR (0x68)

Bit	Name	Description	R/W Sign	Reset Value
31:30	Reserved	----------	R	00
29:24	P35~P30	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	0
23:16	P27~P20	Clear the Chip Port Status	R/W	00

		0: no effect 1: The port is cleared and outputs a low level		
15:8	P17~P10	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
7:5	---	Reserved	R	0
4:0	P04~P00	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00

Note: The readout value is meaningless

13.8.3 PB port data set register PBSET (0x6C)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
23:16	P67~P60	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
15:8	P57~P50	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
7:0	P47~P00	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00

Note: The readout value is meaningless

13.8.4 PB Port Clear Setting Register PBCLR (0x70)

Bit	Name	Description	R/W Sign	Reset Value
31:24	P77~P70	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	0
23:16	P67~P60	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
15:8	P57~P50	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
7:0	P47~P40	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00

Note: The readout value is meaningless

13.8.5 PC port data set register PCSET (0x74)

Bit	Name	Description	R/W Sign	Reset Value
31:30	P117~P116	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	0
29：28	---	Reserved	R/W	0
27:24	P113~P110	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
23:20	Reserved	----------	R	0
19:16	P103~P100	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	0
15:8	P97~P90	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00
7:0	P87~P80	Set Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00

Note: The readout value is meaningless

13.8.6 PC Port Clear Setting Register PCCLR (0x78)

Bit	Name	Description	R/W Sign	Reset Value
31:30	P117~P116	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	0
29：28	---	Reserved	R/W	0
27:24	P113~P110	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
23:20	Reserved	----------	R	0
19:16	P103~P100	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
15:8	P97~P90	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00
7:0	P87~P80	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00

Note: The readout value is meaningless

13.8.7 PD port data set register PDSET (0x7C) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	00
23:16	P147~P140	Reset Chip Port Status 0: no effect 1: The port is set and outputs a high level P141 not supported at this time	R/W	0
15:8	P137~P130	Reset Chip Port Status 0: no effect 1: The port is set and outputs a high level P133/P136/P137 not supported at this time	R/W	00
7:0	P127~P120	Reset Chip Port Status 0: no effect 1: The port is set and outputs a high level	R/W	00

Note: The readout value is meaningless

13.8.8 PD Port Clear Setting Register PDCLR（0x80）（新增）

Bit	Name	Description	R/W Sign	Reset Value
31:24	---	Reserved	R/W	00
23:16	P147~P140	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level P141 not supported at this time	R/W	00
15:8	P137~P130	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level P133/P136/P137 not supported at this time	R/W	00
7:0	P127~P120	Clear the Chip Port Status 0: no effect 1: The port is cleared and outputs a low level	R/W	00

Note: The readout value is meaningless

13.9 IO Configuration Register

13.9.1 LPUART multiplexing configuration register LURT_CFG (0x100) (new)

LPUART and UARTx Multiplexed IO Configuration Register

Bit	Name	Description	R/W Sign	Reset Value
31:3	---	Reserved	R	0
2:0	LURT_CFG	000：LPUART invalid 001：LPUART multiplexes the IO of UART0 010：LPUART multiplexes the IO of UART1 011：LPUART multiplexes the IO of UART2 100：LPUART multiplexes the IO of UART3	R/W	0

		101：LPUART multiplexes the IO of UART4 110：LPUART multiplexes the IO of UART5 111：Reserved When the LPUART is valid, the multiplexing of the original UARTx is disabled, and the specific multiplexing relationship is configured according to the GPIO chapter.		

13.9.2 IO driver configuration register IOCFG (0x104) (new)

Bit	Name	Description	R/W Sign	Reset Value
31:28	---	Reserved	R	0
27:24	IOCFG_6	P143~P146 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: Driving capacity is 1.5mA, slew rate is slow mode	R/W	1
23:20	IOCFG_5	P110~P113 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: Driving capacity is 1.5mA, slew rate is slow mode	R/W	1
19:16	IOCFG_4	P52~P55 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: Driving capacity is 1.5mA, slew rate is slow mode	R/W	1
15:12	IOCFG_3	P44~P47 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: Driving capacity is 1.5mA, slew rate is slow mode	R/W	1
11:8	IOCFG_2	P40~P43 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: Driving capacity is 1.5mA, slew rate is slow mode	R/W	1
7:4	IOCFG_1	P20~P23 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: driving capacity is 1.5mA, slew rate is slow mode	R/W	1
3:0	IOCFG_0	P14~P17 IO driver configuration: 1: Driving capacity is 3mA, slew rate is fast mode 0: driving capacity is 1.5mA, slew rate is slow mode	R/W	1

13.10 GPIO operation procedure

1、 Configure the system control chapter module enable 1 register MOD1_EN bit 5 is 1 to turn on the GPIO module clock.

2、 Configure the GPIO input and output mode.

3、 Configure the GPIO port data register.

4、 Configure the GPIO port multiplexing function. After selecting the GPIO multiplexing function, the GPIO input and output functions will follow the GPIO multiplexing configuration.

5、 When the MCU is powered by 5v, and the peripheral I2C, SPI or other device operates at 3.3V, you can select GPIO that can be configured as an N-ch open-drain output and an input buffer type with TTL mode.

6、 When using as an input IO port, configure the corresponding bit of the input enable register to 0 to enable the

input. In low power mode, the IO port can be configured as input mode and the input enable can be turned off.

14 External Interrupt Controller INTC (modified)

The SoC has a built-in external interrupt controller (INTC) to handle interrupt requests coming in from the chip pins.

14.1 Features

The external interrupt controller has the following features:

- ◎ Supports mode configuration of 8 external interrupts: upper and lower edges and double edges can be set;
- ◎ Supports external interrupt status indication;
- ◎ Supports software triggering of external interrupts;
- ◎ Supports external interrupt status;
- ◎ Supports external interrupt masking;
- ◎ Supports external interrupt filtering for about 10 system clock cycles;

14.2 Register Description

Module register base address

module Name	physical address	mapping address
INTC	0x40044000	0x40044000

Register Bit of the INTC module

register Name	offset address	description
INTC_CTL	0x0	INTC Control Register
INTC_MODE	0x4	INTC Mode Register
INTC_MASK	0x8	INTC Mask Register
INTC_STA	0xc	INTC Status Register

14.2.1 INTC_CTL (0x0) (modified)

INTC Control Register Address 0x40044000+0x0

Bit	Name	description	Read/Write	reset value
31:08	---	reserved	R	0
8	IRQ_CTL	External interrupt merge function configuration: 0: 8-channel external interrupt INT0~INT7 independent, backward compatible 1: The 8 external interrupts INT0~INT7 share a common interrupt number EXT0, and which external interrupt is generated is determined by querying the STA register interrupt flag.	R/W	0
7:0	Enable	Enable signals, Enable[7:0] correspond to external interrupt requests 7~0, respectively. The corresponding external pins are: P37~P30. 0: Turn off the corresponding external interrupt 1: Enable the corresponding external interrupt	R/W	0

14.2.2 INTC_MODE (0x4)

INTC Mode Register Address 0x40044000+0x4

Bit	Name	description	Read/Write Flag	reset value
31:16	---	reserve	R	0
15:14	MODE7	External Interrupt Request 7 (P37/INT7) Mode Selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
13:12	MODE6	External Interrupt Request 6 (P36/INT6) Mode Selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
11:10	MODE5	External Interrupt Request 5 (P35/INT5) Mode Selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
9:8	MODE4	External interrupt request 4 (P34/INT4) mode selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
7:6	MODE3	External interrupt request 3 (P33/INT3) mode selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
5:4	MODE2	External interrupt request 2 (P32/INT2) mode selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
3:2	MODE1	External interrupt request 1 (P31/INT1) mode selection 00: Rising edge 01: Falling edge 10: Double Edge 11: Reserved	R/W	0
1:0	MODE0	External interrupt request 0 (P30/INT0) mode selection 00: Rising edge 01: Falling edge 10: Double Edge	R/W	0

		11: Reserved		

14.2.3 INTC_MASK (0x8)

INTC Mask Register Address 0x40044000+0x8

Bit	Name	description	Read/Write Flag	reset value
31:8	---	reserve	R	0
7:0	MASK	MASK[7:0] corresponds to external interrupt requests 7 to 0, respectively. 0: Interrupt disabled 1: Interrupt Enable	R/W	0

14.2.4 INTC_STA (0xC)

INTC Status Register Address 0x40044000+0xc

Bit	Name	description	Read/Write Flag	reset value
31:08	---	reserve	R	0
7:0	STA	STA[7:0] corresponds to the external interrupt requests 7~0, respectively. 0: Interrupt event did not occur 1: Interruption event occurs Note: Write 1 and cleared	R/W	0

15 KBI

The SoC has a built-in key interface controller to handle interrupt requests from the chip pins, which can automatically wake up the CPU through interrupts when the CPU is sleeping.

15.1 Features

The key interface controller has the following characteristics:

- ◎ Support 8 keys, corresponding pins are P10/KEY0~P17/KEY7;
- ◎ Supports per-key status query;
- ◎ Supports per-key input filtering with 24ms filtering time;
- ◎ Support for each key can be individually masked interrupt

15.2 Register Description

Table 13- 1 KBI register base address

module Name	physical address	mapping address
KBI	0x40028000	0x40028000

Table 13- 2 KBI Register Bites

register Name	offset address	description
KBI_CTL	0x0	Control register
KBI_SEL	0x4	Selection Register
KBI_DATA	0x8	Data register
KBI_MASK	0xc	Mask Register

15.2.1 Control register KBI _CTL (0x0)

Table 13- 3 KBI control register KBI _CTL

Bit	Name	description	Read/Write	reset value
31:8	---	reserved	R	0
7:0	EN	Enable signals, EN[7:0] correspond to KEY[7:0]. The corresponding external pins are: P17/KEY7~P10/KEY0. 0: Disable the corresponding KEY 1: Enable the corresponding KEY	R/W	0

15.2.2 Selection register KBI _SEL (0x4)

Table 13- 4 KBI Select Register KBI _SEL

Bit	Name	description	Read/Write	reset value
31:8	---	reserved	R	0
7:0	SEL	SEL[7:0] corresponds to KEY[7:0] 0: Rising edge active 1: Falling edge active	R/W	0

15.2.3 Data register KBI _DATA (0x8)

Table 13- 5 KBI Data Register KBI _DATA

Bit	Name	description	Read/Write	reset value
31:8	---	reserved	R	0
7:0	DAT	DAT[7:0] corresponds to KEY[7:0]. Write 1 to	R/W	0

		clear 0: Key not pressed 1: Key pressed		

15.2.4 Mask register KBI _MASK (0xC)

Table 13- 6 KBI Mask Register KBI _MASK

Bit	Name	description	Read/Write	reset value
31:8	---	reserve	R	0
7:0	MASK	MASK[7:0] corresponds to KEY[7:0] 0: Interrupt disabled 1: Interrupt Enable	R/W	0

15.3 KBI Operating Process

1、Configure the KBI enable register KBI_EN to turn on the clock by configuring bit 8 and the corresponding KBI clock bit to 1.

2、Configure the KBI control register KBI_CTL to enable the corresponding KBI.

3、Configure the KBI selection register KBI_SEL to set the corresponding KBI as a rising or falling edge.

4、Configure KBI_MASK to turn on the corresponding interrupt enable and turn on the KBI interrupt NVIC_EnableIRQ(KBI_IRQn);

5、Write the KBI interrupt service program:

```
void KBI_HANDLER(void)
{
    if(KBI->DATA&0x01)
    {

    }
    KBI->DATA = 0xff;
}
```

All KBI interrupts are 1 entry, and need to determine what KBI generated interrupt according to KBI_DATA .

6．Complement

16 UART (modified)

SoC internally installed 6 UART interfaces for external asynchronous serial communication.

16.1 Overview

UART interface controller has the following feature:

- ◎ Six full-duplex UART interfaces;
- ◎ Internally installed baud rate generator, the baud rate is configured to support different;
- ◎ Data bits wide support 5/6/7/8bit;
- ◎ Stop bits can set 1 or 2bit;
- ◎ Optional 38kHz IR modulation;
- ◎ Supports automatic baud rate detection;
- ◎ Supports IR wake;
- ◎ Supports Universal DMA functionality;
- ◎ Supports 300 baud rate@29MHz;
- ◎ All six UARTs support DMA;

16.2 Register Description

Table 14- 1 UART Register Base Address

Module Name	Physical Address	Address Mapping
UART0	0x40000000	0x40000000
UART1	0x40004000	0x40004000
UART2	0x40008000	0x40008000
UART3	0x4000C000	0x4000C000
UART4	0x40018000	0x40018000
UART5	0x4001C000	0x4001C000

Table 14- 2 UART Register Address Offset

Register Name (X=0,1,2,3,4,5)	Address Offset	Description
UARTx_CTL	0x0	UART Control Register
UARTx_BAUD	0x4	UART Baud Rate Configuration Register
UARTx_STAT	0x8	UART Status Indication Register
UARTx_TXD	0xC	UART Transmit Data Register
UARTx_RXD	0x10	UART Receive Data Register
UARTx_DMA_CTL(new)	0x18	UART DMA Control Register
UARTx_DMA_TBADR(new)	0x1c	UART DMA Transmit Starting Address Register
UARTx_DMA_RBAD(new)	0x20	UART DMA Receive Starting Address Register
UARTx_DMA_TLEN(new)	0x24	UART DMA Transmit Length Register
UARTx_DMA_RLEN(new)	0x28	UART DMA Receive Length Register

UARTx_DMA_TADR(new)	0x2c	UART Current Transmitting DMA Address Register
UARTx_DMA_RADR(new)	0x30	UART Current Receiving DMA Address Register
UARTx_DMA_IE(new)	0x34	UART DMA Interrupt Enable Register
UARTx_DMA_FLG(new)	0x38	UART DMA Interrupt Flag Register
UARTx_DMA_TO(new)	0x3C	UART DMA Receive Timeout Configuration Register

Note: The control register and baud rate register cannot be modified during operation.

16.2.1 UART Control Register UARTx_CTL（0x0）

Bit	Name	Description	R/W Sign	Reset Value
31:15	---	Reserved	R	0
14	NEG	UART polarity selection: 0: Positive polarity, the default drive level is high, the polarity of the transmitted/received data remains unchanged. 1: Negative polarity, the default drive level is low, transmit/receive data polarity is reversed.	R/W	0
13	LMSB	LSB/MSB selection method 0: LSB transmission first 1: MSB transmission first Note: When PARS is selected as user-defined check, the check digit is regarded as the highest bit of data expansion. At this time, MSB is selected, and the first bit transmitted will be the check digit.	R/W	0
12	IRSEL	Infrared modulation polarity selection: 0: Positive polarity, that is, low-level modulation output, high level (default state) remains 1: negative polarity, that is, data is inverted, high-level modulation output, low-level hold Note: IRSEL only determines the level of the idle output (inactive level) and does not affect the level during the valid data period.	R/W	0
11	ILBE	Enable internal loop back 0: Internal loop back unable 1: Internal loop back enable, TXD and RXD shorted inside the module	R/W	0
10	IRE	Infrared modulation enable bit 0: Close infrared modulation output 1: Open infrared modulation output, low-carrier modulation with 38k output data	R/W	0
9:7	PARS	Select the parity bit 000: No parity	R/W	0

		001: Odd parity 010: Even parity 011: Fixed zero parity 100: Fixed one parity Other: User-defined parity		
6:5	DATLEN	Transmission bit data width 00:5-bit 01:6-bit 10:7-bit 11:8-bit	R/W	0
4	STOPS	Stop bit wide select 0:1-bit stop bit 1:2-bit stop bit	R/W	0
3	ERRIE	Error interrupt enable bit, the corresponding flag bit is the status indicator register bit5~bit2. 0: Disable interrupt 1: Enable interrupt	R/W	0
2	RXIE	Receive data interrupt enable bit, the corresponding flag bit is the status indicator register bit1. 0: Disable interrupt 1: Enable interrupt	R/W	0
1	TXIE	Transmit data interrupt enable bit, the corresponding flag bit is status indicator registers bit0. 0: Disable interrupt 1: Enable interrupt	R/W	0
0	EN	Module Enable 0: Disable 1: Enable	R/W	0

16.2.2 UART Baud Rate Configuration Register UARTx_BAUD（0x4）

Bit	Name	Description	R/W Sign	Reset Value
31:12	---	Reserved	R	0
11:0	CLKDIV	UARTx clock divide The formula of baud rate is: System Clock/[16*(CLKDIV+1)]	R/W	0

16.2.3 UART Status Indication Register UARTx_STA（0x8）

Bit	Name	Description	R/W Sign	Reset Value
31:8	---	Reserved	R	0
9	tx_fifo_full	Transmit FIFO is full: 0: Not full 1: Full	R	0
8	tx_fifo_empty	Transmit FIFO is empty:	R	1

		0: Not empty 1: Empty		
7	TB	Send state flag 0: Did not send 1: Sending data	R	0
6	RB	Receive status flag 0: Did not receive 1: Receiving data	R	0
5	DE	Data errors, write 1 cleared After the UART transmit FIFO is full, continue to write to the UART transmit register or write new transmit data during transmission. This bit will be set. 0: No error 1: Error	R/W	0
4	FE	Frame error, write one cleared The data received by the UART does not match the frame format flag. If the received stop bit is 0 instead of 1, the bit will be set. 0: No error 1: Error	R/W	0
3	OE	Overflow error, write one cleared The UART receive data register is not read in time and causes a receive overflow. This bit will be set. 0: No error 1: Error	R/W	0
2	PE	Parity error, write one cleared The data checksum error received by the UART, this bit will be set 0: No error 1: Error	R/W	0
1	TX	Send flag, write one cleared 0: Data not yet been sent or no data to be transmitted 1: Date has sent	R/W	0
0	RX	Receive flag, write one cleared 0: No receive data 1: Data has received	R/W	0

16.2.4 UART Transmit Data Register UARTx_TXD（0xC）

Bit	Name	Description	R/W Sign	Reset Value
31:9	---	Reserved	R	0
8	UP	User defined parity bit	R/W	0
7:0	TXDATA	Transmit data register	R/W	0

16.2.5 UART Receive Data Register UARTx_RXD（0x10）

Bit	Name	Description	R/W Sign	Reset Value
31:9	---	Reserved	R	0
8	UP	Parity bit	R	0
7:0	RXDATA	Receive data register	R	0

16.2.6 Baud Rate Fractional Divider Configuration Register UARTx_FDIV（0x14）

Bit	Name	Description	R/W Sign	Reset Value
31:14	---	Reserved	R	0
13:0	FDIV	Fractional division factor. The calculation formula is: $F = \left[\left(\frac{fi}{16 \times fo} - \left[\frac{fi}{16 \times fo}\right]\right) \times 2^{14} + 0.5\right]$ Where fi is the input clock (cpu current running clock), fo is the output clock, "[ ]" is the downward integer operator. For example, if the input clock is 1.8432MHz and the output clock is 9837Hz, then: $F = \left[\left(\frac{1843200}{16 \times 9837} - \left[\frac{1843200}{16 \times 9837}\right]\right) \times 2^{14} + 0.5\right]$ Find F=11647.	R/W	0

16.2.7 UART DMA Control Register UARTx_DMA_CTL（0x18）

Bit	Name	Description	R/W Sign	Reset Value
31:5	Reserved	Reserved	R	0
4	DMA_PARS	DMA Parity bit	R/W	0
3	RX_CYC_MODE	Receive circular mode enable	R/W	0
2	TX_CYC_MODE	Transmit circular mode enable	R/W	0
1	RX_DMA_EN	Receive DMA enable	R/W	0
0	TX_DMA_EN	Transmit DMA enable	R/W	0

16.2.8 UART DMA Transmit Starting Address Register UARTx_DMA_TBADR（0x1C）

Bit	Name	Description	R/W Sign	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_TBADR	DMA transmit starting address（Byte address） The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

16.2.9 UART DMA Receive Starting Address Register UARTx_DMA_RBADR（0x20）

Bit	Name	Description	R/W Sign	Reset

				Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RBADR	DMA receive starting address（Byte address） The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

16.2.10 UART DMA Transmit Length Register UARTx_DMA_TLEN（0x24）

Bit	Name	Description	R/W Sign	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_TLEN	DMA transmit length（Byte address）=（n）Byte The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

16.2.11 UART DMA Receive Length Register UARTx_DMA_RLEN（0x28）

Bit	Name	Description	R/W Sign	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RLEN	DMA receive length（Byte address）=（n）Byte The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

16.2.12 UART DMA Current Transmitting Address Register UARTx_DMA_TADR（0x2C）

Bit	Name	Description	R/W Sign	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_TADR	Current transmitting DMA address（Byte address）	RO	0

16.2.13 UART DMA Current Receiving Address Register UARTx_DMA_RADR（0x30）

Bit	Name	Description	R/W Sign	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RADR	Current receiving DMA address（Byte address）	RO	0

16.2.14 UART DMA Interrupt Enable Register（0x34）

Bit	Name	Description	R/W Sign	Reset Value
31:6	Reserved	Reserved	R	0
5	RX_ERR_IE	Received data overlay interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
4	TX_ERR_IE	Transmit data error interrupt enable 0: Disable interrupt	R/W	0

		1: Enable interrupt		
3	RX_FIE	DMA receive all full interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
2	RX_HIE	DMA receive half full interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
1	TX_FIE	DMA transmit all empty interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
0	TX_HIE	DMA transmit half empty interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0

16.2.15 UART DMA Interrupt Flag Register UARTx_DMA_IF（0x38）

Bit	Name	Description	R/W Sign	Reset Value
31:7	Reserved	Reserved	R	0
6	RX_ DONE	UART module proprietary, If a receive timeout occurs，This bit will be set. write one cleared	R/WC	0
5	RX_ERR	Received data overlay flag, write one cleared	R/WC	0
4	--	Reserved	R	0
3	RX_FDONE	DMA receive all full interrupt flag, write one cleared	R/WC	0
2	RX_HDONE	DMA receive half full interrupt flag, write one cleared	R/WC	0
1	TX_FDONE	DMA transmit all empty interrupt flag, write one cleared	R/WC	0
0	TX_HDONE	DMA transmit half empty interrupt flag, write one cleared	R/WC	0

16.2.16 UART DMA Receive Timeout Configuration Register UARTx_DMA_TO（0x3C）

Bit	Name	Description	R/W Sign	Reset Value
31:4	Reserved	Reserved	R	0
3:0	TIMEOUT_CNT	UART Receive Timeout Configuration, When UART does not receive the start bit for a certain period of time, DMA automatically ends. n=n UART data bit width time. Invalid configuration for 0	RW	0

16.3 UART Data Receiving and Sending Procedure

1、 Enable the corresponding UART clock in the 0 register MOD0_EN in the system control chapter module, enable module;。

2、 Configure the baud rate configuration register UART x_ BAUD. For example, when the system clock is 3.6864MHz and the communication baud rate is 9600, the baud rate configuration register can be set to:

UART0->BAUD = 3686400 / (9600*16)-1;

3、 Configure the communication control register UART x _CTL to select the data bit, stop bit, check mode and interrupt enable;

4、 Write 0x3f to clear the UART status indication register (UART x_ STA) status;

5、 Configure the UART interrupt enable, open the UART interrupt NVIC_ Enable IRQ (UART x_ IRQ n);

6、 Write an interrupt service routine, such as the UART0 interrupt service routine:

```
void UART0_HANDLER(void)
{
        u32    status;
        u8     temp;
        status = UART0->STA;

        /* UART error irq */
        if((UART0->CTRL & 0x8) && (status & 0x3c))
        {
            /* Start adding user code. Do not edit comment generated here */
        }
         /* receive data complete irq */
        if((UART0->CTRL & 0x4) && (status & 0x1))
        {
            /* Start adding user code. Do not edit comment generated here */
        }
        /* transmit data complete irq */
        if((UART0->CTRL & 0x2) && (status & 0x2))
        {
            /* Start adding user code. Do not edit comment generated here */
        }
}
```

The UART receive, transmit, and error interrupts are the same interrupt entry. The interrupt Enable bit and status flag opened by the control register should be used to determine which interrupt is active at this time;

7、 Process the received or sent data and complete it;

8、 Note: The UART port is full-duplex mode, which can transmit and receive at the same time. When RS485 half-duplex communication mode is used, when the RS485 chip is transmitting, there will be interference signal at the receiving end. In this case, it is recommended to turn off the receiving interrupt of the MCU when sending, and turn off the sending interrupt when receiving to eliminate interference.

17 ISO7816

SoC internal installed two ISO7816 channels, support for external two 7816 protocol interface device.

17.1 Overview

ISO7816 interface controller has the following features:

- ◎ Support standard ISO7816 protocol, working in master mode;
- ◎ Support card clock output, frequency can be set between 1 ~ 5MHz;
- ◎ Support 7816 various frequency division ratio setting;
- ◎ Support MSB first output logic low and logic high output LSB first data encoding;
- ◎ Support 1, 2 ETU width set the width of the error signal;
- ◎ Support 0~254 ETU width EGT configuration;
- ◎ Supports sending data transmission error retransmission mechanism, the number of retransmissions can be set between 0 to 7;
- ◎ 7816 card stack supports two interfaces (Esam and card): esam modules receive and transmit ports with a pin;
- ◎ Support card interface for receiving and sending separation;

17.2 Register Description

Table 15- 1 ISO7816 Register Base Address

Module Name	Physical Address	Address Mapping
ISO7816	0x40038000	0x40038000

Table 15- 2 ISO7816 Register Address Offset

Register Name	Address Offset	Description
ISO7816_CTRL0	0x0	Control Register 0
ISO7816_CTRL1	0x4	Control Register 1
ISO7816_CLK	0x8	Clock Configuration Register
ISO7816_BDDIV0	0xc	Baud Rate Configuration Register 0
ISO7816_BDDIV1	0x10	Baud Rate Configuration Register 1
ISO7816_STA0	0x14	Status Indication Register 0
ISO7816_STA1	0x18	Status Indication Register 1
ISO7816_DATA0	0x1c	Data Transmit Register 0
ISO7816_DATA1	0x20	Data Transmit Register 1

- Control register (0x0)

Table 15- 3 ISO7816 Control Register 0 ISO7816_CTL0

Bit	Name	Description	R/W Sign	Reset Value
31:28	---	Reserved	R	0
27	RX_GT0	Receive data GT select bit, when sending fixed 2etu 1: Receive data GT is 1etu 0: Receive data GT is 2etu	R/W	0
26	TX0_DMA_EN	Reserved	R/W	0
25	RX0_DMA_EN	Reserved	R/W	0
24:17	EGT0	EGT width selection value (0 to 255), that the extra guard time N, the default value N = 0.	R/W	0

		In the range of 0 to 254, N is used to calculate the delay between two consecutive data of a start edge: 12 etu + (Q × (N / f)). Formula, Q should take one of two values below: ——When T=15 does not exist in answer to reset, take F/D; ——When T=15 exit in answer to reset, take Fi/Di; N = 255 means that during transport protocol, a minimum of two consecutive characters start edge delay between the two directions of transmission are the same. The minimum delay value is: ——T=0,12etu ——T=1, 11etu		
16: 14	REP_CNT0	Automatic retransmission number control when data parity error occurs 000：0 time 001：1 time 010：2 times 011：3 times 100：4 times 101：5 times 110：6 times 111：7 times	R/W	011
13	RXPAR_ESEL0	Receive data parity error handling mode selection 1: Parity error, according to the T = 0 protocol post back error signal. Set RX_PAR_ERR flag, interrupt. 0: Parity error, do not send error signal, set RX_PAR_ERR flag, direct interrupt.	R/W	1
12:11	ERRWTH0	Error signal width select bit, it applies only to receive, and RXPAR_ESEL0 = 1 00:2 etu 01:1 etu 10:1.5 etu 11:2etu	R/W	01
10:8	PARSEL0	Parity bits select 000: No parity 001: Odd parity 010: Even parity 011: Fixed zero parity 100: Fixed one parity Other: Reserved	R/W	010
7	BGT_EN0	Data received BGT control bits transmitted 0: Close BGT function, data between transmission and reception don't insert BGT 1: Open BGT function, data between transmission and reception insert BGT (22etu)	R/W	0
6	ERR_IRQ_EN0	Transmission error interrupt enable bit, data collision when transmitting data, the data is received and the received data frame format overrun error	R/W	0

		0: Prohibit transmission error interrupt is generated 1: Enable transmission error interrupt is generated		
5	RX_IRQ_EN0	Data receive interrupt enable bit, enables data is shifted from the shift register to the receive buffer register to generate an interrupt 0: Prohibit data reception interrupt is generated 1: Enable data reception interrupt is generated	R/W	0
4	TX_IRQ_EN0	Data transmit interrupt enable bit to enable the completion of the data from the transmit shift register to generate an interrupt 0: Prohibit sending data to generate an interrupt 1: Enable data transmission interrupt is generated	R/W	0
3	RX_EN0	Receive data enable 0: Prohibit data reception 1: Enable data reception	R/W	0
2	TX_EN0	Enable sending data 0: Prohibit data transmission 1: Enable data transmission	R/W	0
1	DIRSEL0	Data coding mode selection bit 0: LSB first pass being logical data encoding 1: MSB first pass negative logic data encoding (data negated)	R/W	0
0	EN0	ISO7816 The controller enable bit 0: Controller close 1: Controller open	R/W	0

- ISO7816 control register 1 (0x04)

Table 15- 4 ISO7816 Control Register 1 ISO7816_CTL1

Bit	Name	Description	R/W Sign	Reset Value
31	CARD1_CHECK_EN	Card out Detect Flag, it is only active after the detection function of OLD is enable 1: Enable card out detection interrupt function 0: Disable card out detection interrupt function	R/W	0
30	OLD1_IRQ_EN	OLD detection interrupt function flag, it is only active after detection function of OLD is enable 1: Enable OLD detection interrupt function 0: Disable OLD detection interrupt function	R/W	0
29	OLD1_EN	OLD detection function flag 1: Enable OLD detection function 0: Disable OLD detection function	R/W	0
28	RX1_GT0	GT of received data choice bit, it is always 2etu when data is transmitted 1:GT of received data is 1etu 0:GT of received data is 2etu	R/W	0
27	TX1_DMA_EN	Reserved	R/W	0
26	RX1_DMA_EN	Reserved	R/W	0

25	IO1_EN	bidirectional data enable signal 1:78161_IO port is a bidirectional signal 0:78161_IO port is a one-way signal , output only, the data are input at 78161_I port	R/W	1
24:17	EGT1	EGT width selection (0~255), extra protection time N Default N=0. In the range of 0 to 254, N: before it was ready to receive the next character, the card need the delay(it sent by card or interface device) which start with onset of the first character: 12 etu +(Q×(N/f)) In the formula, Q should be one of two values: F/D, it is used to compute the value of etu. When T = 15 don't exist in the reset reply, Fi/Di, When T = 15 exist in the reset reply. N=255when the transmission protocol is effective, Minimize Delay between onset of two continuation character in either direction remains the same. Minimize Delay: When T=0,12etu When T=1,11etu	R/W	0
16: 14	REP_CNT1	Automatic retransmission number control when data parity error occurs 000:0time 001:1time 010:2times 011:3times 100:4times 101:5times 110:6times 111:7times	R/W	011
13	RXPAR_ESEL1	Receive data parity error handling mode selection 1: Parity check is wrong, According to T = 0 protocol, error signal will be post back, RX_PAR_ERR flag bit will be set and generate the interrupt. 0: Parity check is wrong, do not send error signal, RX_PAR_ERR flag bit will be set, generate the interrupt.	R/W	1
12:11	ERRWTH1	Width selection bit of the error signal 00:2etu 01:1etu 10:1.5etu 11:2etu	R/W	01
10:8	PARSEL1	Parity select bit 000: No parity 001: Odd 010: Even 011: Fixed to zero check 100: Fixed to one check	R/W	010

		Other: Reserved		
7	BGT_EN1	BGT control bit between data transmission and reception 0: Disable BGT function, do not insert the BGT between data reception and transmission 1: Enable BGT function, insert the BGT between data reception to transmission	R/W	0
6	ERR_IRQ_EN1	Transmit error interrupt flag, Data conflicts when data is transmitting, Data overflow when data is receiving and the received data frame is error 0: Disable the interrupt when data transmission is error 1: Enable the interrupt when data transmission is error	R/W	0
5	RX_IRQ_EN1	Receive interrupt flag, data transfer from shift registers to receive buffer registers 0: Disable data reception interrupt to generate 1: Enable data reception interrupt to generate	R/W	0
4	TX_IRQ_EN1	Transmit interrupt flag, set by hardware after completion of a serial transfer from shift registers 0: Disable the interrupt between data transmission 1: Enable the interrupt between data transmission	R/W	0
3	RX_EN1	Receive data enable 0: Disable receive data 1: Enable receive data	R/W	0
2	TX_EN1	Transmit data enable 0: Disable transmit data 1: Enable transmit data	R/W	0
1	DIRSEL1	Data coding mode selection bit 0: LSB first pass that is positive logic data coding method 1: MSB first pass negative logic data coding method (negate values)	R/W	0
0	EN1	ISO7816 Controller flag 0: Disable the controller 1: Enable the controller	R/W	0

- ISO7816_CLK（0x08）

Table 15- 5 ISO7816 Clock Control Register 1 ISO7816_CLK

Bit	Name	Description	R/W Sign	Reset Value
31:4	---	Reserved	R	0
3	CLKO_EN	Card clock output enable bit 0: Disable card clock output 1: Enable card clock output	R/W	0
2:0	CLKDIV	ISO7816 Division factor of clock output (CLK_O) ISO7816 source clock of module gain from fsyspll of system clock 000: No frequency division; 001:2 frequency division; 010:4 frequency division; 011:8 frequency division;	R/W	0

		100:16 frequency division 101:32 not support; 110: not support; 111:128 not support;		

- ISO7816 Baud Rate Factor 0 Register (0x0c)

Table 15- 6 ISO7816 Baud Rate Factor 0 Register ISO7816_BDDIV0

Bit	Name	Description	R/W Sign	Reset Value
31:22	---	Read-only, not writeable	R	0
21	FDS0_EN	Enable soft configuration coefficient of F/D 1: Baud rate coefficient will be determined by FDS0 which is written by software 0: Baud rate coefficient will be determined by FD0	R/W	0
20:8	FDS0	Baud rate coefficient which are configured by software, this bit can be written only when FDS0_EN is 1, In other cases, it is13'd372.	R/W	13'd372
7:0	FD0	8bit FI and DI is transmitted from answer to reset	R/W	8'h01

- ISO7816 Baud Rate Factor 1 Register (0x10)

Table 15- 7 ISO7816 Baud Rate Factor 1 Register ISO7816_BDDIV1

Bit	Name	Description	R/W Sign	Reset Value
31:22	---	Read-only, not writeable	R	0
21	FDS0_EN	Enable soft configuration coefficient of F/D 1: Baud rate coefficient will be determined by FDS0 which is written by software 0: Baud rate coefficient will be determined by FD0	R/W	0
20:8	FDS0	Baud rate coefficient which are configured by software, this bit can be written only when FDS0_EN is 1, In other cases, it is13'd372.	R/W	13'd372
7:0	FD0	8bit FI and DI is transmitted from answer to reset	R/W	8'h01

- ISO7816 status 0 register (0x14)

Table 15- 8 ISO7816 Status 0 Register ISO7816_ STA0

Bit	Name	Description	R/W Sign	Reset Value
31:12	---	Read-only, not writeable	R	0
11	FRAME_ERR0	Receive data frame format error interrupt flag this bit will be reset by writing '1' 1: Send the error frame format error of receiving data , it will generate the interrupt when transmission error interrupt is enable 0: Unsent the error frame format error of receiving data	R/W	0
10	BDDIV_R0	Baud rate matching instruction, the matching instructions between FI and DI, FD default is 8'h01, clock matching, it will be set as 1 when FD unmatched. 1: matched 0: unmatched	R	1
9	TX_FLAG0	Transmit data buffer empty flag. The automatic set after power-on reset, and it shows Buffer is empty and can be written. The flag will be	R	1

		automatically cleared after MCU is written. After shift data from transmit buffer registers to shift registers, this bit will be set as 1 1: Data transmit buffer is empty 0: The data transmit buffer has data to be transmitted		
8	RX_FLAG0	Data buffer full flag,7816 Interface controller receives every bit data, hardware automatic clear settings, it shows Interface controller receives 1 bit data, Reading data receive buffer register will be reset. 1: 1byte data is received, data buffer is full 0: There is no data received, data buffer is empty	R	0
7	RXBUSY0	Reception data busy flag. Set by hardware, reset by software Hardware automatic clear settings 0: Receive data idle 1: RSR are receiving data, it will be set as 1 after start bit is received, it will automatic clear zero after stop bit is received	R	0
6	TXBUSY0	Transmit data busy flag. Set by hardware, reset by software Hardware automatic clear settings 0: Transmit data idle 1: TXSHF are sending data, it will be set as 1 after start bit is send, it will automatic clear zero after stop bit is send	R	0
5	TXPAR_ERRIF0	Send data parity error flag, there is still parity error after retry, then this bit is turned on. this bit will be reset by writing '1' 1: Parity error occurred when data is transmitted. 0: Parity error didn’t occur when data is transmitted.	R/W	0
4	RXPAR_ERRIF0	Receive data parity error flag bit, there is still parity error after retry, then this bit is turned on. this bit will be reset by writing '1' 1: Parity error occurred when receiving data is received 0: Parity error didn’t occur when data is received	R/W	0
3	COL_IF0	Send data conflict error interrupt flag. Set by hardware, reset by software, this bit will be reset by writing '1' 0: No interrupt 1: Interrupt occurs	R/W	0
2	OVL_IF0	Receive data overflow flags. Set by hardware, reset by software this bit will be reset by writing '1' 0: No overflow 1: Interrupt occurs, the receive buffer register didn’t be read, and received the new data. Overflow flag bit is enable	R/W	0
1	RXIF0	Transmit data interrupt flag bit. After shift data from shift registers to transmit buffer registers, it will be set as 1. Set by hardware, reset by software this bit will be reset by writing '1' 0: No interrupt 1: Interrupt occurs	R/W	0

0	TXIF0	Transmit data interrupt flag. After move data from send buffer registers to shift registers, it will be set as 1, set by hardware, reset by software, this bit will be reset by writing '1' 0: No interrupts 1: Interrupt occurs	R/W	0

- ISO7816 status 1 register (0x18)

Table 15- 9 ISO7816 Status 1 Register ISO7816_ STA1

Bit	Name	Description	R/W Sign	Reset Value
31:14	---	Read-only, not writeable	R	0
13	CARD_OUT_FLAG	This bit is Effective, after CARD_CHECK_EN enabled. this bit will be reset by writing '1'. 1:Detected card was uprooted (the width of high level pulse of input port is more than 40mS) 0: Pulling out the card is not detected (the width of high level pulse of input port is not more than 40mS)	R	0
12	OLD_FLAG	After OLD_EN enabled, this bit is Effective, to match the received RA9105 signal of OLD interrupt flag bit, this bit will be reset by writing '1'. 1:OLD signal has been received. 0:OLD signal hasn't been received.	R/W	0
11	FRAME_ERR0	Receive data overflow flag, this bit will be reset by writing '1' 1: Send received data frame format error, Interrupt occurs when the transmit error interrupt is enabled 0: Unsent received data frame format error	R/W	0
10	BDDIV_R1	Baud rate matching direction, FI and DI matching direction; FD defaults to 8'h01, clock matching, it will be set as 1 when FD unmatched. 1: matched 0: unmatched	R	1
9	TX_FLAG1	Send Buffer empty flag. It automatic setting after power-on reset, And it shows Buffer is empty, and it can be written. The flag will be automatically clean after MCU is written, After move data from send buffer registers to shift registers, this bit will be set as 1 1: Buffer is empty 0: There is data which are ready to send in the buffer	R	1
8	RX_FLAG1	The data reception complete flag,7816 Interface receives every bit data, receiver channel generate the interrupt. Set by hardware, reading data receiving buffer register clean. Interface controller receives every bit data, Hardware automatic Clear Settings, it shows Interface controller receives 1 bit data, Read data receiving buffer register will be reset. 1:1byte data is received, receive data buffer is full 0: There is no data received, receive data buffer is empty	R	0

7	RXBUSY1	Receive data busy flag. Hardware set, reset by software Hardware automatic clear settings 0: Data reception go idle 1: RSR are receiving data, it will be set as 1 after start bit is received, it will automatic clear zero after stop bit is received	R	0
6	TXBUSY1	Transmit data busy flag. Hardware set, reset by software Hardware automatic Clear Settings 0: Data transmission go idle 1: TXSHF are sending data, it will be set as 1 after start bit is transmitted, it will automatic clear zero after stop bit is transmitted	R	0
5	TXPAR_ERRIF1	Transmit data parity error flag bit. Hardware set, reset by software this bit will be reset by writing '1' 1: Parity error occurred data is transmitted 0: Parity error didn't occur data is transmitted	R	0
4	RXPAR_ERRIF1	Receive data parity error flag bit. Hardware set, reset by software this bit will be reset by writing '1'. 1: Parity error occurred data is received 0: Parity error didn't occur data received	R/W	0
3	COL_IF1	Send data conflict error interrupt flag bit. set by hardware, reset by software this bit will be reset by writing '1' 0: No interrupts 1: Interrupt occurs	R/W	0
2	OVL_IF1	Receive data overflow flag bit. Set by hardware, reset by software this bit will be reset by writing '1' 0: There is no overflow 1: Interrupt occurs, the receive buffer register don't be read, and received the new data. Overflow flag bit is Enable	R/W	0
1	RXIF1	Receive data interrupts flags bit. After move data from shift registers to send buffer registers, it will be set as 1, set by hardware, reset by software this bit will be reset by writing '1' 0: No interrupts 1: Interrupt occurs	R/W	0
0	TXIF1	Sending data interrupts flag bit. After move data from send buffer registers to shift registers, it will be set as 1.Set by hardware, reset by software this bit will be reset by writing '1' 0: No interrupts 1: Interrupt occurs	R/W	0

- ISO7816 Data 0 Register (0x1C)

Table 15- 10 ISO7816 Data 0 Register ISO7816_ DATA0

Bit	Name	Description	R/W Sign	Reset Value

Reserved	--	Read-only, not writeable	R	0
8	DATA0[8]	It is PARITY bit of data frames,when parsel is in User-defined mode	R/W	0
7:0	DAT0	Data Register0	R/W	0

- ISO7816 data 1 register (0x20)

Table 15- 11 ISO7816 Data 1 Register ISO7816_ DATA1

Bit	Name	Description	R/W Sign	Reset Value
Reserved	--	Read-only, not writeable	R	0
8	DATA1[8]	It is PARITY bit of data frames,when parsel is in User-defined mode	R/W	0
7:0	DAT1	Data Register1	R/W	0

17.3 7816 And ESAM Communication Steps

1、The 7816 communicates with the ESAM. There is no need to consider the isolation problem. The data IO can share one line. It is recommended to use the 7816 module 0.

2、Configure the system control chapter module to enable the 0 register MOD0_EN, set the 13th position to 1, and turn on the 7816clock.

3、The 7816control register is configured as ISO7816_CTL0. Using the national network ESAM, the register can be configured as 0x00000201.

4、Clear the ISO7816 status register ISO7816_STAT0.

5、 Turn on the 7816bus clock. For example, when the system clock is 3.6864MHZ, ISO7816 -> CLK=0x09; at this time, the 7816module clock is 1.8432MHZ.

6、 Data can be read and written to the 7816 bus by interrupt mode or query status mode.

17.4 7816 And Card Communication Steps

1、For the card table, the card needs to be isolated from the main power, and the 1-5MHZ clock is required to work normally. Most of the existing SOC uses a high-speed optical scheme to isolate the main power from the card. This solution has high cost and use high-speed optocouplers are used to isolate high-frequency clocks, which are less reliable at high and low temperatures. We provide a dedicated chip RN8501 for connection to the card, which uses two common optocouplers for data communication with the MCU.

2、Configure the system control chapter module to enable the 0 register MOD0_EN, set the 13th position to 1, and turn on the 7816clock.

3、The 7816control register is configured as ISO7816_CTL1. Because it is isolated from the card, it is separated from the transmission. ISO7816->CTRL1 can be configured as 0x60000201.

4、Clear the ISO7816 status register ISO7816_STAT0.

5、 Turn on the 7816bus clock. For example, when the system clock is 3.6864MHZ, ISO7816 -> CLK=0x09; at this time, the 7816module clock is 1.8432MHZ.

6、Can read and write data to the 7816 bus through interrupt mode or query status mode.

After using RN8501, the insertion and extraction detection of the card and the reset information reading of the card will be different from the separation scheme:

1、 Card insertion detection: Connect the detection pin of the card holder to the CHK of the RN8501. When the card is inserted into the card holder, the CHK pin is low level, and the RN8501 sends a low level signal of about 9MS

through the 7816 port connected to the RN821x. When the OLD detection enable of ISO7816_CTL1 is turned on, an interrupt is generated and it is considered that there is a card inserted outside.

2、 Card pull-out detection: After the card of ISO7816_CTL1 is configured to pull out the detection enable position, the pullout of the card can be detected. Note: After the card operation is completed, the card pull-out detection interrupt can be opened.

3、The reset information of the card is read after the RN821x and RN8501 communication handshake is completed.

4、More specific steps can be found in the RN8501 data sheet.

18 IIC Interface

The SoC has a built-in I² C interface controller.

18.1 Overview

The controller of I²C Interface has the following features:

- ◎ Master and slave mode are supported;
- ◎ Support for 7-bit addresses;
- ◎ Support Many frequency division ratio settings
- ◎ Supports 100kbps and fast mode 400kbps;

18.2 Register Descriptions

Table 16- 1 I²C Register Base Address

Module Name	Physical Address	Mapping Address
I²C	0x40024000	0x40024000

Table 16- 2 I²C Register Offset Address

Register	Address Offset	Descriptions
I²C_CTRL	0x0	Control Register
I²C_CLK	0x4	Clock Configuration Register
I²C_STA	0x8	Status Indication Register
I²C_ADDR	0xC	Slave Device Address Register
I²C_DATA	0x10	Transmit And Receive Data Register

- Control register (0x0)

Table 16- 3 Control Register I²C_CTL

Bit	Name	Description	R/W Sign	Reset Value
31:6	---	Read-only, not writeable	R	0
5	MODE	MASTER/SLAVE 1: MASTER 0: SLAVE	R/W	0
4	ACK	ACK sending enable 1: After received the signal of the ninth SCL, generate ACK 0: After received the signal of the ninth SCL, don't generate ACK	R/W	0
3	IRQE	I²C interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
2:1	BUSCON	A bus control bit, start command is effective when bus is idle or host is posted. Start command is effective when host is posted When timing of the stop or start is detected, command bit will be clear	R/W	0

		00:no action 01: Producing the time for START 10: Producing the time for STOP 11: Reserved		
0	EN	Module Enable 1: Enable I²C 0: Disable I²C	R/W	0

- Clock Configuration Register (0x4)

Table 16- 4 Clock Configuration Register I² C_ CLK

Bit	Name	Description	R/W Sign	Reset Value
31:3	---	Read-only, not writeable	R	0
2:0	CLKDIV	I²C clock separate frequency parameters selection bit: I²C calculating formula for communication clock rate: SCL=APBCLK/m, there into m produced by CLKDIV, shown in the table below. It generated High-speed mode or Normal-mode communication clock according to different System frequency and Separate frequency parameters. If configuration option is not in the table below, it defaults to divide-by-ten.	R/W	001

System frequency	Separate frequency parameters /CLKDIV(m)	
	High-speed mode	Normal-mode
1.8432Mhz	Not support	010（20）
3.6864Mhz	001（10）	011（38）
7.3728Mhz	010（20）	100（76）
14.7456Mhz	011（38）	101（152）
29.4912Mhz	100（76）	110（304）

- Status indication register (0x8)

Table 16- 5 Status Indication Register I² C_ STAT

Bit	Name	Description	R/W Sign	Reset Value
31:9	---	Read-only, not writeable	R	0
8	DIR	Direction of Reading or writing flag 1: Write. 0: Read.	R	0
7	MATCH	Address matching, when timing of the stop or start is detected, command bit will be clear 0: Address mismatch 1: Address matching	R	0
6	BUSY	Traffic Status flag	R	0

		0: IIC is idle 1: IIC is busy		
5	COL	Sending conflict interrupt. this bit will be reset by writing '1' Sending data register is not empty or When receiving data, user write new data to data register. Trigger sending interrupt flag 0: No trigger send conflict interrupt 1: Trigger send conflict interrupt	R/W	0
4	OVERF	Receive overflow interrupt flag. this bit will be reset by writing '1' When receiving data, a new data is received before previous data don't be took away, Trigger overflow interrupt flag 0: No trigger overflow interrupt 1: Trigger overflow interrupt	R/W	0
3	TXEMPT	Sending data register is empty error flag. this bit will be reset by writing '1' In slave mode, the host asked slave to send data, when send buffer is empty, trigger send data is empty error interrupt flag 0: No trigger send data is empty error interrupt 1: Trigger send data is empty error interrupt	R/W	0
2	TRANC	Transfer complete interrupt flag. this bit will be reset by writing '1' When sending data, send buffer is empty , or when receiving data , receive buffer is full. Trigger transfer complete interrupt flag 0: Transfer has not been completed 1: Transfer has been completed	R/W	0
1	RX_NACK	Received NACK interrupt flag. this bit will be reset by writing '1' 1: Received NACK 0: No NACK was received	R/W	0
0	STPD	STOP time sequence inspection interrupt flag. this bit will be reset by writing '1' When timing of the start is detected or module is power off, this bit will be clear 0: No STOP timing detected 1: Detect STOP timing	R/W	0

- Slave device address register (0xC)

Table 16- 6 Slave Device Address Register I²C_ADDR

Bit	Name	Description	R/W Sign	Reset Value

31:8	---	Read-only, not writeable	R	0
7:1	SADR	Device address, it can't be written during the transport address. In host mode, it is slave device address; In slave mode, this address is used to compare with address which host send.	R/W	0
0	RW	Direction of Reading or writing of host flag 0: write 1: read	R/W	0

- Transmit And Receive Data Register（0x10）

Table 16- 7 Transmit And Receive Data Register I^2C_ DATA

Bit	Name	Description	R/W Sign	Reset Value
31:8	---	Read-only, not writeable	R	0
7:0	TRDAT	Send/receive data	R/W	0

19 SPI Interface (modified)

The chip integrates 4 SPI M/S interfaces with ordinary DMA, supports SPI full-duplex mode, is used to communicate with external SPI interface devices, can be programmed to achieve master mode and slave mode work.

19.1 Overview

The controller of SPI Interface has the following features:

- ◎ Supports SPI full duplex mode;
- ◎ Supports both master and slave mode operation;
- ◎ Supports clock polarity and phase setting;
- ◎ Supports separate double buffers for transmit and receive;
- ◎ Supports LSB and MSB transmission modes 8-bit, 16-bit, 32-bit configurable;
- ◎ Supports 256 baud rates programmable up to 14.7456MHz (fcpu=29.4912MHz);
- ◎ Slave low-speed and high-speed modes can be configured, low-speed mode slaves support up to fcpu/8; high-speed mode supports fcpu/4.
- ◎ Supports data transfer completion interruptions;
- ◎ Support for data transmission conflict interruption;
- ◎ Support for SCSN mode error interrupts;
- ◎ Supports DMA function

19.2 I/O pin multiplexer and mapping

SPI0：P44~P47、P110~P113；

SPI1：P52~P55、P20~P23、P40~P43；

SPI2：P110~P113、P40~P43；

SPI3：P110~P113、P14~P17、P20~P23、P47&P46&P84&P83

The same SPI can not be multiplexed to different IOs at the same time, otherwise the data will be disordered, and the design should be careful to avoid it.

19.3 Functional Description

The SPI interface conforms to the standard SPI HOST protocol, and the SPI clock operating mode is set by the CPOL (Clock Polarity) and CPHA (Clock Phase) parameters: CPOL determines whether the leading edge of the clock is a rising or falling edge, and CPHA determines whether the leading edge of the clock is a data sample or a data establishment.

The detailed operating modes are listed in the table below:

Table 17- 1 SPI clock operating mode

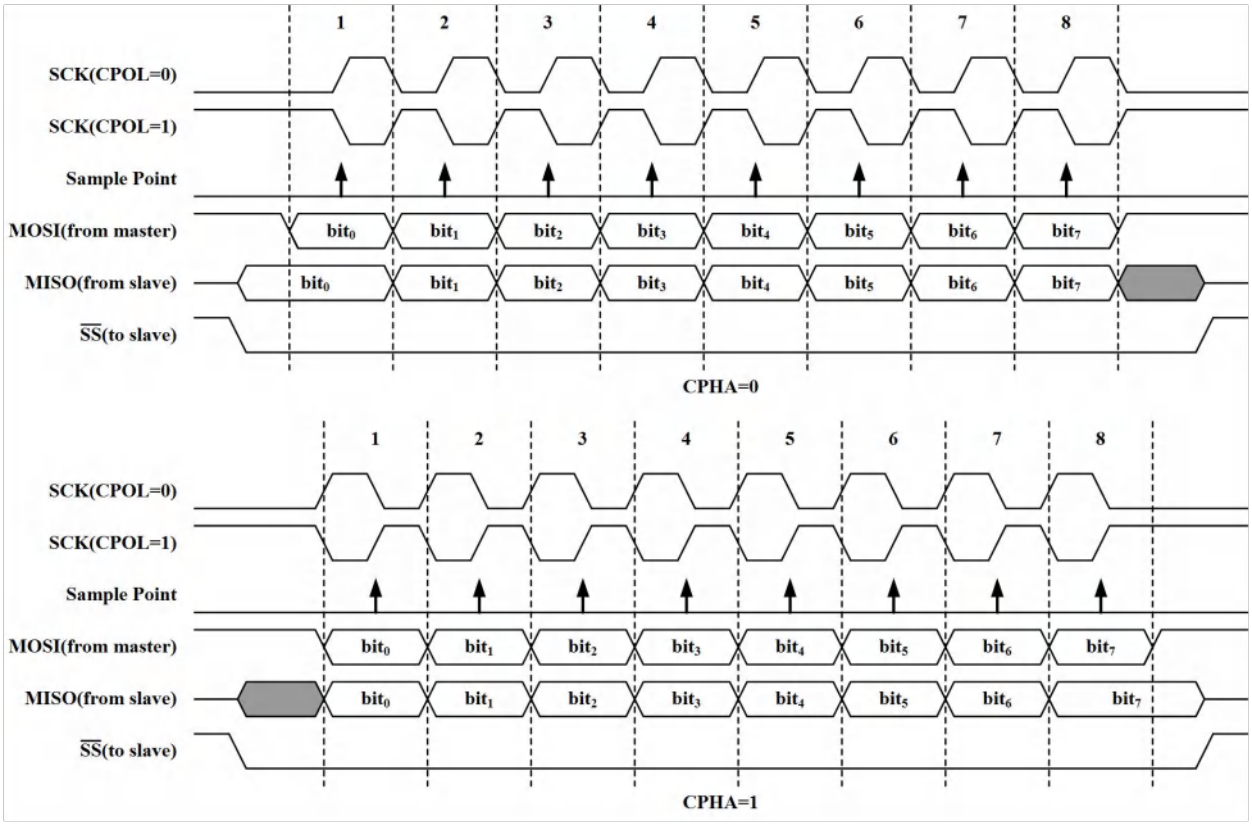
SPI MODE	CPOL/CPHA	Front edge	Back edge
0	**0/0**	rising edge, data sampling	falling edge, data build
1	**0/1**	rising edge, data build	falling edge, data sampling
2	**1/0**	falling edge, data sampling	rising edge, data build
3	**1/1**	falling edge, data build	rising edge, data sampling

The data transfer size supports 8/16/32bit width. The SPI clock source comes from the system clock, which generates the communication clock after a dividing factor.

Four types of interrupts are supported, including data transmission conflict interrupt, data reception overflow interrupt, end of transmission interrupt, and SS mode error interrupt.

Send data conflict, when a data send is in progress (txbusy is 1), at this time there is another write command on the bus, then TXCOLIF is set to 1. If COL_IRQ_EN=1, an interrupt will be generated, and at the same time this send command will not be responded to, and the data that is being sent will be transferred to completion normally.

Figure 14-2 SPI clock operating mode



Receive Data Overflow: If the RXDATA register is not read before the next complete receive data enters the shift register, receive data overflow will be generated, then RXCOLIF will be set to 1. If COL_IRQ_EN=1, an interrupt will be generated, and at the same time, the new receive data will be saved into the receive data register, and the data that has not been read away originally will be overwritten.

End Of transmission interrupt: when the transmission ends (sck_end), if TR_IRQ_EN=1, an interrupt will be generated and TRIF will be set to 1 at the same time.

SCSN mode error interrupt: In the slave mode, SCSN must be input, When data is transmitted, SCSN become high, SCSN mode error flag will be set as 1;In the host mode, only enable the host model SCSN error detection(SCSN_EN=1),meanwhile SCSN is low, SCSN mode error flag will be set as 1. When SCSN mode error flag is 1, transmission is terminated, SPI module is reset, if ERR_IRQ_EN=1, interrupt occurs.

Note: After the control register is configured, when it is in the host mode, the SPI read/write operation will be started only when data is written to the data transmission register.

19.4 Register Description

Table 17- 2 SPI Register Base Addresses

Module name	Physical address	Mapping address
SPI0	0x40020000	0x40020000
SPI1	0x40050000	0x40050000
SPI2	0x40054000	0x40054000
SPI3	0x40058000	0x40058000

Table 17- 3 SPIx Register Offset Addresses

Register name (x means "0~3")	Address Offset	Description
SPIx_CTRL	0x0	Control Register
SPIx_STAT	0x4	Status Register
SPIx_TXDATA	0x8	Transmit Data Register
SPIx_RXDATA	0xC	Receive Data Register
SPIx_TXDFLT	0X10	Default send data configuration when SPI send data is empty
SPIx_DMA_CTRL	0x14	SPIX DMA Control Register
SPIx_DMA_TBADR	0x18	SPIX DMA Transmit Starting Address Register
SPIx_DMA_RBADR	0x1c	SPIX DMA Receive Starting Address Register
SPIx_DMA_TLEN	0x20	SPIX DMA Transmit Length Register
SPIx_DMA_RLEN	0x24	SPIX DMA Receive Length Register
SPIx_DMA_TADR	0x28	SPIX Current Transmitting DMA Address Register
SPIx_DMA_RADR	0x2c	SPIX Current Receiving DMA Address Register
SPIx_DMA_IE	0x30	SPIX DMA Interrupt Enable Register
SPIx_DMA_FLG	0x34	SPIX DMA Interrupt Flag Register

19.4.1 SPI Control Register SPIx_CTRL（0x0）

Bit	Name	Description	R/W	Reset Value
31:27	---	Read-only, not writeable	R	0
26	SLV_TX_ADV	SPI Slave High Speed Mode Enable Bit = 0, SPI slave low-speed mode, fcpu/8, backward compatible =1, SPI slave high speed mode, slave rate up to fcpu/4. Note: Slave high speed mode, without considering path delay, the slave rate can reach fcpu/2.	R/W	0
25	SCSN_POS_IRQEN	SCSN_POS interrupt enable 0: Disable interrupt 1: Enable interrupt	RW	0
24	SCSN_NEG_IRQEN	SCSN_NEG interrupt enable 0: Disable interrupt 1: Enable interrupt	RW	0
23	TXEMPT_IRQEN	TXEMPT interrupt enable 0: Disable interrupt 1: Enable interrupt	RW	0

22	TX_DFLT_EN	Whether to send SPI_TXDFLT register data when sending BUF null. 0: Send the value of the last transmission of SPI_TXDATA 1: Send SPI_TXDFLT register value	RW	0
21	TX_DMA_EN	Send DMA request 1: Enable DMA request 0: Disable DMA request	R/W	0
20	RX_DMA_EN	Receive DMA request 1: Enable DMA request 0: Disable DMA request	R/W	0
19:12	CLKDIV	SCK clock division factor SCK frequency = system clock frequency/(2*(CLKDIV + 1))	R/W	0
11:10	WIDTH	Data width selection 0：8bit 1：16bit 2：32bit 3：Reserved, 8bit	R/W	0
9	SCSN_EN	SCSN model error detection enable, Works only in the master mode 0： Disable SCSN model error detection in the master mode, SCSN is a general purpose IO 1： Enable SCSN model error detection in the master mode, SCSN as the input of SPI	R/W	0
8	CPHA	Clock phase selection 0: Front edge sampling data 1: Front edge build data	R/W	0
7	CPOL	Clock polarity selection 0: "SCK" is set low in the idle state. 1: "SCK" is set high in the idle state.	R/W	0
6	LMSB	LSB/MSB selection 0: MSB transmits first 1: LSB transmits first	R/W	0
5	TXCOL_IRQ_EN	Data conflict interrupt enable 0: Disable write conflict interrupt 1: Enable write conflict interrupt	R/W	0
4	RXCOL_IRQ_EN	Data conflict interrupt enable 0: Disable read conflict interrupt 1: Enable read conflict interrupt	R/W	0
3	ERR_IRQ_EN	SCSN mode error interrupt enable 0: Disable mode error interrupt 1: Enable mode error interrupt	R/W	0
2	TR_IRQ_EN	Data transmission interrupt enable	R/W	0

		0: Disable transmit data interrupt 1: Enable transmit data interrupt		
1	MAST/SLAV	MASTER/SLAVE 1: MASTER 0: SLAVE	R/W	1
0	EN	Enable 0: Disable SPI Interface 1: Enable SPI Interface	R/W	0

19.4.2 SPI Status Register SPIx_ STAT（0x4）

Bit	Name	Description	R/W	Reset Value
31:8	---	Read-only, not writeable	R	0
7	SCSN_POS	Flags for CSN pull-up events when acting as a slave 0: No CSN pull-up event occurred 1: A CSN pull-up event occurred	R/W	0
6	SCSN_NEG	Flags for CSN pull-down events when acting as a slave 0: No CSN pull-down event occurred 1: A CSN pull-down event occurred	R/W	0
5	TXEMPT	Send data null conflict flag bit. When BUF is empty, a write data null conflict occurs when the SPI bus needs to send data 0：No data sent null conflict interrupt 1：Generate sent data null conflict interrupt	R/W	0
4	TXBUSY	Sending data busy state flag. 0: Sending data is idle, bus can write command of SPITX register 1: Data is sending, bus can’ t write command of SPITX register	R	0
3	TXCOLIF	Write conflict flag. this bit will be reset by writing '1' When data is sending (TXBUSY is 1), user write new sending data to SPI, then new sending data will be lost and Write conflict flag will be set as 1. 0: No write data conflict interrupt 1: Generate the interrupt of write data conflict	R/W	0
2	RXCOLIF	Receiving data overflow flag. this bit will be reset by writing '1'. When receiving data in a row, if user don’t read RXDATA register, generate the receiving data overflow 0: No receiving data overflow interrupt 1: Generatethe receiving data overflow interrupt	R/W	0
1	ERRIF	SCSN mode conflict interrupt flag bit: when SPI is in host mode, only when SCSN_EN is 1, meanwhile“SCSN”is low, this bit will be set as 1; when SPI is in slave mode, “SCSN” as slave input, When the data was transmitted, if “SCSN” is high,	R/W	0

		this bit will be set as 1; if ERR_IRQ_EN=1,interrupt occurs, if generate the mode conflict, SPI module will be reset. this bit will be reset by writing '1' 0: No mode conflict interrupt 1: Generatethe mode conflict interrupt		
0	TRIF	Sending data interrupt flag bit, When the data transfer is finished, this bit will be set as 1, if TR_IRQ_EN=1,interrupt occurs, this bit will be reset by writing '1' 0: No sending data interrupt 1: Generatethe sending data interrupt, send data register is empty.	R/W	0

19.4.3 SPI Transmit Data Register SPIx_ TXDATA（0x8）

Bit	Name	Description	R/W	Reset Value
31:0	TXDATA	Transmit data register	R/W	0

19.4.4 SPI Receive Data Register SPIx_RXDATA（0xC）

Bit	Name	Description	R/W	Reset Value
31:0	RXDATA	Receive data register	R	0

19.4.5 SPI Default Transmit Data Register SPIx_TXDFLT（0x10）

Bit	Name	Description	R/W	Reset Value
31:0	TXDFLT	Default transmit data register	R	0

19.4.6 SPI DMA Control Register SPIx_DMA_CTRL（0x14）

Bit	Name	Description	R/W	Reset Value
31:4	Reserved	Reserved	R	0
3	RX_CYC_MODE	Receive circular mode enable	R/W	0
2	TX_CYC_MODE	Transmit circular mode enable	R/W	0
1	RX_DMA_EN	Receive DMA enable	R/W	0
0	TX_DMA_EN	Transmit DMA enable	R/W	0

19.4.7 SPI DMA Transmit Starting Address Register SPIx_DMA_TBADR（0x18）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0

16:0	DMA_TBADR	DMA transmit starting address（Byte address） The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

19.4.8 SPI DMA Receive Starting Address Register SPIx_DMA_RBADR（0x1C）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RBADR	DMA receive starting address（Byte address） The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

19.4.9 SPI DMA Transmit Length Register SPIx_DMA_TLEN（0x20）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_TLEN	DMA transmit length（Byte address）=（n）Byte The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

19.4.10 SPI DMA Receive Length Register SPIx_DMA_RLEN（0x24）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RLEN	DMA receive length（Byte address）=（n）Byte The lowest two bits must be configured according to the specific interface data bit width configuration	R/W	0

19.4.11 SPI DMA Current Transmitting Address Register SPI_DMA_TADR（0x28）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_TADR	Current transmitting DMA address（Byte address）	RO	0

19.4.12 SPI DMA Current Receiving Address Register SPIx_DMA_RADR（0x2C）

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	R	0
16:0	DMA_RADR	Current receiving DMA address（Byte address）	RO	0

19.4.13 SPI DMA Interrupt Enable Register SPIx_DMA_IE（0x30）

Bit	Name	Description	R/W	Reset Value

31:6	Reserved	Reserved	R	0
5	RX_ERR_IE	Received data overlay interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
4	TX_ERR_IE	Transmit data error interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
3	RX_FIE	DMA receive all full interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
2	RX_HIE	DMA receive half full interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
1	TX_FIE	DMA transmit all empty interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0
0	TX_HIE	DMA transmit half empty interrupt enable 0: Disable interrupt 1: Enable interrupt	R/W	0

19.4.14 SPI DMA Interrupt Flag Register SPIx_DMA_IF（0x34）

Bit	Name	Description	R/W	Reset Value
31:6	Reserved	Reserved	R	0
5	RX_ERR	Received data overlay flag, write one cleared	R/WC	0
4	--	Reserved	R	0
3	RX_FDONE	DMA receive all full interrupt flag, write one cleared	R/WC	0
2	RX_HDONE	DMA receive half full interrupt flag, write one cleared	R/WC	0
1	TX_FDONE	DMA transmit all full interrupt flag, write one cleared	R/WC	0
0	TX_HDONE	DMA transmit half full interrupt flag, write one cleared	R/WC	0

19.5 Application Methods

1、In the System Control section, enable the SPI clock.

2、As a master:

1) Configure the corresponding GPIO multiplexing as SPI0/1 pins. Note: For master mode application, the SCSN pin is configured as an IO port and software is used to generate the SCSN level;

2）Enable SPI interrupt;

3) Initialize SPI0/1, configure TXDFLT, CTRL and other registers, and select SPI MAST mode by setting MAST/SLAV bit 1 of SPI_CTL. The frequency of data transfer is configured by CLKDIV of SPI_CTL, set the SPI_CTL data transfer interrupt enable bit TR_IRQ_EN to 1;

4) Prepare the data to be sent, pull SCSN low, write the first data to be sent to SPI_TXDATA, and start

sending data;

5) If SPI interrupt occurs, enter IRQ processing function, if query SPI_STA.TRIF is 1, it indicates that transmission of one bit width (configured by SPI_CTL.WIDTH) data is completed, read SPI_RXDATA register to receive data and fill in the next data to be sent to SPI_TXDATA;

6) Repeat 5) until all data to be sent has been sent, pull up the SCSN;

3、As a slave

1) Configure the corresponding GPIO multiplexing as SPI0/1 pins. Note: The SCSN pin should be configured for SCSN function when applied in slave mode;

2）Enable SPI interrupt;

3) Initialize SPI0/1, configure TXDFLT and CTRL registers, set MAST/SLAV position 0 of SPI_CTL, i.e., SPI SLAVE mode is selected, the frequency of data transmission is decided by the host computer, set TR_IRQ_EN, SCSN_NEG AND SCSN_POS of SPI_CTL register to 1, and prepare the data to be sent;

4) If SPI interrupt occurs, enter IRQ processing function, if query SPIS_STIF.SCSN_NEG_IF IS 1, IT MEANS THE HOST INITIATES SPI COMMUNICATION, THE SLAVE RECEIVES SPI_RXDATA ON SDI AND PARSES IT, AND WRITES THE DATA TO BE SENT TO SPI_TXDATA; if query SPI_STA.TRIF is 1 it indicates that the transmission of once bit width (configured by SPI_CTL.WIDTH) data is completed, take out the SPI_RXDATA register to receive data and fill in the next data to be sent to SPI_TXDATA; if query to SPI_STA.SCSN_POS_IF is 1 indicates that this frame data transmission is completed, take out the SPI_RXDATA register to receive data.

20 LPUART (New)

20.1 Overview

The LPUART module is a low-power general-purpose serial port capable of full-duplex UART communication with limited power consumption. The operating clock only needs to be configured to 32.768 kHz to achieve 9600 baud rate communication. LPUART can work in low frequency mode to realize low power consumption asynchronous data sending and receiving. When the CPU is in SLEEP mode and a wake-up event is detected, the LPUART can generate a wake-up interrupt to quickly wake up the CPU.

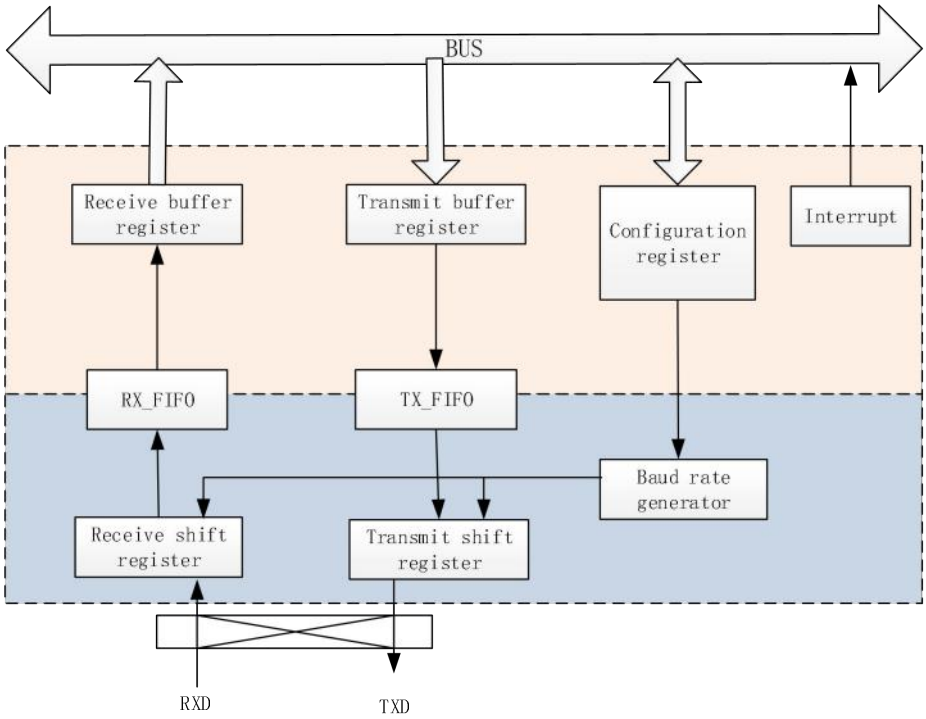
The LPUART protocol consists of two data lines, LPUART_TX and LPUART_RX, where LPUART_TX is the transmit data line and LPUART_RX is the receive data line. The function of this module consists of 3 main parts: configuring the data frame format for serial data transmission; detecting the start bit for data reception; and waking up from low-power mode.

20.2 Specificities

- Maximum 9600 baud rate at 32.768k operating clock, baud rate range 300~9600bps
- Transmit/Receive buffer supports separate 4-byte FIFO.
- Supports data bit widths of 5/6/7/8bit and stop bits of 1bit or 2bit.
- Parity bit Support parity, even parity, all 0/1, no parity bit or user-defined parity bit
- Supports four low-power wake-up modes: RX falling edge wake-up, start bit detection wake-up, (single or multi-frame) data reception completion wake-up, and one-frame data matching wake-up.
- Separate transmit and receive interrupt enables
- Supports 38kHz IR modulation output
- Receive support for idle frame detection

20.3 Functional block diagram

The operating clock of LPUART is 32.768 KHz, and the clock source can be selected from internal low-frequency clock RCL32k and external low-frequency crystal LOSC.The LPUART register read/write clock is the system clock.

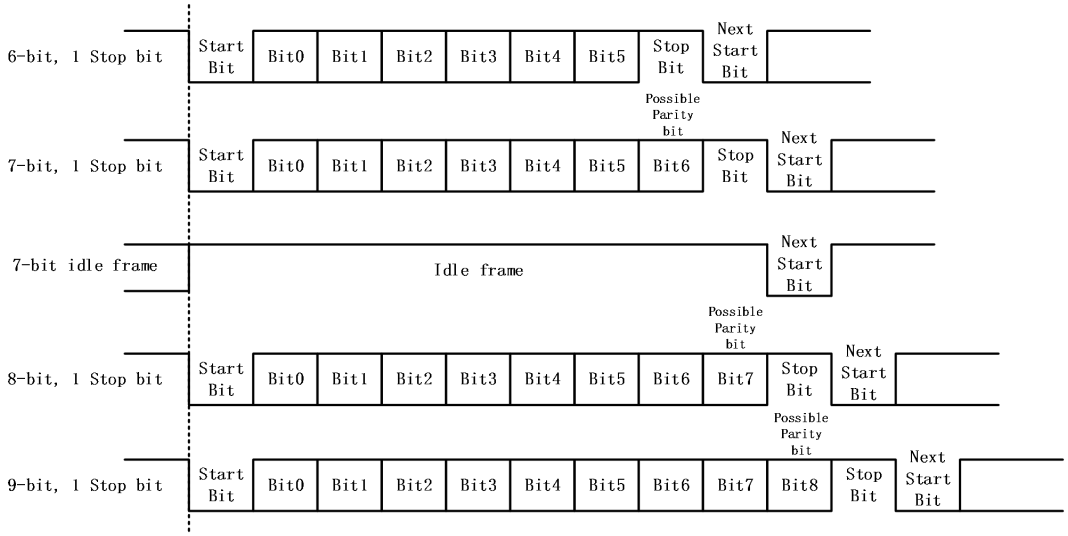


20.4 Frame structure

By programming the DATLEN bit of the LPUART_MODE register, the length of the data frame can be set from 5 to 8 bits. The format of a data frame is: start bit + data bit + check bit + stop bit.

By default, the start bit of TX and RX is low and the end bit is high, or the polarity of each bit can be reversed by polarity configuration. The parity bit is set to the last bit of the data, and the stop bit can be set to 1bit or 2bit. if the parity bit selects the user-defined parity bit and sets the high data to be sent first, the parity bit will be sent first.

An idle frame is a segment of a consecutive frame of data length including start and stop bits that is high, counting from the end of the stop bit of the previous frame, and the length of the idle frame varies with the length of the data.



20.5 FIFO function

The LPUART has a transmit FIFO and a receive FIFO with a width of 9 bits, and the depth of the FIFO is 4.

When the transmit FIFO state is empty/half empty, and the receive FIFO state is non-empty/full/half-full, interrupt flags will be set, and interrupt enable can be configured. The transmit and receive FIFOs are reset when the transmit enable and receive enable are turned on respectively.

When the transmitter is enabled, the instruction to write data to the LPUART_TXD register adds one data to TXFIFO, and the data written to the LPUART_TXD register is queued in TXFIFO. The write operation can be continued when TXFIFO is set up with both empty and half empty flags, and there is no need to judge whether TXFIFO is full or not at each write:

① Software-controlled writing of 4 bytes to TXFIFO when TXFIFO empty flag is generated;

② Software control to write 2 bytes to TXFIFO when TXFIFO half empty flag is generated.

The non-empty/half-full/full-full flags of the RXFIFO on the receive side all indicate that the data is ready to be read, and reading LPUART_RXD will return the earliest data entered into the RXFIFO.

① When the RXFIFO is full, the interrupt software can be generated to read 4 bytes of data at a time;

② When RXFIFO is half full, an interrupt can be generated, and the software reads 2 bytes of data at a time.

③ When the receiving end detects an idle frame, it is recognized as the end of the current packet transmission and automatically turns off the baud rate generator enable, and when the interrupt signal is enabled it can generate an idle interrupt for the software to read the data in the RXFIFO.

20.6 Transmitting engine

20.6.1 Transmission characteristics

The transmit engine includes a transmit control register, a transmit buffer register, and a transmit shift register. The transmit engine can send data length, parity bit, and stop bit width according to the configuration of the control register.

The transmit enable bit TE is set to the transmit control register on the first transmission, and TE cannot be reset during data transmission.During LPUART transmission, the TX pin sends the lowest bit LSB first by default.

Writing data to be sent to LPUART_TXD adds one data to TXFIFO and the written data is queued in TXFIFO. Reading the LPUART_TXD register returns the earliest data in the TXFIFO.

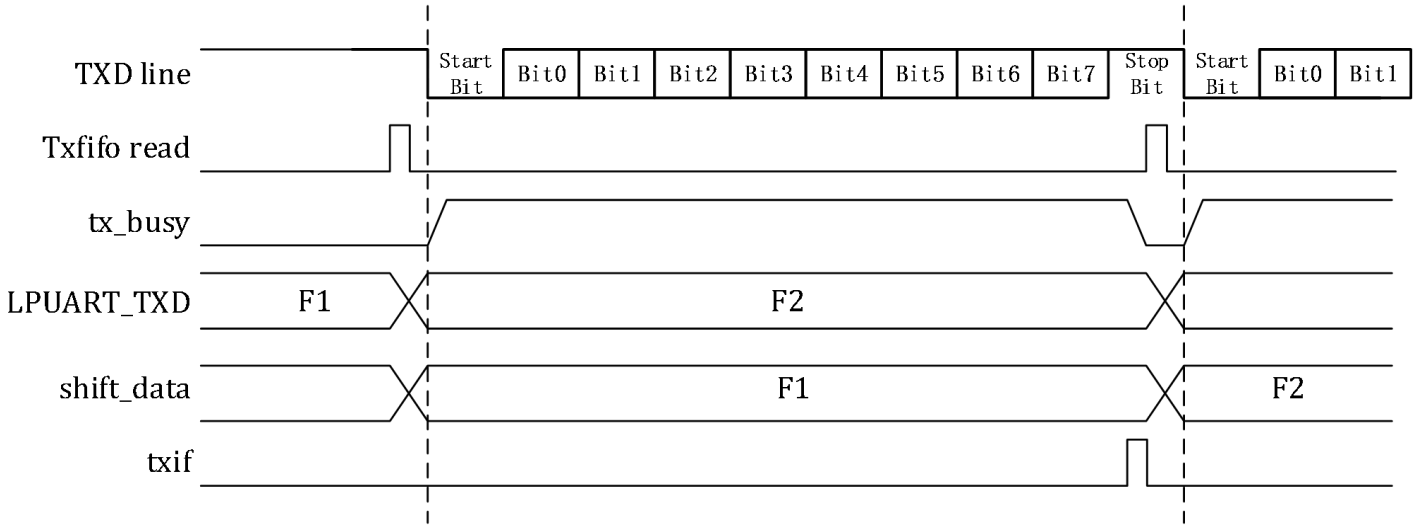
After all the data has been written, you must wait until both the TXIF bit and the TXFFIF bit of LPUART_STA are equal to 1, indicating that all frames have been sent and that both the TXFIFO and the shift register are empty, before you can enter SLEEP mode.

20.6.2 Single-byte communication flow

The TXFNFIF flag is set to 1 by hardware to indicate that the TXFIFO is not full and the next data can be written to the LPUART_TXD register without overwriting the old data.

When transmitting, the write instruction to the LPUART_TXD register stores the data in the TXFIFO, and copies the data to the shift register when the transmission currently in progress is finished.When the TXFIFO is empty, TXFEIF is 1, indicating that 4 bytes can be written to the TXFIFO; when it is half-empty, TXFHEIF is 1, indicating that 2 bytes can continue to be written. If TXFIFO interrupt is enabled, it can generate empty/half empty interrupt.

If the current frame has been sent, indicating that the buffer register is empty, TXIF will go high at the last end bit of a frame. An interrupt can be generated if TXIE is set. After writing the last data to the register, you must wait for TXIF=1 and TXFEIF=1 before disabling the LPUART or the MCU enters SLEEP mode.



Single-byte transmit timing schematic diagram

20.7 Receiver engine

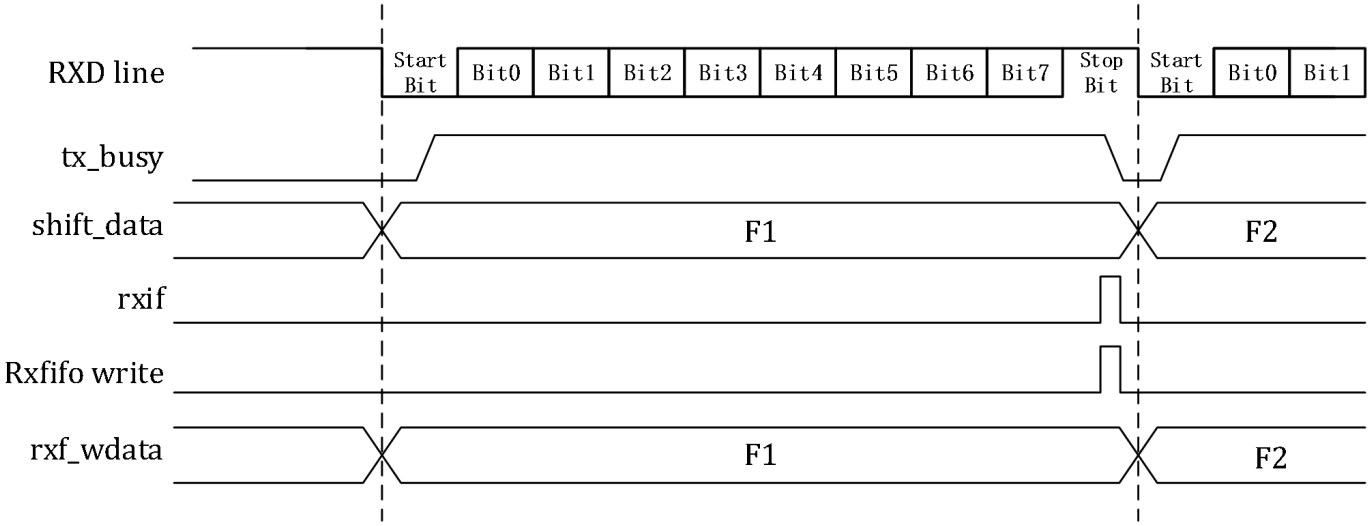
20.7.1 Transmission Characteristics

The data bits are 5/6/7/8bit wide and the DATLEN bit and stop bit length STOPS are set in the LPUART_MODE register.

During LPUART reception, the data is first shifted the lowest bit through the RX pin. If the internal loopback is enabled, the transmitter TX and the receiver RX are shorted inside the module.

The RXFNEIF bit is 1, indicating that RXFIFO is not empty, and reading LPUART_RXD will return the earliest data entered into RXFIFO. The RXFNE bit is cleared to zero when RXFIFO is empty.When RXFIFO is full, the first data in RXFIFO must be read before ending reception of the next character to avoid an overflow error.

If a frame error, noise error, or overflow error has been detected during reception, it corresponds to error flag position 1.



Single-byte receive timing schematic diagram

20.7.2 Start Bit Detection

The falling edge of the RX line is detected, and then the middle of the start bit is sampled to confirm that it is maintained as 0. If the start bit sampling judgment is 1, the noise error flag NEIF is set, the start bit is discarded, and the receiver waits for a new start bit.

20.7.3 Stop Bit Detection

1 stop bit ： Sampling at the stop bit sampling position

2 stop bit ： sampling at the position of the second stop bit, the first stop bit is not used to check for frame formatting errors

20.7.4 Idle frame detection

When enabling RXFIFO, if the RXFIFO is set with half-full or full-full flag but does not reach the FIFO threshold after receiving the last frame, it is possible that the FIFO has been waiting for the received data, resulting in that the cached data is not read out in time, and it is necessary to utilize the idle frame detection to determine this.

Software usage example: When the receive enable is turned on and data is received, idle frame detection is turned on, and when a high level on the RX line is detected for more than one frame of data length, an idle frame interrupt flag is generated, and if the interrupt is enabled, it enters the corresponding interrupt service program. When the flag is set, idle frame detection is stopped until the next time there is data reception and then restart detection. If the idle frame interrupt is enabled, an interrupt flag can be generated.

20.7.5 Reception error

1）Overflow error

An overflow error occurs when the receive shift register is ready to pass data to the FIFO and the receive FIFO is full. Data cannot be transferred from the shift register to the LPUART_RXD register until a free location exists in the RXFIFO.The RXFIFO is set with full and half-full flags, and an overflow error occurs if new data is received with RXFFIF=1. When an overflow error occurs: the OEIF position is 1, the data in the RXFIFO will not be lost, the shift register will be overwritten, and any data received during the overflow will be lost.

2）Frame format error

When the end bit is not recognized at the expected receive time (i.e., stop bit sample value = 0). When a frame error is detected: the FEIF is set by hardware, invalid data is transferred from the shift register to LPUART_RXD. single-byte communication, the module generates an interrupt by the RXFNE bit, and the FEIF is set if a frame format error occurs.

20.7.6 Baud rate generator

In the LPUART module, the baud rate selection at the TX side is generated using fractional division, and the register bit-width modulation configurations MCTL[11:0] corresponding to different baud rates need to be configured separately, and MCTL[0] must be configured as 1.

Table: LPUART Bitwidth Modulation Configuration MCTL[11:0]

Baud rate /bps	LPUART_BAUD[2:0]	LPUART_BAUD[27:16].MCTL
300	101/110/111	0x111
600	100	0xB6D

1200	011	0x249
2400	010	0x6DB
4800	001	0xF7F
9600	000	0x4A5

20.7.7 Parity check bit

Set the PARS parity bit in the LPUART_MODE register. The parity bit can be configured during 5/6/7/8bit length data transfers.

Parity check is performed during reception: if the parity check fails, PEIF of the LPUART_STA register is set to 1; if the PEIE bit is 1 an interrupt is generated. The receiver does not check the user-defined parity bit.

Parity Generation on Transmit: If the PARS bit is not 000 or a user-defined parity bit, the data written in the data register is transmitted first, followed by one parity bit (for even parity, the number of 1's is even; for odd parity, the number of 1's is odd). If the user-defined parity bit is selected on the transmitter side, the parity bit is transmitted first when LMSB = 1.

20.7.8 Low-power wake-up mode

The LPUART receives data and wakes up the CPU in Sleep mode, before the system kernel clock is turned off, it needs to use registers to configure the wake-up method and wake-up interrupt enable, until a specific event arrives to wake up the chip to exit Sleep mode.The LPUART supports four low-power wake-up events, which can be configured in registers: RX falling edge wake-up, start bit wake-up, data reception completion wake-up, and one frame data match wake-up.

Before entering low power mode, LPUART ensures that no data is being sent or received (check the BUSY flag), and turns off the kernel clock when entering sleep mode.The LPUART module clock is not turned off during sleep, and data reception is automatically turned on when the falling edge of RX is detected. It is also necessary to configure the WUSEL select wake-up interrupt event of LPUART_MODE in advance, enable the LPUART low-power wake-up interrupt by setting WUFIE position 1, and turn on the receive enable by setting RE to 1, and then enter SLEEP mode.

When performing a low-power wake-up, in order not to lose data, it is necessary to ensure that the CPU completes the wake-up process before the receive data buffer register/receive FIFO is full, and starts writing data to memory, otherwise an overflow error is likely to occur.

Existing MCUs running the Sleep instruction will only turn off the CPU core clock, the peripheral clocks are not turned off, and it takes 3 pclk for the CPU core to go from generating a wake-up interrupt to entering LCMM mode.

20.7.8.1 RX falling edge wake-up

The chip remains listening on the RX pin in hibernation mode. Configure register LPUART_MODE for RX falling edge detection interrupt enable WUSEL. when in hibernation mode the receiver detects an RX falling edge event turn on the module clock and automatically start data reception and request a wake-up CPU. the falling edge wake-up does not perform the noise detection for the start bit.

20.7.8.2 Wake on Start Bit

Configuration register for start bit detection wakeup. After listening to the falling edge of RX, it is judged to be the start bit when the sampling value of the middle position of the start bit is 0, and a wake-up event is sent to the MCU at the end of the start bit.

20.7.8.3 Wake up when data reception is complete

In sleep mode, after listening to the falling edge of the RX terminal, it starts to receive data and cache it, and after the data is received, it does not match the data and directly generates an interrupt to wake up the CPU.

The wake-up interrupt source of the LPUART can be set to:

RXFNEIF flag (RXFIFO is not empty, 1 byte has been received), RXFNEIE must be set to 1 before hibernation.

RXFHFIF flag (RXFIFO half full, 2 bytes have been received), RXFHFIE must be set to 1 before hibernation.

RXFFIF flag (RXFIFO is full, 4 bytes have been received), RXFFIE must be set to 1 before hibernation.

20.7.8.4 Wake on Frame Data Matching

Configure the MDATA data in the data matching register in advance, and compare the first frame data with the MDATA data bit by bit when the first frame is received in the hibernation mode, if the data matching is successful then the MDATIF flag bit is 1, triggering an interrupt, which can be used to wake up the data reception in the hibernation mode; if the data matching fails then the received data is ignored. In hibernation mode, if RXFNEIF=0, the next received data frame is determined as the first frame for data matching.

20.8 Register description

20.8.1 Register list

Module	Physical address	Mapping address
LPUART	**0x40070000**	**0x40070000**
Register name	**Address offset**	**Description**
LPUART_MODE	0x0	LPUART Mode Configuration Register
LPUART_IE	0x4	LPUART interrupt enable Register
LPUART_STA	0x8	LPUART Status Indicator Register
LPUART_BAUD	0xC	LPUART baud rate modulation register
LPUART_TXD	0x10	LPUART Transmit Data Buffer Register
LPUART_RXD	0x14	LPUART Receive Data Buffer Register
LPUART_DMR	0x18	LPUART Data Match Register

Note: LPUART_MODE & LPUART_BAUD are not allowed to be modified during transmission.

20.8.2 LPUART_MODE（0x00）

LPUART Mode Configuration Register

Reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:15	---	Reserved	R	0
14:13	WUSEL	Wake-up interrupt event configuration 00: START start bit detection 01: RX falling edge detection 10: Data reception completed 11: One frame of data matched successfully	R/W	0
12	ILBE	Enable internal loop back	R/W	0

		0: Internal loop back unable 1: Internal loop back enable, TX and RX shorted inside the module		
11	LMSB	LSB/MSB transmission mechanism selection method 0: LSB first pass 1: MSB first pass Note: When PARS is selected as user-defined parity, the parity bit is treated as the highest bit of the data extension, and if the selection mode is MSB at this time, the parity bit will be transmitted first.	R/W	0
10	STOPS	Stop Bit Width Selection 0: 1-bit stop bit 1: 2-bit stop bit	R/W	0
9:7	PARS[2:0]	Check Digit Selection Bit 000: No calibration 001: odd calibration 010: Even Check 011: Fixed to 0 checksum 100: fixed to 1 checksum 101/110/111: User-defined checksums	R/W	0
6:5	DATLEN[1:0]	Transmit data width bits (excluding parity bits) 00: 5-bit 01: 6-bit 10: 7-bit 11: 8-bit	R/W	0
4	IRPOL	Infrared modulation output polarity selection 0: Positive polarity, the default drive level is held high, low level modulation outputs 1: Negative polarity, the default drive level is kept low, and high level modulation is output Note: IRSEL only determines the level during idle output (invalid level) and does not affect the level during valid data	R/W	0
3	NEG	Transmit and receive data polarity configuration 0: positive polarity, default drive level is high 1: Negative polarity, default drive level is low	R/W	0
2	IRE	Infrared Modulation Output Function Configuration 0: Closed 1: Open	R/W	0
1	RE	LPUART receiver enable bit 0: Closed 1: Open	R/W	0
0	TE	LPUART transmitter enable bit 0: Closed 1: Open	R/W	0

20.8.3 LPUART_IE（0x04）

LPUART Interrupt Enable Register

Default reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:14	---	Reserved	R	0
13	RXFFIE	Receive FIFO full interrupt flag enable 0: disable 1: enable	R/W	0
12	RXFHFIE	Receive FIFO half full interrupt flag enable 0: disable 1: enable	R/W	0
11	RXFNEIE	Receive FIFO non-air-break flag enable 0: disable 1: enable	R/W	0
10	TXFHEIE	Send FIFO half empty interrupt flag enable 0: disable 1: enable	R/W	0
9	TXFEIE	Transmit FIFO Empty Flag Enable 0: disable 1: enable	R/W	0
8	IDLEIE	Idle frame detection interrupt enable 0: disable 1: enable	R/W	0
7	NEIE	Start Bit Noise Detection Enable 0: disable 1: enable	R/W	0
6	DEIE	Data Error Enable 0: disable 1: enable	R/W	0
5	FEIE	Frame format error enable 0: disable 1: enable	R/W	0
4	OEIE	Overflow Error Enable 0: disable 1: enable	R/W	0
3	PEIE	Parity error enable 0: disable 1: enable	R/W	0
2	WUFIE	To wake up the interrupt enable from hibernate mode, the interrupt enable must be turned on before entering hibernate mode, and is only valid in hibernate mode WUF. The software turns off this interrupt enable after wakeup. 0: disable	R/W	0

		1: enable		
1	RXIE	Receive data completion interrupt enable 0: disable 1: enable	R/W	0
0	TXIE	Send Data Completion Interrupt Enable 0: disable 1: enable	R/W	0

20.8.4 LPUART_STA（0x08）

LPUART Status Indicator Register

Reset value: 0x0

Write 0x3ff reset

Bit	Name	Description	R/W	Reset Value
31:24	---	Reserved	R	0
22:20	RXFCNT[2:0]	Number of data in the receive FIFO	R	0
19:17	TXFCNT[2:0]	Number of data in the send FIFO	R	0
16	RXFFIF	Receive FIFO full interrupt flag bit, write 1 to clear it 0: not full 1: Full	R/W	0
15	RXFHFIF	Receive FIFO half-full interrupt flag bit, indicates that the receive FIFO has 2 data, write 1 to clear the bit 0: not half full 1: Half full	R/W	0
14	RXFNEIF	Receive FIFO non-empty interrupt flag, write 1 to clear it 0: Empty 1: Non-empty	R/W	0
13	TXFF	Send FIFO full flag, write 1 to clear it or hardware auto-clear it 0: Not yet full 1: Full	R/W	0
12	TXFHEIF	Send FIFO half empty interrupt flag bit, indicates that there are two empty bits in the send FIFO, write 1 to clear it 0: Not half empty 1: Half empty	R/W	0
11	TXFEIF	Send FIFO empty interrupt flag bit, write 1 to clear it 0: non-empty 1: Empty	R/W	1
10	RBUSY	Receive Status Flag Bit 0: No reception 1: Data being received	R	0
9	TBUSY	Transmit Status Flag Bit 0: not sent 1: Flag bit being sent	R	0

8	IDLEIF	Idle frame detection interrupt flag, write 1 to clear it 0: No idle frame detected 1: Idle frame detected	R/W	0
7	NEIF	Start bit noise detection flag, write 1 to clear it 0: No noise 1: There is noise	R/W	0
6	DEIF	Data error flag, write 1 to clear Continuing to write the LPUART transmit register after the LPUART transmit FIFO has been filled sets this bit up 0: No error 1: There is an error	R/W	0
5	FEIF	Frame format error flag bit, write 1 to clear it The data received by the LPUART does not conform to the frame format flag bit, i.e., the received stop bit is a 0 instead of a 1, and this bit is set 0: No error 1: There is an error or an interrupt character is detected	R/W	0
4	OEIF	Overflow error flag bit, write 1 to clear it LPUART receive data buffer register not read in time causing receive overflow 0: No error 1: There is an error	R/W	0
3	PEIF	Parity error flag bit, write 1 to clear it 0: No error 1: There is an error	R/W	0
2	WUF	Receive wakeup event flag, write 1 to clear it 0: No wakeup event occurred 1: A wake-up event has occurred Wake-up events are selected by WUSEL: RX falling edge wake-up, start bit detection wake-up, data reception completion wake-up, one frame data matching wake-up	R/W	0
1	RXIF	Receive complete interrupt flag, write 1 to clear 0: Receive data not completed 1: Receiving data is complete and can be read from the data buffer registers Triggered at the completion of each frame reception.	R/W	0
0	TXIF	Send completion interrupt flag, write 1 to clear 0: Sending not completed 1: Sending completed Triggered when the STOP bit of the currently sent byte has been sent.	R/W	0

Note: The software reads and writes the data first after entering the FIFO interrupt and clears the flag bits later.

20.8.5 LPUART_BAUD（0xC）

LPUART baud rate modulation register

Reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:28	---	Reserved	R	0
27:16	MCTL	Bit-width modulation signal corresponding to each bit of LPUART. Recommended bit-width modulation values for different baud rates (bps): 9600: 0x4A5 4800: 0xF7F 2400: 0x6DB 1200: 0x249 600: 0xB6D 300: 0x111	R/W	0
15:3	---	Reserved	R	0
2:0	BAUD	Baud rate control (bps) 000: 9600 001: 4800 010: 2400 011: 1200 100: 600 101/110/111: 300 Note: The baud rate modulation register can only be modified when the enable is turned off.	R/W	0

20.8.6 LPUART_TXD（0x10）

LPUART Transmit Data Buffer Register

Reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:9	---	Reserved	R	0
8	UP	User-defined parity bits	R/W	0
7:0	TXDATA	Transmit Data Register Note: Transmit data can only be written after the transmit enable is turned on.	R/W	0

20.8.7 LPUART_RXD（0x14）

LPUART Receive Data Buffer Register

Reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:9	---	Reserved	R	0
8	UP	check bit	R	0

7:0	RXDATA	Receive Data Register	R	0

20.8.8 LPUART_DMR（0x18）

LPUART Data Match Register

Reset value: 0x0

Bit	Name	Description	R/W	Reset Value
31:8	---	Reserved	R	0
7:0	MDATA	Compare with the received first frame data, if the data is detected to be the same, trigger the wake-up interrupt for receiving wake-up in sleep mode.	R/W	0

Note: This register can be written only when receive is not enabled.

20.9 Software Operation Procedure

20.9.1 Send process

1）Configure LPUART configuration register LURT_CFG[2:0] to select LPUART and UARTx multiplexing IO configuration and configure the multiplexing pins;

2）Write 1 to the module enable 0 register MOD0_EN[25].LPUART_EN bit to enable the LPUART module;

3）Set the configuration of character length, stop bit width, parity method, baud rate, interrupt enable, etc;

4）Write 0x1ffff to clear the LPUART_STA register state;

5）Configure LPUART interrupt enable and priority, and write interrupt service program. LPUART receive, transmit, and error interrupts are the same interrupt entry, and it is necessary to judge what kind of interrupts according to the interrupt enable bit and status flag.

6）Enable the transmitter by setting TE bit 1 to LPUART_MODE during the first transmission;

7）Write data to the transmit data buffer register;

8）Wait for an interrupt event and continue writing data to the transmit data buffer register.

20.9.2 Receiving process

1）Configure LPUART configuration register LURT_CFG[2:0] to select LPUART and UARTx multiplexing IO configuration and configure the multiplexing pins;

2）Write 1 to the module enable 0 register MOD0_EN[25].LPUART_EN bit to enable the LPUART module;

3）Set the configuration of character length, stop bit width, parity method, baud rate, interrupt enable, etc;

4）Write 0x1ffff to clear the LPUART_STA register state;

5）Configure LPUART interrupt enable and priority, and write interrupt service program. LPUART receive, transmit, and error interrupts are the same interrupt entry, and it is necessary to judge what kind of interrupts according to the interrupt enable bit and status flag;

6）Enable the receiver side by setting RE bit 1 to LPUART_MODE before the first reception;

7）Wait for an interrupt event to process received data and errors.

21 CRC (new)

21.1 Overview

Cyclic redundancy check (CRC) is mainly used to detect or verify the integrity of data transmission or storage. The CRC calculation unit uses a polynomial generator to generate a CRC code from an 8bit/16bit/32bit data.

CRC calculations for 7816, I2C, UART and SPI module data can be performed through software control.

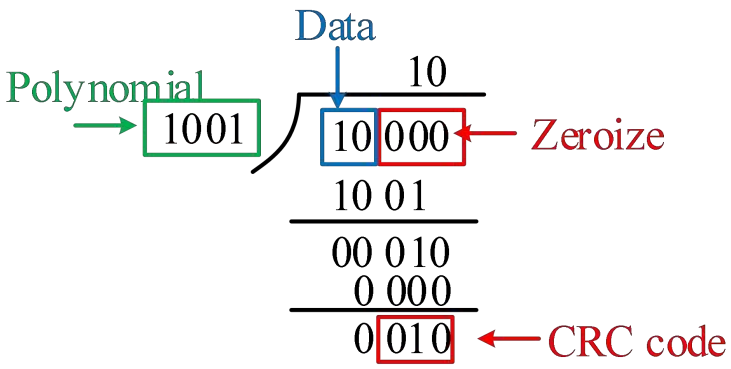
21.2 Specificities

- Supports 7/8/16/32 bit CRC, supports arbitrary polynomials
- Handles 8-bit, 16-bit, and 32-bit data sizes
- Programmable CRC Initial Value
- Supports input data inversion by byte/half word/full word
- Supports output results inversion, XOR
- 1 cycle to complete 8bit CRC operation, 4 cycles to complete 32bit operation
- Supports general-purpose DMA function

21.3 Rationale

The basic principle of CRC, using the transmitted data divided by another number (polynomial) to get the remainder is the CRC code.

The most basic CRC operation uses modulo 2 division, modulo 2 division of each bit of the result does not affect the other bits, that is, not borrowing bits from the previous bit, so in fact it is the bit by bit isomorphism, each calculation needs to be shifted left by 1 bit, when the number of bits of the divisor is less than the divisor, the result will be the remainder.



The most basic CRC division has the obvious flaw that adding some zeros to the beginning of the data doesn't affect the result of the final checksum word, and it also requires complete data to calculate the CRC code. In fact, the real CRC calculation is based on the original CRC algorithm with some minor changes. Two concepts have been added. The first is the initial value of the remainder, and the second is result XOR value.

21.4 Polynomial

Polynomials whose highest and lowest bits must be 1 are commonly used as follows:

$CRC8 = X^8 + X^5 + X^4 + 1$

CRC-CCITT$= X^{16} + X^{12} + X^5 + 1$

CRC16$= X^{16} + X^{15} + X^2 + 1$

CRC32$= X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X^1 + 1$

The bit-width of a polynomial is the number of its binary bits minus one, e.g., CRC8 has a bit-width of 8, but the binary number has nine bits. In order to shorthand the value of a polynomial, it is expressed in hexadecimal writing, because the highest bit of polynomial must be 1, and the highest bit is omitted from the shorthand, e.g. the shorthand for CRC-CCITT is 0x1021, which actually represents 0x11021.

21.5 Initial value of the remainder

The remainder initial value is what gives the CRC register an initial value at the beginning of the CRC value calculation. In a segmented CRC calculation, the result of each calculation is used as the initial value of the remainder for the next calculation. For example, if you use the CRC-CCITT polynomial's computation model for 16-bit data to compute the 32-bit data 0xaabbccdd, you first compute the CRC value of the high 0xaabb, then you use that value as the residual initial value to compute the CRC value of 0xccdd, and you compute the CRC value of 0xccdd, and the final result is equivalent to the CRC value of 0xaabbccdd.

21.6 Result XOR value

The resulting XOR value is the value of the CRC register that is used as the final check value after the XOR operation with this value is completed.

21.7 Input Data Reversal

Supports input data, bit reversal by byte, bit reversal by half-word, and bit reversal by word.

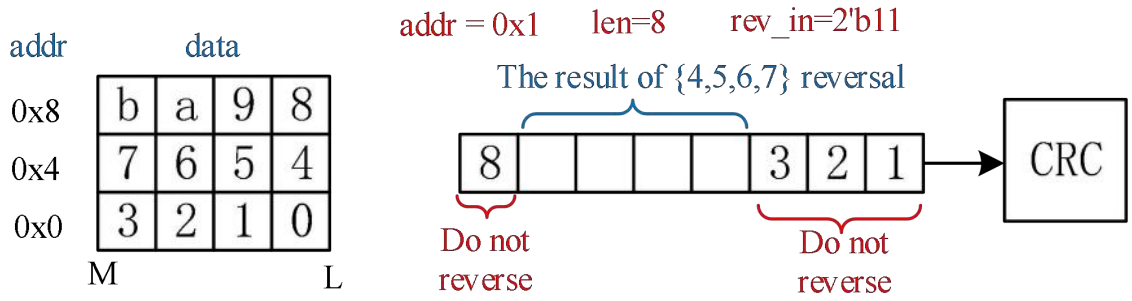
Example: Input data as 0x1A2B3C4D

- Perform bit reversal by byte, data becomes 0x58D43CB2; //[31:0]->[0,1,2,3,……,31]
- Perform bit reversal by half-word, data becomes 0xD458B23C; //[31:0]->[16,15…...,31,0,1….15]
- Performing bit reversal by word, the data becomes 0xB23CD458. //[31:0]->[24,…,31,16,…,23,8..,15,0,…,7]

When the effective data bit width is not equal to a multiple of the inverted bit width, the inversion will not be executed. Example Valid data data[7:0], set to execute inversion by half word/word, will not execute the inversion operation.

The DMA fetch will determine whether it can be inverted based on the valid data fetched at the current address.

Exception, Example: Start address is 0x1, perform bit reversal by word, first fetched data is {1,2,3}, only 24bit valid data, no reversal, second fetched data is {4,5,6,7}, 32bit valid data, perform bit reversal by word. The third fetched data is {8}, only 8bit valid data, no inversion.

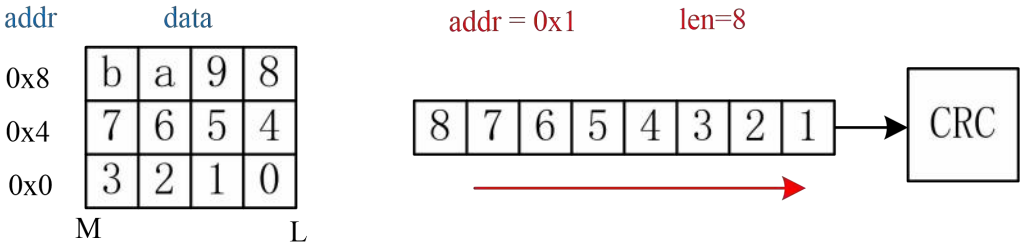


21.8 DMA interface

The CRC module reads data from SRAM via DMA and performs checksums, the results of which are still stored in registers.

21.8.1 CRC calculation

Data calculation order: start from the lowest byte of the address. Example: In the following figure, each square represents 1 byte, the starting address is 0x1, and the length is 8. Data {1,2,3,4,5,6,7,8} is obtained by DMA. The CRC calculation is performed in this order. That is, the CRC of "1" is calculated first, and then the CRC of "2" is calculated until the last byte.



21.8.2 Checksum calculation

Checksum calculation is only used when CHKSUM_DMA is enabled, and the accumulative bit width can be determined as 8bit/16bit/32bit by setting CRC_CR.OPDW, and the calculation result is saved as 32bit in CRC_DR register. It supports setting the initial value of calculation, output inversion and XOR, and input data inversion, but when the effective data bit width is not equal to a multiple of the inverted bit width, the inversion will not be executed.

Output inversion is to invert the 32bit result.

Set the accumulation bit width to 8bit, and the length and start address of the DMA can be any value;

Set the accumulation bit width to 16bit, the DMA length can be any value, the lower two bits of the start address must be 0, and configure other values will be 0. When the remaining length does not meet the 16bit, It will automatically add zeros in the high bit.

Set the accumulation bit width to 32bit, the DMA length can be any value, the lower two bits of the start address must be 0, and configure other values will be 0. When the remaining length does not satisfy 32bit, It will automatically add zeros in the high bit.

21.9 Computational speed assessment

21.9.1 CRC calculations

Configuration register calculations take 1 cycle for 8bit data, 2 cycles for 16bit data, and 3 cycles for 32bit data.

When using DMA, the length n*byte, the fastest it can take is 4+n cycles to complete, the actual operation cycle

is also related to the configured address as well as the SRAM contention.

21.9.2 Checksum calculation

Accumulation bit width is 8bit, DMA length is n*byte, and it takes 4+n cycles to complete at the fastest.

Accumulation bit width is 16bit, DMA length is n*byte, the fastest time required is 2+ n/4 *3 cycles to complete.

Accumulation bit width is 32bit, DMA length is n*byte, the fastest time to complete is 2+ n/4 *3 cycles.

21.10 Register description

Register list

Base address of the CRC module

Module name	Physical address	Mapping address
CRC	0x40074000	0x40074000

Register offset address of the CRC module

Register name	Address offset	Description
CRC_DR	Offset+0x0	CRC Data Register
CRC_STA	Offset+0x4	CRC Status Register
CRC_CTRL	Offset+0x8	CRC Control Register
CRC_INIT	Offset+0xC	CRC initial value register
CRC_POL	Offset+0x10	CRC polynomial register
CRC_XOR	Offset+0x14	CRC output XOR register
CRC_DMA_CTL	Offset+0x18	CRC DMA control register
CRC_DMA_BADR	Offset+0x1C	CRC DMA Start Address Register
CRC_DMA_LEN	Offset+0x20	CRC DMA Data Length Register
CRC_DMA_ADR	Offset+0x24	CRC DMA Current Address Register
CRC_DMA_IE	Offset+0x28	CRC DMA Interrupt Enable Register
CRC_DMA_FLG	Offset+0x2C	CRC DMA Interrupt Flag Register

21.10.1 CRC_DR（0x00）

CRC Data Register

Offset address = 0x0

Bit	Name	Description	R/W	Reset Value
31:0	DR	CRC calculations: This register is used as a data input register and saves the result of the CRC calculation at the end of the operation. When writing to this register, it is used as a data input register, and the CRC is calculated once for each data write, and the write is	R/W	0

		invalidated when DMA is enabled; When this register is read, the result of the CRC calculation is returned. When used as input: If OPDW==00, write data DR[31:0] is valid; If OPDW==01, write data DR[15:0] is valid; If OPDW==1x, write data DR[7:0] is valid. When saving results: If it is a 7-bit polynomial result is saved in DR[6:0]; If it is an 8-bit polynomial result is saved in DR[7:0]; If it is a 16-bit polynomial result is saved in DR[15:0]; If it is a 32-bit polynomial result is saved in DR[31:0]. Note: The CRC is calculated on a byte basis, first for DR[7:0], then for DR[15:8] up to the last valid byte. Checksum calculation: This register is used only to save the result of the checksum. write is disabled when DMA is enabled.		

21.10.2 CRC_STA（0x04）

CRC Status Register

Offset address = 0x04

Bit	Name	Description	R/W	Reset Value
31:1	---	Reserved	R	0
0	DONE	CRC operation completion flag 0: CRC operation not completed 1: CRC operation completed When using DMA, the CRC operation is complete when all the DMA data has completed the operation.	RO	1

21.10.3 CRC_CTRL（0x08）

CRC Status Register

Offset address = 0x08

Bit	Name	Description	R/W	Reset Value
31:9	---	Reserved	R	0
7:6	OPDW	Calculate data bit width selection (Operation by data width) 00: 32bit data calculation 01: 16bit data calculation 1x: 8bit data calculation When DMA is not enabled, it is used as the calculated data bit	R/W	00

		width selection for writing registers to calculate the CRC. When CRC_DMA is enabled, the hardware performs adaptive calculations based on the DMA length, and this configuration is invalid. When CHKSUM_DMA is enabled, it is used as a selection of the accumulation bit width. Configured at the time of the CRC operation and will be used as the configuration for the next calculation. Unmatched in checksum operations, invalid configuration		
5:4	REV_IN	Reverse input data 00: No reversal 01: Perform bit reversal by byte 10: Perform bit reversal by half word 11: Perform bit reversal by word For example, the calculated data is 0x1A2B3C4D REV_IN==00, calculated directly using data 0x1A2B3C4D; REV_IN==01, change the data to 0x58D43CB2 and calculate again; REV_IN==10, change the data to 0xD458B23C and calculate again; REV_IN==11, change the data to 0xB23CD458 and calculate again. When the effective data bit width is not equal to a multiple of the inverted bit width, no inversion is performed (see 29.7 for a detailed description). Not configurable at computing time, configuration is invalid.	R/W	00
3	REV_OUT	Reverse output data 0: Output not inverted 1: Output inverted by CRC result bit length For example, the CRC result is 0xAABB REV_OUT==1, the output is 0xDD55; REV_OUT==0, the output is 0xAABB. The checksum calculation will be inverted according to 32bit. Not configurable at computing time, configuration is invalid.	R/W	0
2	XOR	Enable bitwise XOR of output data 0: Output data is not operated 1：XOR of output data and CRC_XOR register value Not configurable at computing time, configuration is invalid.	R/W	0
1:0	POLYSIZE	polynomial size 00: 32-bit polynomial 01: 16-bit polynomial 10: 8-digit polynomial 11: 7-digit polynomials Not configurable during CRC operations, invalid configuration	R/W	00

		This configuration bit is not used in checksum calculations.		

21.10.4 CRC_INIT（0x0C）

CRC initial value register

Offset address = 0x0C

Bit	Name	Description	R/W	Reset Value
31:0	INIT	CRC initial value. If 32-bit polynomial size is selected, INIT[31:0] is valid; If 16-bit polynomial size is selected, INIT[15:0] is valid; If 8-bit polynomial size is selected, INIT[7:0] is valid; If a 7-bit polynomial size is selected, INIT[6:0] is valid. Not configurable at computing time, configuration is invalid. CRC calculations: When using the configuration register to calculate the CRC, the register is not configured before performing the CRC calculation, then the initial value of the remainder will use the result of the previous data calculation. When using DMA, the value of this register is automatically adopted as the initial value of the remainder without reconfiguration; if the initial value of the remainder needs to be changed, it must be configured before the calculation. Checksum calculation: As the initial value for accumulation.	R/W	0

21.10.5 CRC_POL（0x10）

CRC polynomial register

Offset address = 0x10

Bit	Name	Description	R/W	Reset Value
31:0	POLY	Polynomial for CRC calculations, lowest significant bit is used if the polynomial is less than 32 bits Writing the value of a polynomial ignores the value of the highest bit. For example, the polynomial for CRC-CCITT is x16+x12+x5+1, which in hexadecimal is 0x11021, ignoring the highest bit, the value written is 0x1021 If 32-bit polynomial size is selected, POLY [31:0] is valid; If 16-bit polynomial size is selected, POLY [15:0] is valid; If 8-bit polynomial size is selected, POLY [7:0] is valid; If a 7-bit polynomial size is selected, POLY [6:0] is valid. Not configurable during CRC operations, invalid configuration	R/W	0

21.10.6 CRC_XOR（0x14）

CRC OUTPUT XOR REGISTER

Offset address = 0x14

Bit	Name	Description	R/W	Reset Value
31:0	XOR	CRC operation result XOR register(exclusive OR) 当 When CRC_CR.XOR is 1, the data in this register is XOR before the CRC/checksum result is output. If 32-bit polynomial size is selected, XOR [31:0] is valid; If 16-bit polynomial size is selected, XOR [15:0] is valid; If 8-bit polynomial size is selected, XOR [7:0] is valid; If a 7-bit polynomial size is selected, XOR [6:0] is valid. Not configurable at computing time, invalid configuration	R/W	0

21.10.7 CRC_DMA_CTL（0x18）

CRC DMA Control Register

Offset address: 0x18

Bit	Name	Description	R/W	Reset Value
31:2	Reserved	Reserved	R	0
2	CHANNEL	Data Channel Selection 0: SRAM channel 1: ROM channel	R/W	0
1:0	DMA_EN	DMA Enable. 00: Do not enable DMA; 01: Enable CRC_DMA. 10: Enable CHKSUM_DMA; 11: Reserved, does not enable DMA; One CRC/checksum calculation is performed for each enable, the enable is automatically turned off at the end of the calculation, and the enable needs to be reconfigured for the next calculation. If the checksum calculation is configured during the CRC calculation, the final result will be wrong. If CRC calculation is configured during checksum calculation, the final result will be wrong. If you need to change the calculation during the calculation, you must turn off the DMA and then restart it. Note: It is not allowed to configure DMA_LE	R/W	0

		N=0, DMA_EN=1, otherwise DMA_EN will always be 1 and will not be cleared automatically, and the DONE flag will always be 0. If DMA_LEN=0, DMA_EN=1 are configured, DMA_EN needs to be written to 0 before the next calculation.		

21.10.8 CRC_DMA_BADR（0x1C）

CRC DMA Start Address Register

Offset address: 0x1C

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reservations.	R	0
16:0	DMA_BADR	DMA start address (Byte address) When the checksum calculation uses 16/32bit accumulation, the lower two bits must be 0. The lower two bits are not valid even if they are configured. Other cases can be configured arbitrarily. When using the ROM channel, the address is a maximum of 14 bit	R/W	0

21.10.9 CRC_DMA_LEN（0x20）

CRC DMA Length Register

Offset address: 0x20；

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reservations.	R	0
16:0	DMA_LEN	DMA length (Byte address) = (n) Byte Start address + data length must not exceed the address range of the SRAM When using the ROM channel, the maximum length is 14 bits.	R/W	0

21.10.10 CRC_DMA_ADR（0x24）

CRC Current DMA Address Register

Offset address: 0x24；

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reservations.	R	0
16:0	DMA_ADR	Current DMA address (Byte address)	RO	0

21.10.11 CRC_DMA_IE（0x28）

CRC DMA Interrupt Enable Register

Offset address:0x28

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	Reservations.	R	0
0	CRC_DONE_IE	CRC operation completion interrupt enable = 0, not enabled = 1, enable	R/W	0

21.10.12 CRC_DMA_FLG（0x2C）

CRC DMA Interrupt Flag Register

Offset address: 0x2C；default:0x0

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	Reservations.	R	0
0	CRC _DONE	CRC operation completed interrupt flag, write "1" to clear the bit. The interrupt flag is set when all the data of the DMA has been calculated. This flag will not be raised if the software turns off the DMA.	R/WC	0

21.11 CRC Software Operation Procedure

21.11.1 Configure the DR register for calculations

21.11.1.1 Calculation of single data

```
CRC_INIT    = 0xxxxx; // the CRC_INIT register must be reconfigured for new data calculations
CRC_CR      = 0xxxxx; // configuration related controls OPDW, REV_IN, REV_OUT, XOR, POLYSIZE
CRC_POL     = 0xxxxx; // configuration polynomial
CRC_DR      = 0xxxxx;// configure calculation data - must be last to configure data
//Wait for the end of the calculation
//8bit data calculation without waiting
// NOP;     // 16bit data calculation wait 1 cycle
// NOP; NOP; NOP;       // 32bit data calculation wait 3 cycles;
crc_result      = CRC_DR[x:0].              //read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured,     crc_result     = CRC_DR[6:0];
//CRC8，            crc_result     = CRC_DR[7:0];
//CRC16,            crc_result     = CRC_DR[15:0];
//CRC32,            crc_result     = CRC_DR[31:0];
```

```
// Use of flag bits
CRC_INIT    = 0xxxxx; // the CRC_INIT register must be reconfigured for new data calculations
CRC_CR      = 0xxxxx; // configuration related controls OPDW, REV_IN, REV_OUT, XOR, POLYSIZE
CRC_POL     = 0xxxxx; // configuration polynomial
CRC_DR      = 0xxxxx; // configure calculation data - must configure data last
while(!(CRC_STA & 0x1));                    // Wait for the flag bit
crc_result  = CRC_DR[x:0];                  // read the result of the CRC calculation
// Read the result according to the configured POLYSIZE
// If CRC7 is configured,crc_result      = CRC_DR[6:0];
//CRC8，            crc_result      = CRC_DR[7:0];
//CRC16,            crc_result      = CRC_DR[15:0];
//CRC32,            crc_result      = CRC_DR[31:0];
```

21.11.1.2 Calculate data multiple times

Take the example of calculating 6byte of data:

```
CRC_INIT    = 0xxxxx; // the CRC_INIT register must be reconfigured for new data calculations
CRC_CR      = 0xxxxx; //configuration related controls OPDW, REV_IN, REV_OUT, XOR, POLYSIZE
                      //OPWD = 2'b00 ;first calculate 4byte data
CRC_POL     = 0xxxxx; //configuration polynomial
CRC_DR      = 0xxxxx;//configuration calculation data, write high 4byte data
CRC_CR      = 0xxxxx; //configuration related controls OPDW, REV_IN, REV_OUT, XOR, POLYSIZE
                      //OPWD = 2'b01 ;then calculate 2byte data
CRC_DR      = 0xxxxx;                       //configure the calculation data, write the last 2byte of data
NOP();                                      //Wait for the calculation to finish
crc_result  = CRC_DR[x:0].                  //read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured,      crc_result      = CRC_DR[6:0];
//CRC8，            crc_result      = CRC_DR[7:0];
//CRC16,            crc_result      = CRC_DR[15:0];
//CRC32,            crc_result      = CRC_DR[31:0];
```

Take the example of calculating 8byte data:

```
CRC_INIT    = 0xxxxx; // the CRC_INIT register must be reconfigured for new data calculations
CRC_CR      = 0xxxxx; //configuration related controls OPDW, REV_IN, REV_OUT, XOR, POLYSIZE
                      //OPWD = 2'b00 ;calculate 4byte data
CRC_POL     = 0xxxxx; //configuration polynomial
CRC_DR      = 0xxxxx; //configure calculated data, write high 4byte data
NOP().
CRC_DR      = 0xxxxx; //configure calculated data, write low 4byte data
NOP().
NOP().
NOP().
```

```
crc_result      = CRC_DR[x:0].   //read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured, crc_result      = CRC_DR[6:0].
//CRC8，          crc_result      = CRC_DR[7:0];
//CRC16,          crc_result      = CRC_DR[15:0];
//CRC32,          crc_result      = CRC_DR[31:0];
```

21.11.2 Calculation using DMA

21.11.2.1 Calculate DMA data

```
CRC_INIT      = 0xxxxx;          //Configure the initial value, if the initial value is unchanged can not be configured
CRC_CR        = 0xxxxx.          //Configuration related controls REV_IN, REV_OUT, XOR, POLYSIZE
CRC_POL       = 0xxxxx;          // Configure the polynomial
DMA_BADR =0xxxxx;                //configure the DAM start address
DMA_LEN       =0xxxxx;                 //configure the DMA data length
DMA_CTL       = 0x1.             //Enable DMA
while(! (CRC_STA & 0x1));        //Wait for the flag bit
crc_result    = CRC_DR [x:0].    //read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured,       crc_result      = CRC_DR[6:0];
//CRC8，          crc_result      = CRC_DR[7:0];
//CRC16,          crc_result      = CRC_DR[15:0];
//CRC32,          crc_result      = CRC_DR[31:0];
```

```
// Use the interrupt flag
CRC_INIT      = 0xxxxx;          //Configure the initial value, if the initial value is unchanged can not be configured
CRC_CR        = 0xxxxx.          //Configuration related controls REV_IN, REV_OUT, XOR, POLYSIZE
CRC_POL       = 0xxxxx;          // Configure the polynomial
DMA_IE        = 0x1.             //interrupt enable
DMA_BADR =0xxxxx;                //configure the DAM start address
DMA_LEN       =0xxxxx;                 //configure the DMA data length
DMA_CTL       = 0x1.             //Enable DMA
while(1);                        // wait for interrupt
---- enters the interrupt program
crc_result    = CRC_DR[x:0] ;    //Read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured,       crc_result      = CRC_DR[6:0];
//CRC8，          crc_result      = CRC_DR[7:0];
//CRC16,          crc_result      = CRC_DR[15:0];
//CRC32,          crc_result      = CRC_DR[31:0];
DMA_FLG     = 0x1;               // write 1 to clear interrupt, exit interrupt
---- exits the interrupt program
```

21.11.2.2 Multi-Segment DMA Data Calculation

```
CRC_INIT      = 0xxxxx;          //Configure the initial value, if the initial value is unchanged can not be configured
CRC_CR        = 0xxxxx.          //Configuration related controls REV_IN, REV_OUT, XOR, POLYSIZE
CRC_POL       = 0xxxxx;          // Configure the polynomial
DMA_BADR =0xxxxx;                //configure the DAM start address
DMA_LEN      =0xxxxx;                 //configure the DMA data length
DMA_CTL       = 0x1.             //Enable DMA
DMA_BADR =0xxxxx;                //configure the DAM start address for the next segment
DMA_LEN      =0xxxxx;                 //configure the DMA data length for the next segment
while(! (CRC_STA & 0x1));        //Wait for the flag bit
crc_result    = CRC_DR [x:0].    //read the result of the CRC calculation
CRC_INIT      = crc_result;      // Configure the initial value
DMA_CTL       = 0x1.             //Enable DMA
while(! (CRC_STA & 0x1));        //Wait for the flag bit
crc_result    = CRC_DR [x:0].    //read the result of the CRC calculation
//Read the result according to the configured POLYSIZE
// If CRC7 is configured,      crc_result      = CRC_DR[6:0];
//CRC8，              crc_result      = CRC_DR[7:0];
//CRC16,              crc_result      = CRC_DR[15:0];
//CRC32,              crc_result      = CRC_DR[31:0];
```

21.11.2.3 Turn off DMA during computation

The CRC operation stops calculating immediately after turning off the DMA.

21.12 Checksum software operation procedure

21.12.1 Calculation using DMA

```
CRC_INIT      = 0xxxxx;          //Configure the initial value, if the initial value is unchanged can not be configured
CRC_CR        = 0xxxxx.          // Configure the related controls REV_IN, REV_OUT, XOR
DMA_BADR =0xxxxx;                //configure the DMA start address
DMA_LEN      =0xxxxx;                 //configure the DMA data length
DMA_CTL       = 0x2.             //Enable DMA
while(! (CRC_STA & 0x1));        //Wait for the flag bit
chksum_result = CRC_DR[31:0];    //read the result of the checksum calculation

//Use the interrupt flag
DMA_FLG       = 0x1;             //write 1 to clear interrupt
CRC_INIT      = 0xxxxx;          //Configure the initial value, if the initial value is unchanged can not be configured
CRC_CR        = 0xxxxx.          // Configure the related controls REV_IN, REV_OUT, XOR
DMA_BADR =0xxxxx;                //configure the DMA start address
DMA_LEN      =0xxxxx;                 //configure the DMA data length
```

```
DMA_CTL      = 0x2.                  //Enable DMA
while(1);                            // wait for interrupt
---- enters the interrupt program
chksum_result = CRC_DR[31:0];        //read the result of the checksum calculation
DMA_FLG      = 0x1.                  //write 1 to clear interrupt, exit interrupt
---- exits the interrupt program
```

21.12.2 Turn off DMA during computation

The checksum operation stops calculating immediately after the DMA is turned off.

22 Pluse forwarding IOCNT(new)

22.1 Overview

Pulse forwarding function, also known as IOCNT function, i.e., it has the function of forwarding the pulses input from GPIO or all the internal metering pulses from GPIO port after frequency division, level inversion and other operations. It also has the function of recording the number of input pulses.

22.2 Functional characteristics

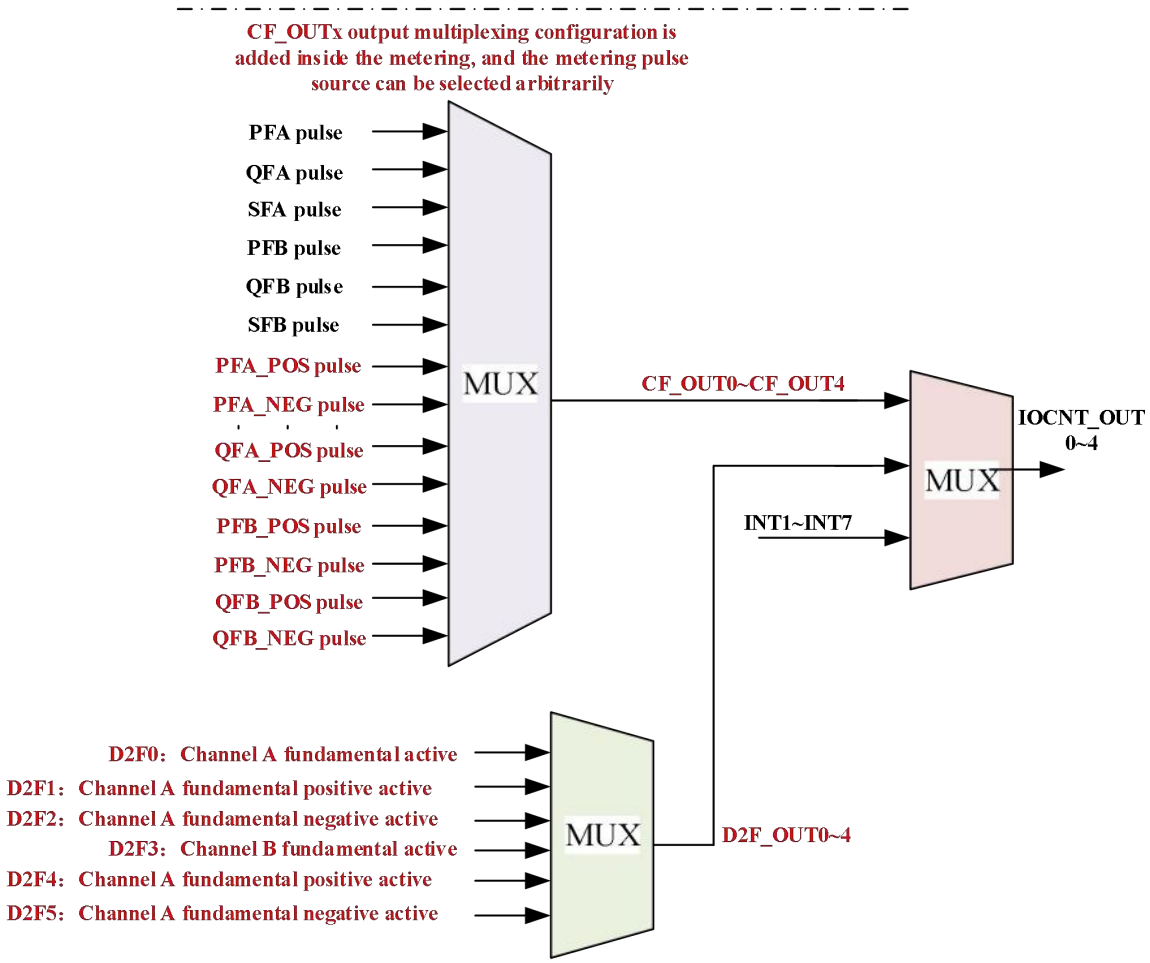
- Support for 5 IOCNT
- Support 1~2048 frequency division
- Supports pulse counting, counting edge can be configured, zero and non-zero after counter reading can be configured.
- Support input pulse level reverse forwarding
- Supports freely assignable input channels

22.3 Reuse relation

All IOCNT_OUTs support internal CF_OUT0~4, D2F_OUT0~4 and INT1~INT7 selectable.

Channel selection IOCNTx_SEL[5:0]	Input	Multiplexed IO		Output	Multiplexed IO		
0x0	CF_OUT0	inside	-	IOCNT_OUT0	P50	P56	-
0x1	CF_OUT1	inside	-	IOCNT_OUT1	P51	-	-
0x2	CF_OUT2	inside	-	IOCNT_OUT2	P57	P13	P10
0x3	CF_OUT3	inside	-	IOCNT_OUT3	P34	P33	P11
0x4	CF_OUT4	inside	-	IOCNT_OUT4	P35	-	P12
0x5	D2F_OUT0	inside	-	-	-	-	-
0x6	D2F_OUT1	inside	-	-	-	-	-
0x7	D2F_OUT2	inside	-	-	-	-	-
0x8	D2F_OUT3	inside	-	-	-	-	-
0x9	D2F_OUT4	inside	-	-	-	-	-
0xA	INT1	P31	P40	-	-	-	-

0xB	INT2	P32	P56	-	-	-	-
0xC	INT3	P33	P41	-	-	-	-
0xD	INT4	P34	P42	-	-	-	-
0xE	INT5	P35	P43	-	-	-	-
0xF	INT6	-	P14	-	-	-	-
0x10	INT7	-	P15	-	-	-	-
0x11	UART0 PF	Inside	-	-	-	-	-
0x12	UART1 PF	Inside	-	-	-	-	-
0x13	UART2 PF	Inside	-	-	-	-	-
0x14	UART3 PF	Inside	-	-	-	-	-
0x15	UART4 PF	Inside	-	-	-	-	-
0x16	UART5 PF	Inside	-	-	-	-	-
0x17	UART0 QF	Inside	-	-	-	-	-
0x18	UART1 QF	Inside	-	-	-	-	-
0x19	UART2 QF	Inside	-	-	-	-	-
0x1A	UART3 QF	Inside	-	-	-	-	-
0x1B	UART4 QF	Inside	-	-	-	-	-
0x1C	UART5 QF	Inside	-	-	-	-	-
0x1D	UART0 FPF	Inside	-	-	-	-	-
0x1E	UART1 FPF	Inside	-	-	-	-	-
0x1F	UART2 FPF	Inside	-	-	-	-	-
0x20	UART3 FPF	Inside	-	-	-	-	-
0x21	UART4 FPF	Inside	-	-	-	-	-
0x22	UART5 FPF	Inside	-	-	-	-	-



22.4 Functional block diagram

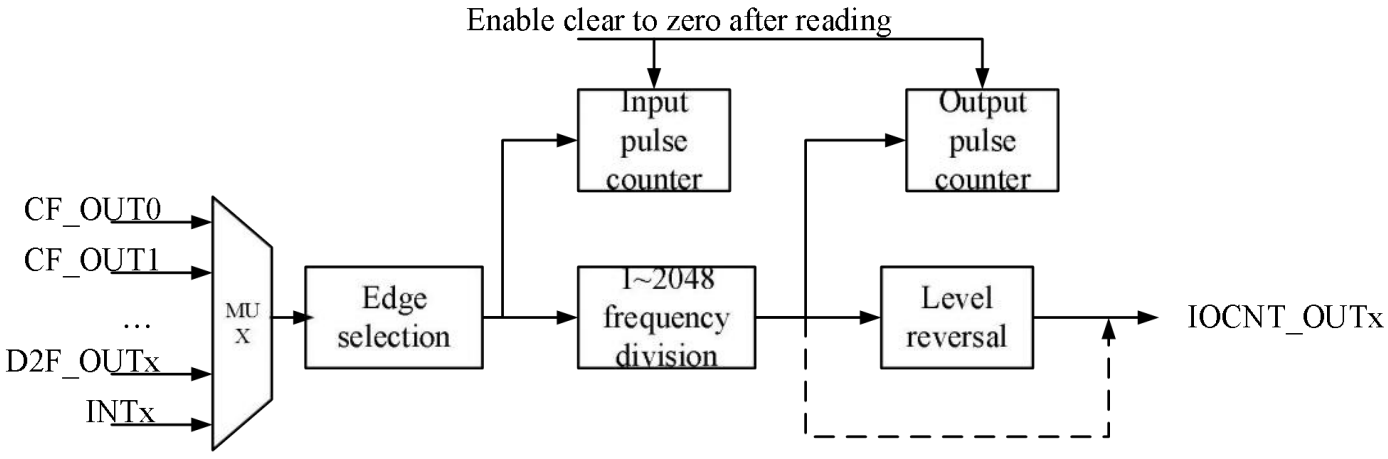


Figure 1 Block diagram of pulse forwarding function

22.5 Waveform analysis

22.5.1 Input Signal Type

The input signals have a uniform distribution of period and a non-uniform distribution of period, and the uniform period case is further divided into the equal duty cycle and unequal duty cycle cases, as shown below.

- Uniform pulse period distribution

Fig. 2 Equal Duty Signal

Fig. 3 Non-equivalent DUTY signals

- Non-uniform distribution of pulse period

Fig. 4 Non-uniform periodic signal

22.5.2 Pulse count

The pulse count is the edge count of the input signal io_in, the rising edge count or falling edge count can be configured via the control registers

Signal Definition:

- io_in：PAD input;
- io_out：the signal between the crossover and the inverter in the diagram above;

22.5.3 Rising edge count

When the input signal io_in input is low by default, it is recommended to use rising edge counting. In this mode io_out outputs low by default.

Startup time point:

- Starts when io_in is low and counts from the first rising edge, as shown in Figure 5
- Started when io_in is high, the count value is incremented by 1, as shown in Figure 6

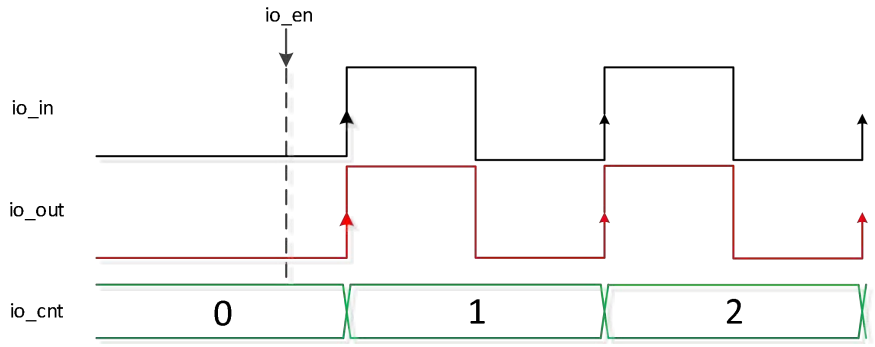


Fig. 5 Low level initiated rising edge counting (pulses not divided)

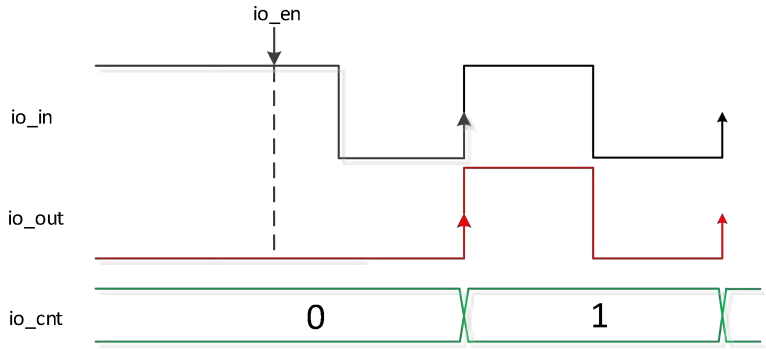


Fig. 6 Rising edge counting initiated at high level (pulses not divided)

22.5.4 Falling edge count

When the input signal io_in input is high by default, it is recommended to use falling edge counting. This mode outputs io_out high by default.

When the io_in state is started high, the first falling edge is valid to start counting, as shown in Figure 7 below.

When the io_in state is started low, the count value is incremented by 1, as shown in Figure 8 below.

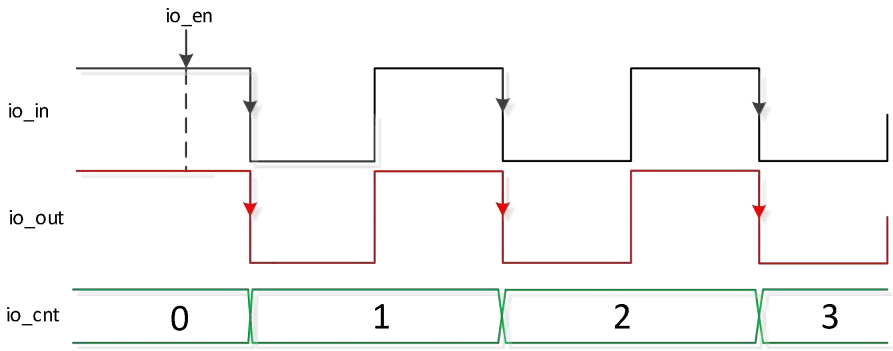


Fig. 7 Falling edge counting initiated at high level (pulses not divided)

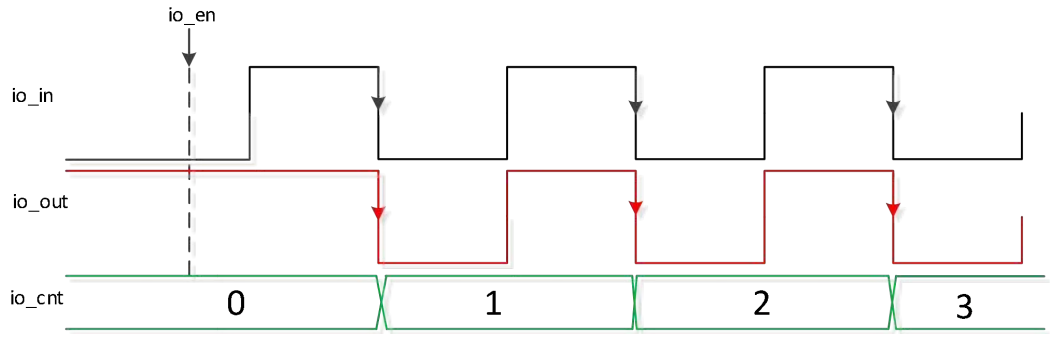


Fig. 8 Falling edge counting with low level start (pulses not divided)

22.5.5 Count Zero and Count Overflow

The historical count value is cleared each time the io_cnt register is read.

- When a read operation arrives before or after an input signal edge change, the current sub-edge accumulates to the next io_cnt, as shown in Figure 9, Figure 10.

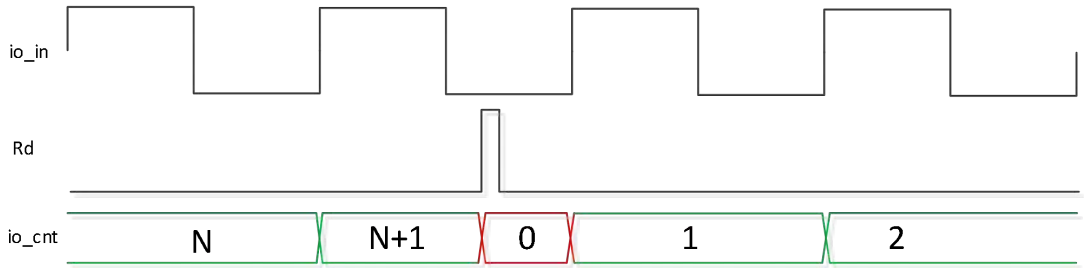


Figure 9 Zero operation before io edge(rising edge counting)…

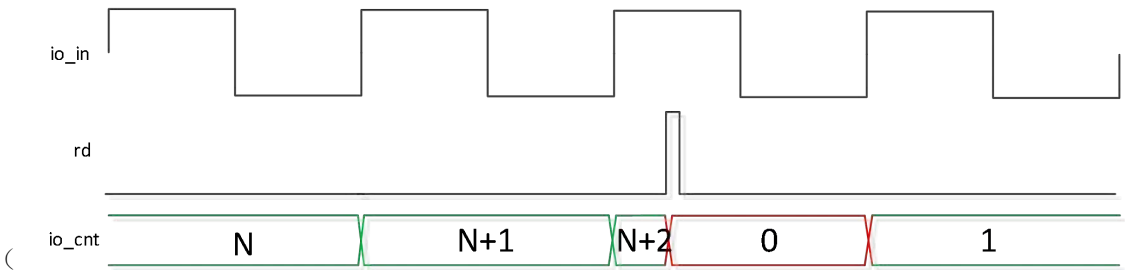


Figure 10 Zero operation after io edge (rising edge counting)

- The read operation occurs at the same time as the input signal edge, the current read is the last count value, and the current edge is accumulated to the next io_cnt, as shown in Figure 11.

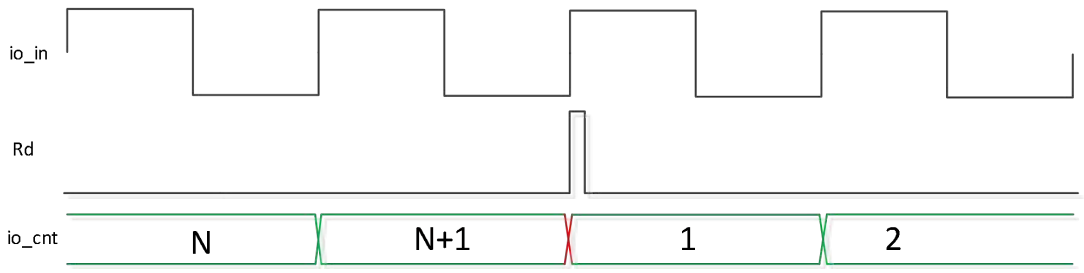


Figure 11 Zeroing operation with io edge (rising edge counting)

- Count overflow design, when io_cnt = 0xffffff and another pulse comes, count overflow, count io_cnt = 0, start counting from the beginning, and subsequent pulses come io_cnt = io_cnt + 1, as shown in Figure 12.

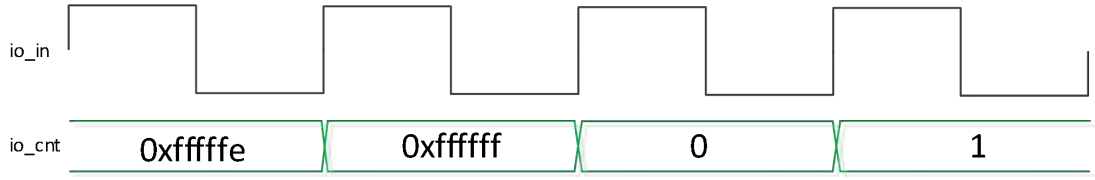


Figure 12 io_cnt overflow (rising edge count)

When the client detects a numeric overflow, the current value a, the actual current count value = a + 0xffffff + 1.

- An overflow occurs at the same time as a read, at which point the read goes to 0xffffff while the count value changes to 1. io_cnt = 1 when an overflow occurs at the same time as a read clear. as shown in Figure 13.

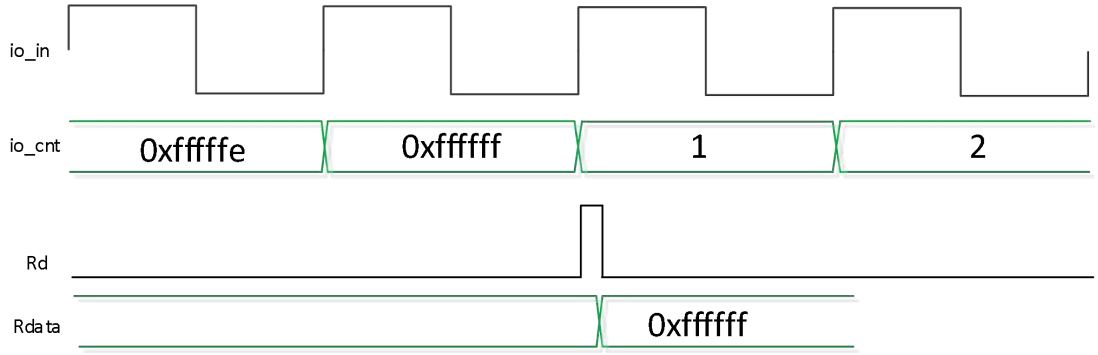


Figure 13 Overflow and read at the same time (rising edge counting)

22.5.6 Pulse division

22.5.6.1 Non-split frequency (pulse following)

- When not deviding frequencies, io_out follows io_in and is not handled
- When io_in is high for more than 80ms, io_out also does not do any special processing and io_out follows io_in.

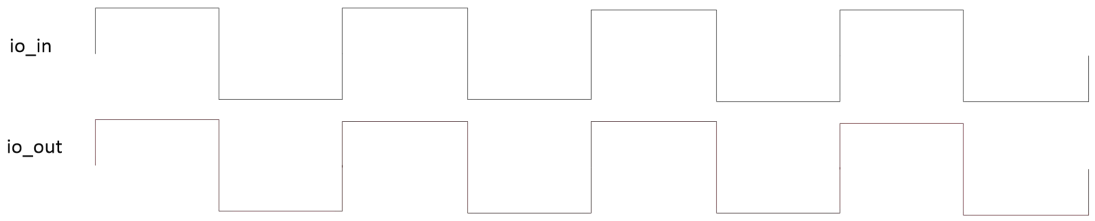


Figure 14 Equal Duty Signal

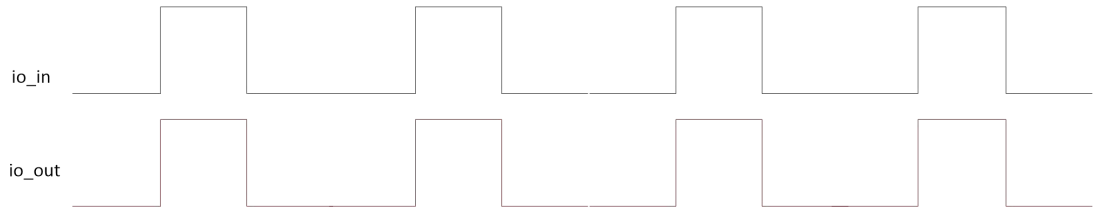


Fig. 15 Non-equivalent DUTY signals

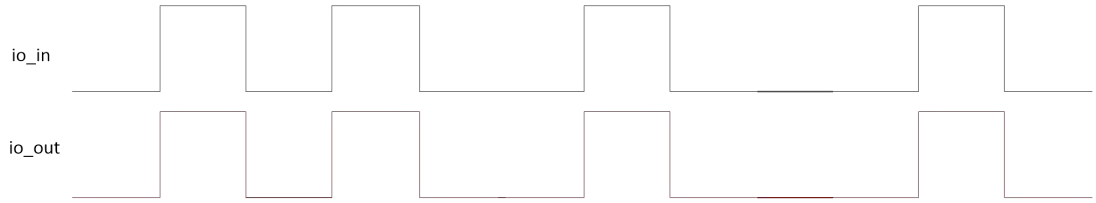


Fig. 16 Non-uniform periodic signal

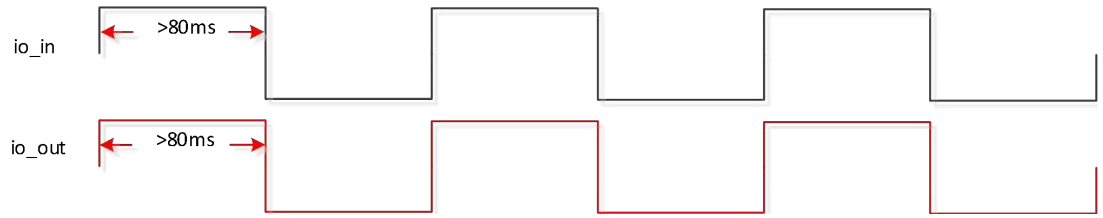


Fig. 17 Input signal pulse width greater than 80ms

22.5.6.2 Even division (io_out high level <80ms)

- io_out is the crossover frequency of io_in, crossover ratio N=n+1, n is the register crossover coefficient configuration value
- The edge alignment of io_out with io_in is determined by the edge configuration mode
- When io_in is uniformly period-distributed, io_out maintains an equal-duty waveform after an even number of divisions, as shown in Fig. 18, Fig. 19, and Fig. 20
- When io_in is a non-uniform period distribution, io_out is a non-equal duty waveform after even frequency division, as shown in Fig. 21

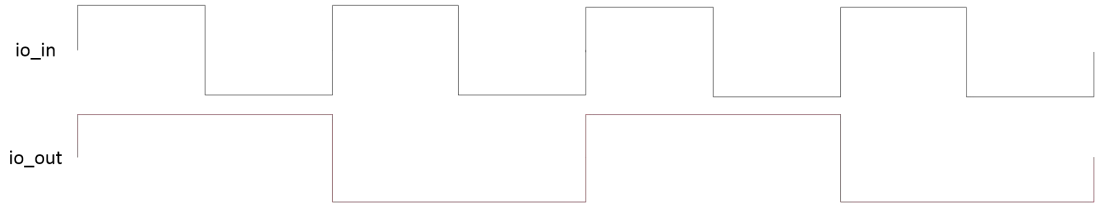


Figure 18 (n+1) crossover frequency

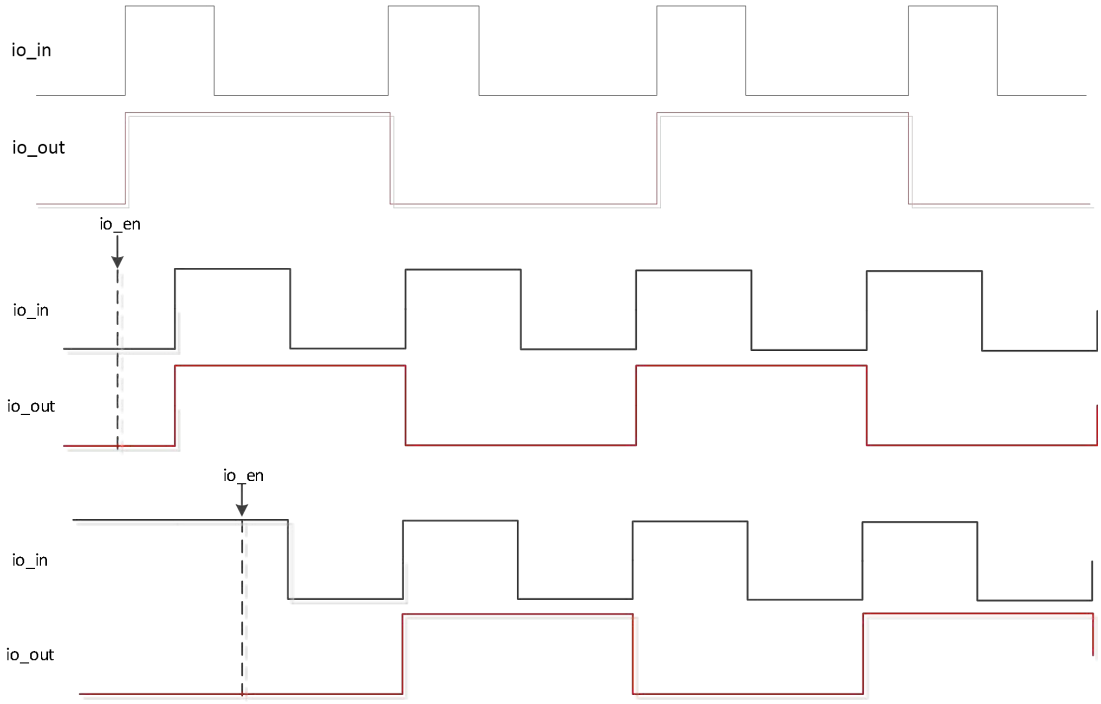


Figure 19 Rising edge alignment

The anomaly is initiated and the first output pulse is non-iso-duty.

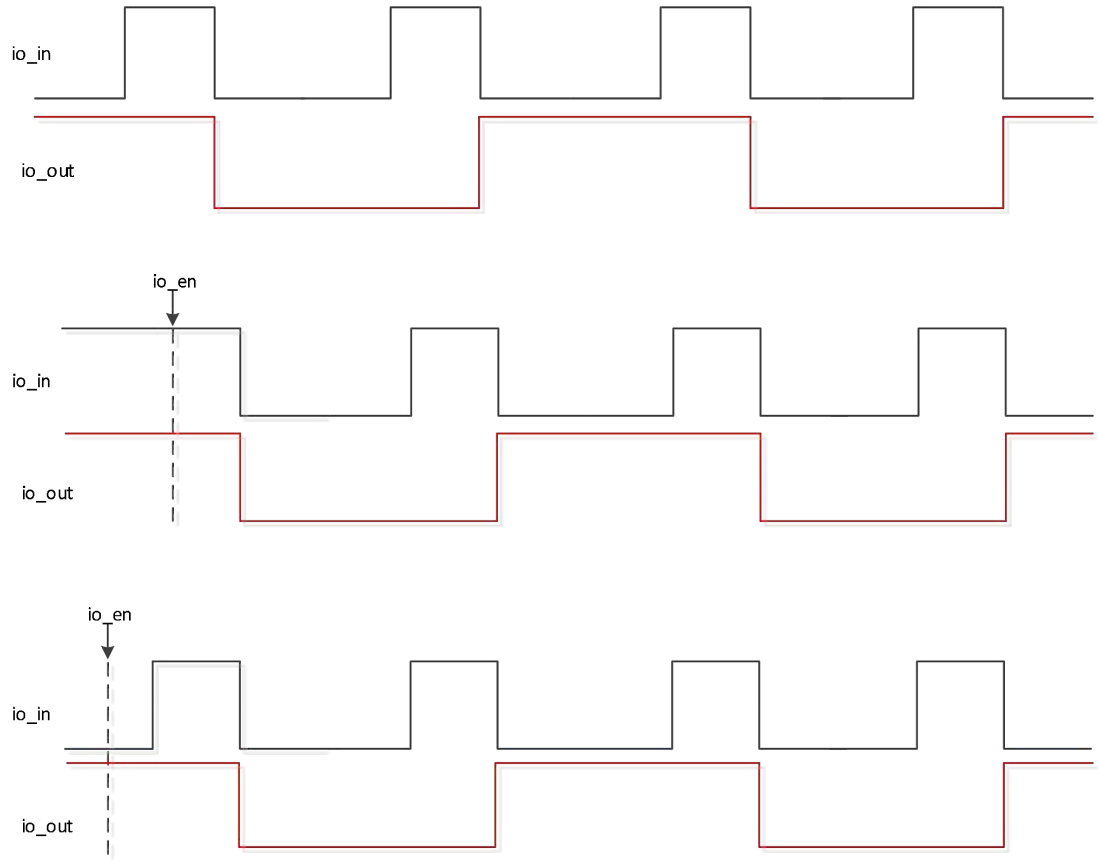


Figure 20 Falling edge alignment

The anomaly is initiated and the first output pulse is non-iso-duty.

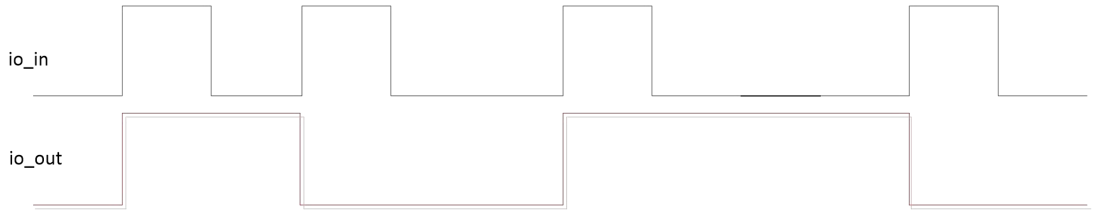


Figure 21 Non-uniform periodic frequency division

22.5.6.3 Odd division (io_out high level <80ms)

- io_out is the crossover frequency of io_in, and the crossover ratio is configured by register n+1.
- The edge alignment of io_out with io_in is determined by the edge counting mode.
- When io_in is uniformly period-distributed, io_out is a non-equal-duty waveform after odd frequency division, as shown in Fig. 22, Fig. 23.。
- When io_in is a non-uniform period distribution, io_out is a non-equal duty waveform after odd frequency division, as shown in Fig. 24.

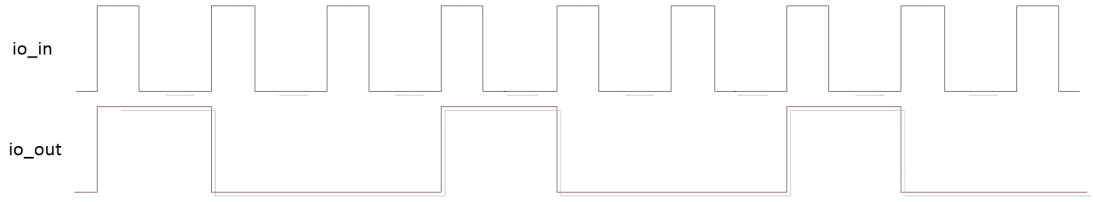


Figure 22 Rising edge alignment

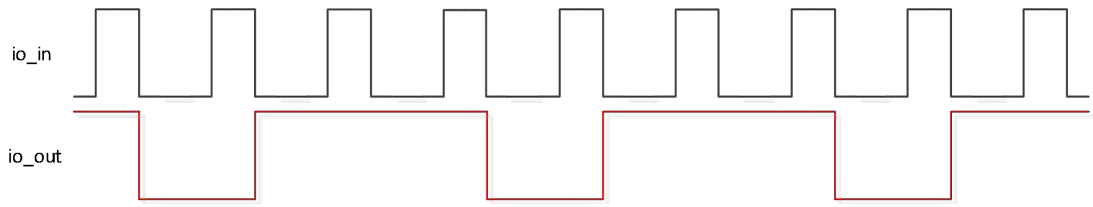


Figure 23 Falling edge alignment

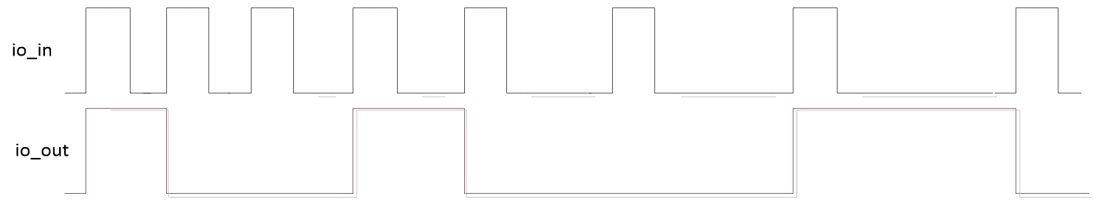


Figure 24 Non-uniform cycles

22.5.6.4 Effective level (high or low) pulse width after crossover ≥80ms

When configured for rising edge counting, the active level is high;

When configured for falling edge counting, the active level is low;

- The rising edge is counted, and after dividing the frequency when the high level pulse width is ≥80ms, the high level is pulled down, holding the high level for 80ms and the low level is held until the end of the dividing cycle.
- Conversely, the falling edge counting case is handled similarly.

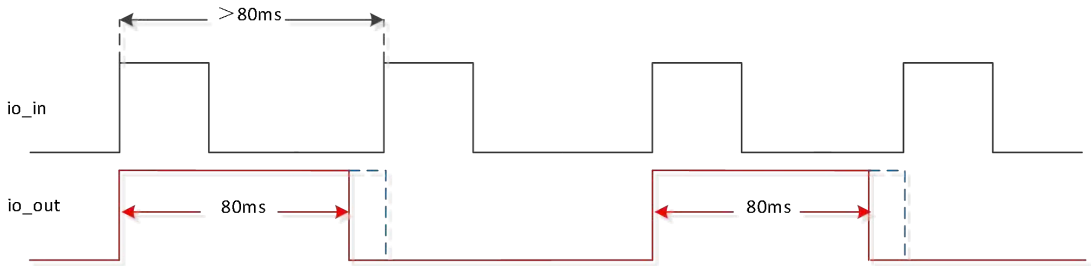


Figure 25 Non-equal duty (bifurcation)

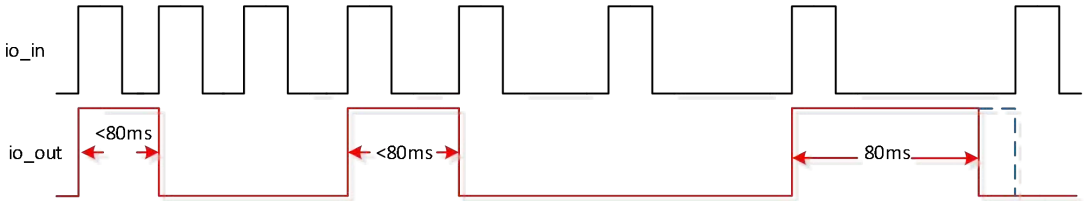


Figure 26 Non-uniform cycles (trisection)

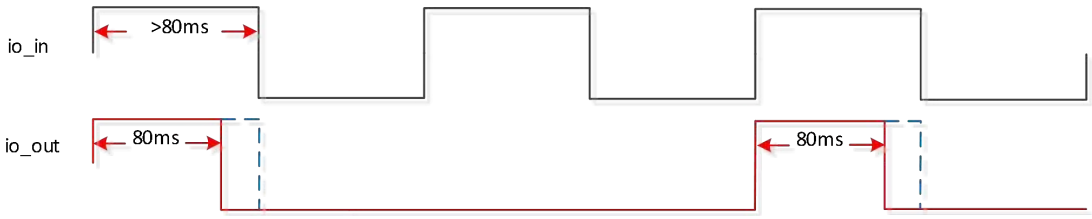


Figure 27 Input effective level greater than 80ms (dichroic)

22.5.7 Pulse level reverse output

- Supports flipping the io_out signal level before output, where io_out is the divided output.

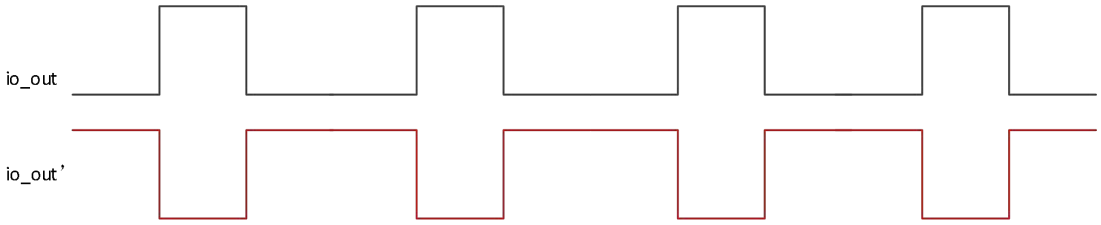


Fig. 28 Pulse level reverse output

22.6 Register description

22.6.1 Register list

Register base address of the IOCNT module

Module name	Physical address	Mapping address
IOCNT	0x4006C000	0x4006C000

Register Offset Addresses for the IOCNT Interface

Register name	Address offset	Description
IOCNT_CFG0	offset+0x0	Pulse Forwarding Configuration Register

		0
IOCNT_CFG1	Offset+0x4	Pulse Forwarding Configuration Register 1
IOCNT_CFG2	Offset+0x8	Pulse Forwarding Configuration Register 2
IOCNT_CFG3	Offset+0xC	Pulse Forwarding Configuration Register 3
IOCNT_CFG4	Offset+0x10	Pulse Forwarding Configuration Register 4
IOCNT_OUT0	Offset+0x20	Pulse forwarding output pulse counter 0
IOCNT_OUT1	Offset+0x24	Pulse forwarding output pulse counter 1
IOCNT_OUT2	Offset+0x28	Pulse forwarding output pulse counter 2
IOCNT_OUT3	Offset+0x2C	Pulse forwarding output pulse counter 3
IOCNT_OUT4	Offset+0x30	Pulse forwarding output pulse counter 4
IOCNT_CHNL	Offset+0x40	Pulse Forwarding Input Channel Selection Register
IOCNT_CTL	Offset+0x48	IOCN Pulse Forwarding Control Registers

Application Notes:

1. Modifying register configuration while module is enabled is not supported
2. Support online system clock frequency adjustment, after mode switching will clear the 80ms counter and restart counting.
3. Turning off the module enable will reset the module and clear all count values to zero.

22.6.2 IOCNT_CFG0~4（0x00~0x10）(new)

Pulse Forwarding Configuration Register 0~4

Bit	Name	Description	R/W	Reset Value
31	INT	Pulse reverse output enable: = 0: The output pulse remains in the same direction as the input pulse level; = 1: Output after reversing the output pulse.	R/W	00
30:20	CFG	Pulse crossover coefficient configuration: crossover coefficient = (CFG+1). Where CFG = 0 when no crossover, up to 2048 crossover support. Remarks: The pulse after dividing frequency is required to keep high level for 80ms, if it is faster than 80ms, then keep equal duty output; it is recommended that CFG is configured as an odd number so that it is easy to realize equal duty. Note: When enabling the UART for pulse forwarding, the crossover coefficient must be configured to be greater than or equal to 2 dividing frequencies, and the filter function must be bypassed.	R/W	00
19:0	CNT	Pulse counter that records the number of pulses before the input	R	00

		pulse is divided according to the configured trigger edge. The CNT register is cleared to zero when read and the design references the electrical energy register.		

22.6.3 IOCNT_OUT0~4（0x20~0x30）(new)

Pulse forwarding output pulse counter 0

Bit	Name	Description	R/W	Reset Value
31:20	---	reservations	R	00
19:0	CNT	Pulse counter that records the number of output pulses after pulse division according to the configured trigger edge. The CNT register is read and cleared to zero, and the design references the electrical energy register.	R	00

22.6.4 IOCNT_CHNL（0x40）(new)

Pulse Forwarding Input Channel Selection Register 0

Bit	Name	Description	R/W	Reset Value
31:30	---	reservations	R	0
29:24	IOCNT4_SEL	Same as IOCNT0_SEL	R/W	0
23:18	IOCNT3_SEL	Same as IOCNT0_SEL	R/W	0
17:12	IOCNT2_SEL	Same as IOCNT0_SEL	R/W	0
11:6	IOCNT1_SEL	Same as IOCNT0_SEL	R/W	0
5:0	IOCNT0_SEL	=0x0~0x4 : Internal input CF_OUT0~CF_OUT4 =0x5~0x9 : Internal input D2F_OUT0~D2F_OUT4 =0xA~0xF : External Interrupt Input INT1~ INT7 =0x11~0x16: Internal Input UART0_PF~UART5_PF =0x17~0x1C: Internal Inputs UART0_QF~UART5_QF =0x1D~0x22: Internal Inputs UART0_FPF~UART5_FPF = Other: Reserved Note: When enabling the UART for pulse forwarding, the dividing coefficient must be configured to be greater than or equal to 2 dividing frequencies, and the filter function must be bypassed.	R/W	0

22.6.5 IOCNT_CTL（0x48）(new)

IOCN Pulse Forwarding Control Register

Bit	Name	Description	R/W	Reset Value
31:25	FLT_CFG	IOCNT4~0 Filter Cycle Number Configuration Filter period = FLT_CFG + 1 clock period, configurable up to 128 periods Filters out only if the width is less than the filter period. If the width is greater than or equal to the filter	R/W	0x1f

		period, it will not be filtered out. For example, if FLT_CFG=3, the filter period is 4, and only waveforms with width less than 3 will be filtered out.		
24:23	--	reservations	R	0
21	FLT_BYPASS4	IOCNT4 filter function bypass enable = 0, filter enable, filter according to flt_cfg configuration =1, bypass filter function	R/W	0
20	FLT_BYPASS3	IOCNT3 filter function bypass enable = 0, filtering enabled, filtering according to flt_cfg configuration =1, bypass filter function	R/W	0
19	FLT_BYPASS2	IOCNT2 filter function bypass enable = 0, filtering enabled, filtering according to flt_cfg configuration =1, bypass filter function	R/W	0
18	FLT_BYPASS1	IOCNT1 filter function bypass enable = 0, filtering enabled, filtering according to flt_cfg configuration =1, bypass filter function	R/W	0
17	FLT_BYPASS0	IOCNT0 filter function bypass enable = 0, filtering enabled, filtering according to flt_cfg configuration =1, bypass filter function	R/W	0
16	CNT_CLR	Pulse Counter Type Configuration = 0, all pulse counters clear after reading = 1, all pulse counters are not cleared after reading	R/W	0
15:13	--	reservations	R	0
12:8	IOCNT_MODE	IOCNT4~IOCNT0 pulse counting mode selection: = 0, rising edge trigger = 1, falling edge trigger Default rising edge trigger	R/W	0
7:5	---	reservations	R	0
4:0	IOCNTx_EN	IOCNT4~IOCNT0 pulse forwarding function enable configuration: = 0, not enabled = 1, enable IOCNT	R/W	0

22.7 Usage Process

22.7.1 Internal Pulse Forwarding

To be supplemented

22.7.2 High level pulse width active

When the input signal is active high, it is recommended that the INTx hardware circuitry be externally connected

to a pull-down resistor to make the INTx default input low and use rising edge counting as follows;

1) Configure IOCNT_CTL register PXX_MODE to select rising edge counting
2) Configure the GPIO multiplexing relationship;
3) Crossover counting and level reversal can be optionally configured;
4) Configure pulse forwarding enable.

22.7.3 Low level pulse width active

When the input signal is active low, it is recommended that the INTx hardware circuit has an external pull-up resistor to make the INTx default input high and use falling edge counting as follows:

1) Configure IOCNT_CTL register PXX_MODE to select rising edge counting
2) Configure the GPIO multiplexing relationship;
3) Crossover counting and level reversal can be optionally configured;
4) Configure pulse forwarding enable.

23 Security Encryption Accelerator SEA(New)

Security Encryption Accelerator is a module that provides hardware acceleration for symmetric encryption algorithms (AES), public key cryptography algorithms (ECDSA, ECDH, etc.). Includes AES hardware acceleration unit, PKA public key algorithm gas pedal (ECC hardware acceleration unit, RSA hardware acceleration unit), hash algorithm gas pedal, 128-bit finite field multiplication unit, true random number generator.

The firmware RS-SEA based on this module is certified with the FIPS 140-3 algorithm, the list of certified algorithms is as follows, please refer to the NIST website for more details: *Cryptographic Algorithm Validation Program | CSRC (nist.gov)*.

Module	Subitem	Concrete content	Compliant with standards
AES	ECB	Key Length-128、192、256	SP800-38A
	CBC	Key Length-128、192、256	SP800-38A
	CTR	Key Length-128、192、256	SP800-38A
	CFB128	Key Length-128、192、256	SP800-38A
	OFB	Key Length-128、192、256	SP800-38A
	GMAC	Key Length-128、192、256	SP800-38D
	GCM	Key Length-128、192、256	SP800-38D
DRBG	CTR	Mode：AES-128、AES-192、AES-256	SP800-90A
HASH	SHA-1	Message Length：0~65536 increment 8	FIPS 180-4
	SHA-224	Message Length：0~65536 increment 8	FIPS 180-4
	SHA-256	Message Length：0~65536 increment 8	FIPS 180-4
	SHA-384	Message Length：0~65536 increment 8	FIPS 180-4
	SHA-512	Message Length：0~65536 increment 8	FIPS 180-4
ECDSA	KeyGen	P-192、P-224、P-256、P-384、P-521	FIPS 186-4
	KeyVer	P-192、P-224、P-256、P-384、P-521	FIPS 186-4
	SigGen	P-192、P-224、P-256、P-384、P-521	FIPS 186-4
	SigVer	P-192、P-224、P-256、P-384、P-521	FIPS 186-4

23.1 AES hardware acceleration unit

23.1.1 Characteristics

AES hardware acceleration unit can support customers to encrypt/decrypt packets with symmetric AES algorithm, and its main functions are as follows：

Support 128bit/192bit/256bit key length;

Support KeyExp key extension;

Support ECB, CBC, CTR, CFB128, OFB, GCM six data stream processing modes;

Support multiplication under GF(2^128) domain, with software can accelerate the identity authentication (GMAC) process in GCM algorithm;

23.1.2 Time consumption information

In-module hardware acceleration unit	Time consumption（Cycles）
128 bits key extension	126
192 bits key extension	141

256 bits key extension	162
128 bits encryption/decryption unit	55
192 bits encryption/decryption unit	63
256 bits encryption/decryption unit	71
128 bit finite field multiplication unit	128

Note: Time consumption refers to the number of AHB clock cycles consumed from the start of the operation to the end of the operation.

23.2 ECC hardware acceleration unit

23.2.1 Characteristics

ECC hardware acceleration unit for Elliptic Curve (EC, Elliptic Curve) computing acceleration, can significantly improve the efficiency of the implementation of elliptic curve-based encryption and decryption protocols. This module with the software can complete the elliptic curve protocols include: NIST (P), SEC (p), SEC (k), Brainpool, etc., can complete the signature authentication algorithms include: ECDSA (EC Digital Signature Algorithm), ECDH (EC Deffie-Hellman) and its variants of the algorithm.

its main functions are as follows：

Support modulo addition and modulo subtraction operations up to 521bit word length;

Support Montgomery parameter precomputation up to 521bit word length;

Support Montgomery's modulo and modulo inverse operations up to 521bit word length;

Support domain conversion from integer domain to Montgomery domain from point-add and point-doubling pre-coordinates;

Support two kinds of basic point operations from 160bit to 521bit word length, such as multiply point and add point;

Support domain conversion from Montgomery domain to integer domain at the end of point operation;

Note: Renergy provides customers with algorithm library functions based on ECC hardware acceleration, which facilitates customers to quickly realize ECDSA and other algorithm applications.

23.2.2 Time consumption information

Hardware acceleration unit	**Time consumption(Cycles)**
J parameter calculation	64
H parameter calculation	2021~24960
Montgomery modular multiplication	2151~25670
Montgomery modular reversal	6330~108764
modulo addition	21~50
modulo subtraction	21~50
point addition	7610~123982
multiplying points	7317~116492
algorithm	**Actual time consumption(consult)**
ECDSA_NIST-P256	72ms~78ms（29MHz 时钟）
ECDSA_Brainpoolp512r1	350ms~359ms（29MHz 时钟）

Note: Time consumption refers to the number of AHB clock cycles consumed from the start of the operation to the end of the operation.

23.3 RSA hardware acceleration unit

23.3.1 Characteristics

RSA hardware acceleration unit provides hardware acceleration for RSA encryption and decryption operations, which can significantly improve the efficiency of the implementation of RSA encryption and decryption protocols. This module supports RSA encryption and decryption with word lengths ranging from 32bit to 576bit.

Its main functions are as follows:

Supports RSA encryption and decryption protocol based on Euler function φ(N)=(P-1)(Q-1);

Supports modular power operations with word lengths from 32bit to 576bit;

Supports word lengths from 32bit to 2048bit for modular multiplication operations;

23.3.2 Time consumption information

hardware accelerator unit	Time Consumption（Cycles）
J parameter calculation	64
H parameter calculation	2021~24960
modular multiplication	2366~28043
modular power	2675~1010246

Note: Time consumption refers to the number of AHB clock cycles consumed from the start of the operation to the end of the operation.

23.4 HASH hardware acceleration unit

23.4.1 Characteristics

The secure hashing algorithms are categorized by the number of hash bits into: 160-bit SHA-1, 224-bit SHA-224, 256-bit SHA-256, 384-bit SHA-384, 512-bit SHA-512 and so on.

The main features of the Hash Algorithm Accelerator are as follows:

Supports SHA-1, SHA-224, SHA-256, SHA-384, SHA-512 Secure Hash Algorithm Acceleration, the actual execution of grouping and data incoming is done by the software;

Supports CPU status query and interrupt mode;

23.4.2 Time consumption information

In-module hardware acceleration unit	Time Consumption（Cycles）
SHA-1	101
SHA-224	85
SHA-256	85
SHA-384	101
SHA-512	101

Note: Time consumption refers to the number of AHB clock cycles consumed from the start of the operation to the end of the operation.

23.5 TRNG true random number generator

23.5.1 Characteristics

The True Random Number Generator uses Fiboracci ring oscillations as entropy sources to generate ns-scale

random bit streams. The features are as follows:

Support up to 29MHz system main frequency to output random number bit stream;

A random number bit stream can be output at the current system main frequency/N (1~65536);

Support random number randomness detection and error reporting function, support error correction algorithm;

Support LFSR pseudo-randomized algorithm;

Support for address interleaving randomness enhancement algorithms;

Support outputting 128bit random numbers at a time in an interrupt mode;

23.5.2 Time consumption information

Generating Data Types	Time Consumption（Cycles）
First 128 bits of data after enabling the module	209
Other groups of 128 bits data	128

Note: Time consumption refers to the number of AHB clock Cycles required to start the operation to 128bits to generate.

23.6 Software configuration process

Please refer to "Renergy Library Functions" for the firmware RS-SEA v1.0.0 of this module. Please refer to "Renergy Application Notes" for the usage process and application plan.

24 Simple Timer SIMP_TC（new）

24.1 Overview

The module integrates four 32-bit system beat counters with two operating modes：

- Single work mode；
- Cyclic work mode；

24.2 Functional Description

The SIMP_TC module is a simple 32-bit system beat counter, which uses the CPU running system clock to count and generates an overflow flag bit when the count value reaches a preset target value.

The counter supports two different modes, single and cyclic, single mode after starting the count, the count value reaches the preset target value after the counter generates an overflow flag bit and stops counting; cyclic mode after starting the count, the count value reaches the preset target value after the counter generates an overflow flag bit and starts counting from zero.

The counter starts counting after the software enables the count enable bit, stops counting after the software disables the count enable bit

24.3 Register description

SIMP_TC register base address

module name	physical address	mapping address
SIMP_TC0	0x40060000	0x40060000
SIMP_TC1	0x4006000C	0x4006000C
SIMP_TC2	0x40060018	0x40060018
SIMP_TC3	0x40060024	0x40060024

SIMP_TC offset address

Register name (x means 0/1/2/3)	address offset	description
SIMP_TCx_CTRL	0x0	SIMP _TCx control registers
SIMP_TCx_LOAD	0x4	SIMP_TCx Target Count Value Registers
SIMP_TCx_VAL	0x8	SIMP_TCx Current Count Value Register

24.3.1 SIMP_TCx control register CTRL CTRL（0x0）

Bit	Name	Description	R/W	Reset Value

31:4	Reserved	Reserved	R	0
3	IRQEN	interrupt enable bit 0: Disable interrupts 1: Enable interrupt	R/W	0
2	MODE	Count Mode Bits 0: Single count 1: Cyclic counting	R/W	0
1	OV	Count Overflow Flag Bit 0: Counter not overflowed 1: Counter overflow Note: Write 1 to clear	R/W	0
0	EN	Count Enable Bit 0: stop counting 1: Start Counting	R/W	0

24.3.2 SIMP_TCx target count value register LOAD （0x4）

Bit	Name	Description	R/W	Reset Value
31:0	LOAD	Target count value: LOAD + 1	R/W	0

24.3.3 SIMP_TCx current count value register VAL （0x8）

Bit	Name	Description	R/W	Reset Value
31:0	VAL	Counter current count value	R	0

25 Memory Handling Unit M2M（new）

The Mem2Mem module uses DMA to automatically perform data handling in SRAM to carry data from a specified source address to a destination address without CPU involvement. The minimum data granularity that can be configured for handling is 1Byte, and source and destination data valid bit configuration is also supported. This module is only available for systems with an SRAM bit width of 32bit.

25.1 Features

- Source and destination addresses are configurable, addresses are configurable Byte aligned
- Source data length is configurable, minimum unit is Byte
- Input data valid bits are configurable
- Output data valid bits are configurable
- Configurable output data is stored in Byte reverse order to the destination address
- Configurable output data is stored insaddress reverse order to the destination address
- A flag is generated when data handling is complete, and an interrupt can be configured

25.2 Functional Description

25.2.1 Input and output data valid bit width configuration

The input and output data configurations here all refer to some Bytes of data are valid per 4 Bytes of data

Support input and output data valid bit width can be configured independently through the registers for ivld[3:0] and ovld[3:0], every 4 Bytes of data, can be configured 1~4 Bytes valid.

Invalid byte of input data indicates that the corresponding byte in each 32bit of data in the source data will be discarded during data handling.

Invalid byte of output data indicates that in the target address, every 32bit of SRAM, the corresponding Byte does not carry out the storage of valid data

- When both the input and output data effective bit widths are configured as 4 Bytes, direct data shifting in SRAM can be realized；
- When the effective bit width of the input data is less than 4 Bytes, the discarding of invalid data in the input source data can be realized；
- When the effective bit width of the output data is less than 4 Bytes, the function of inserting the target data into dummy can be realized；
- Other functions can also be realized by combinations of outputs outputs；

  See later example descriptions for specific functions。

25.2.2 The dummy value can be assigned when the output address is invalid

This can be achieved by register configuration, filling in the configured register value when a bit of the output address is invalid. By default, no write operation is performed on invalid addresses.

Source data length ilen, source data effective bitwidth ivld, target data effective bitwidth ovld. there is a possibility that ilen*ivld/ovld is not an integer, and the application is defined as non-conventional. It is handled as follows:

（1）If DUMMY_EN=0, the valid byte is written to the corresponding valid data, and the extra byte is not written;

（2）If DUMMY_EN=1, the valid byte is written to the corresponding valid data, and the extra byte is written to the dummy value.

25.2.3 Output data placed in reverse order

Configuration register M2M_MODE.ORV_EN=1 enables output Word data reverse order. This reverse order function is determined only according to the bit width of the output Word data, for example, if the bit width of the output Word data byte is 3Bytes, then each time 3 Bytes of data (A0, A1, A2) of the source data are fetched, the reverse order arrangement is carried out once (A2, A1, A0), and then stored into the SRAM.

25.2.4 Configurable source and destination addresses, configurable input data lengths

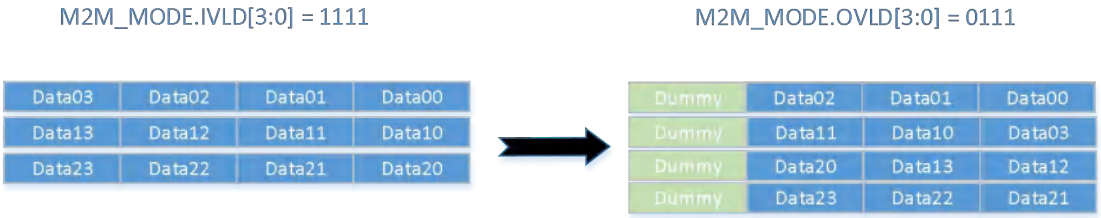
The source data address and destination data address are configured through registers, and the configuration aligned by Word is supported. Meanwhile, the input data length can be configured through registers with a minimum scale of Word. the output data length is self-adaptive according to the input/output length and the valid bits of input/output data

25.2.5 Data in reverse address order

Configure the register as addr_rven=1 to enable the output data to realize address reverse order placement. For example, if 4 Bytes of source data (A3, A2, A1, A0) are fetched, (A3, A2, A1, A0) will be written to the destination address, after which the destination address will be reduced by 4, and the next 4 Bytes of the fetched source data will be stored, and so on, until the last Byte is stored.

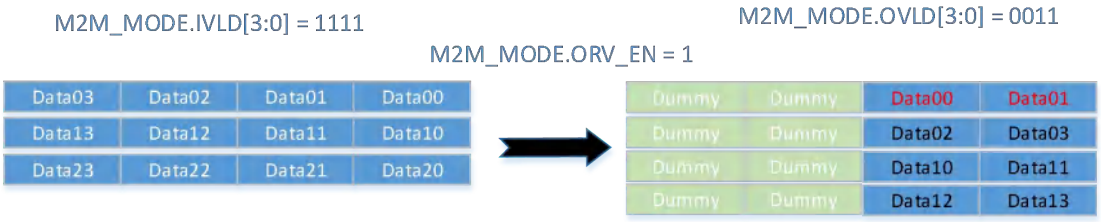
25.3 Examples

25.3.1 Input data 4Bytes valid, output 3Bytes valid



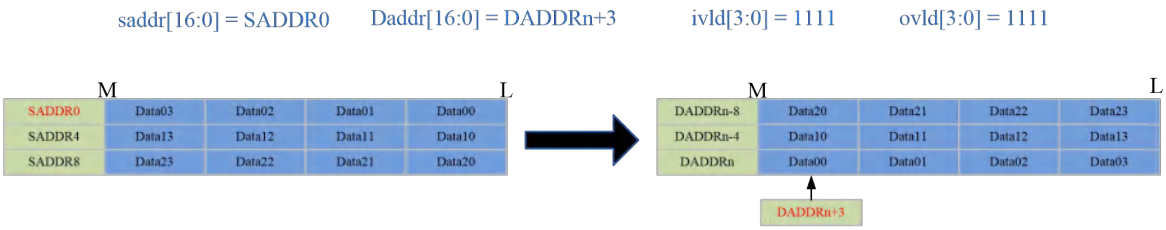
25.3.2 Input data 2Bytes valid, output 4Bytes valid

25.3.3 Input data is stored in reverse order byte (input 4Bytes valid, output 2Bytes valid)



As you can see from the above figure, the output address is discharged in reverse order with the input address; Data00 is placed at the lowest address of a Word in the source address, and in the destination address, Data00 is placed at the highest address of a Word.

25.3.4 Output data in reverse address order



As you can see from the above figure, first take the data (data03, data02, data01, data00) from SADDR0, write it to the address DADDRn+3, write it from the high address to the low address by byte, and according to the output of the valid ovald, store the next data until the last byte.

The SADDR address and DADDR address are aligned according to Byte, and the input and output validity and length can be configured arbitrarily.

25.4 Handling speed

The fastest you can do is 6 cycles to complete the data handling of a Word. The actual speed is also related to the configured M2M_MODE.IVLD and OVLD, as well as the SRAM contention.

25.5 Register description

module name	physical address	mapping address
M2M	0x4006_8000	0x4006_8000

M2M module register offset address

name	address offset	R/W	reset value	descriptive
M2M_MODE	0x00	R/W	0xFF	M2M Mode Configuration Register
M2M_CTL	0x04	R/W	0x0	M2M Control Register
M2M_DUMMY	0x08	R/W	0x0	M2M Invalid Address DUMMY Value Configuration Registers
M2M_SADDR	0x0C	R/W	0x0	M2M source data address configuration registers
M2M_DADDR	0x10	R/W	0x0	M2M target data address configuration registers
M2M_ILEN	0x14	R/W	0x0	M2M source data length configuration registers
M2M_IE	0x18	R/W	0x0	M2M Interrupt Enable Register
M2M_IF	0x1C	R/W	0x0	M2M Interrupt Flag Register

The above registers do not support bitband operations。

25.5.1 M2M_MODE（0x0）

M2M Mode Configuration Register， Address: 0x4006_8000; Default Value: 0xFF；

Bit	Name	Description	R/W	Reset Value
31:11	Reserved	Reserved	RO	0
10	ADDR_RVEN	Data is sorted in reverse order by Word address = 0: not in reverse order = 1: reverse order by Word address	RW	0
9	DUMMY_EN	=0: Invalid byte location in the destination address, no write operation; =1: Invalid byte location in the destination address, write dummy value;	RW	0
8	ORV_EN	Output Word data placed in reverse order byte. = 0: not in reverse order = 1: reverse order	RW	0
7:4	OVLD	Output Word data valid byte configuration = 0: Byte not valid = 1: Byte valid The corresponding Byte is 0, indicating that the dummy value is written when the address of this Byte in the destination address is invalid or M2M_MODE.DUMMY_EN is valid.	RW	0xf
3:0	IVLD	Input Word Data Valid Byte Configuration = 0: Byte not valid = 1: Byte valid The 4-bit configuration corresponds by Byte to each Byte in each Word data, and a high level indicates that the corresponding Byte is valid.	RW	0xf

25.5.2 M2M_CTL（0x4）

M2M control register, address: 0x4006_8004; default value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	Reserved	RO	0
0	M2M_EN	= 0: No action =1: Starts data handling. The specified length is automatically cleared after data handling is completed. When this bit is 1, writing 0 terminates the current handling process.	RW	0

25.5.3 M2M_DUMMY（0x8）

M2M Invalid Address DUMMY Value Configuration Register, Address: 0x4006_8008; Default Value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:0	DUMMY	This register is valid when M2M_MODE.DUMMY_	RW	0

		EN=1. This 32bit value corresponds by Byte to the Byte of the M2M_MODE.OVLD configuration invalid address.		

25.5.4 M2M_SADDR（0xC）

M2M Source Data Address Configuration Register, address: 0x4006_800C; default value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	SADDR	Source data address, aligned in Byte. The address here is the SRAM offset address, the source data address + source data length must not exceed the SRAM address range	RW	0

25.5.5 M2M_DADDR（0x10）

M2M Target Data Address Configuration Register, Address: 0x4006_8010; Default Value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	DADDR	Target data address, aligned in Byte. The address here is the SRAM offset address, the target data address + target data length must not exceed the SRAM address range	RW	0

25.5.6 M2M_ILEN（0x14）

M2M Source Data Length Configuration Register, Address: 0x4006_8014; Default Value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	ILEN	Input data length configuration, aligned by Word The source data length cannot exceed the size of the SRAM. Application Note: It is not allowed to enable M2M at ILEN=0.	RW	0

25.5.7 M2M_IE（0x18）

M2M Interrupt Enable Register, Address: 0x4006_8018; Default Value: 0x0；

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	Reserved	RO	0
0	DONE_IE	Handling completion interrupt enable = 0: Disable interrupt = 1: Enable interrupt	RW	0

25.5.8 M2M_IF（0x1C）

M2M Interrupt Flag Register, Address: 0x4006_801C; Default Value: 0x0；

Bit	Name	Description	R/W	Reset Value

31:1	Reserved	Reserved	RO	0
0	DONE	Handling complete sign, write 1 to clear = 0: Removal not completed = 1: Removal completed This bit is automatically cleared each time M2M_CTL is configured with M2M_EN=1.	RW1C	0

25.6 Software Usage Flow

1) Configure the source data start address M2M_SADDR;
2) Configure the target data start address M2M_DADDR;
3) Configure the source data length M2M_ILEN;
4) Configuration mode register M2M_MODE;
5) Configure interrupt enable M2M_IE;
6) Configure to start M2M_CTL;
7) Wait for an interrupt or flag, read data from the target address, and clear the flag;

26 DSP Core

This module is a DSP module for data signal processing, including operations such as FFT computation in floating-point format, arithmetic units for conversion between integers and floating-point numbers, basic arithmetic units for floating-point operations, Cordic algorithm for computing sine, cosine, and root-mean-square, IIR acceleration operation, FIR acceleration operation, linear interpolation operation, and Lagrange interpolation operation.

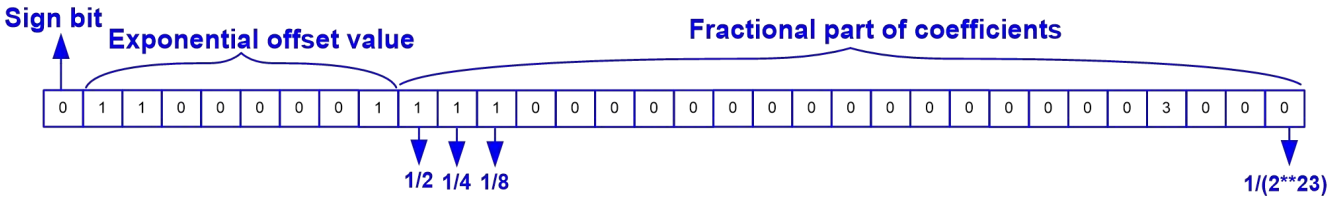
The floating-point numbers referred to here are all single-precision floating-point numbers, with 23 bits of effective digits after the decimal point (in binary).

26.1 Features

- Support conversion between integers and floating-point numbers
- Support floating-point addition, subtraction, multiplication, and division.
- Support single butterfly operation (for complex numbers) and continuous butterfly operation with DMA.
- Support the entire process of radix-2 FFT, with point numbers of 64, 128, 256, 512, and 1024.
- Support automatic data movement operation for bit-reversal, with point numbers of 4, 8, 16, 32, 64, 128, 256, 512, and 1024.
- Support sine and cosine calculation.
- Support root-mean-square calculation.
- Support arctangent calculation.
- Support single IIR calculation and IIR calculation with DMA.
- Support FIR filtering operation.
- Support linear interpolation.
- Support Lagrange interpolation.

26.2 Basic Principles of Calculation Engine

26.2.1 Single-Precision Floating-Point Numbers



The figure above shows the representation method of floating-point numbers. The numeric value of a floating-point number is expressed as $\pm 2^{n}(1+f)$, where n represents the exponent value and f represents the fractional part.

The sign bit represents the positive or negative value of the floating-point number, with 0 representing a positive integer and 1 representing a negative number.

The exponent part is represented using a biased notation, with the highest bit of the 8-bit “exponent bias value” representing the exponent sign and the low 7 bits representing the actual exponent value. For example, the exponent value of 1 represented in biased notation is 1+127=128; the exponent value of -10 represented in biased notation is -10+127=117.

The fractional part of coefficient represents the numbers after the decimal point.

26.2.2 Special Value

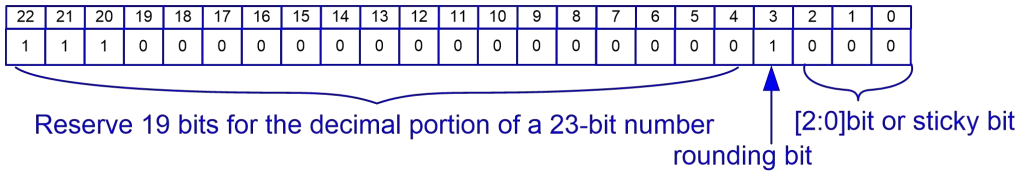
Type	Sign Bit(1bit)	Exponent Bias Value (8bit)	Fractional Part of Coefficient (23bit)
0	0/1	0	0
Denormal	0/1	0	Non-zero
Infinity	0/1	255	0
NaN	0/1	255	Non-zero
Normal	0/1	1~254	Any

The table above lists some special values in floating-point number representation. When performing floating-point arithmetic, it is necessary to check whether the input and output data are special values, perform special processing, and provide flags accordingly.

26.2.3 Floating-Point Rounding

When the bit width of the coefficient decimal part in floating-point arithmetic is greater than the actual representable bit width, rounding is needed to process the data.

First, the following concepts are defined:



For truncating m-bit data to n bits as shown in the figure above:

- rounding bit:Starting from the leftmost highest bit, it is the (n+1)th bit;
- Stick bit: Starting from the leftmost highest bit, all bits starting from the (n+2)th lowest bit.

26.2.4 IEEE 754 Standard Rounding Modes

The IEEE 754 standard specifies four rounding modes:

1. Nearest: Round to nearest, rounding bit=1 and non-zero bits in the sticky bit cause rounding up.
2. +∞ : For positive numbers, rounding bit=1 or non-zero bits in the sticky bit cause rounding up, and no rounding is done for other numbers.
3. -∞ : For negative numbers, rounding bit=1 or non-zero bits in the sticky bit cause rounding up, and no rounding is done for other numbers.
4. Zero: Rounding bit and sticky bit are directly discarded.

26.2.5 Rounding modes of this chip

This chip supports six rounding modes that can be selected based on the configuration:

1. When the configuration is rnd=000, it rounds to the nearest value.
2. When the configuration is rnd=001, it rounds to zero.
3. When the configuration is rnd=010, it rounds up towards positive infinity.
4. When the configuration is rnd=011, it rounds up towards negative infinity.
5. When the configuration is rnd=100, it rounds up.
6. When the configuration is rnd=101, it rounds to nearest and ties away from zero.

26.2.6 Integer to Floating-Point Conversion

Below is a brief explanation of the idea and principle behind integer to floating-point conversion:

Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**
Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**1**

1. Sign bit:
   a) The highest bit is the sign bit for the floating-point number: fp_sign = bit(31);
   b) If the original data is negative, it needs to be converted to two's complement before the next step.
2. Exponent:
   a) Starting from the highest bit, look for the first "1" and record its position as n. The exponent value is n (27 in the table above).
   b) According to the encoding rules, the exponent is represented as fp_exp=n+127;
3. Mantissa:
   a) If n>23, take 24 bits starting from the (n-1)th bit, and round the remaining bits in the original data to determine the lowest bit of m. m is the mantissa.
   b) If n=23, take 24 bits starting from the (n-1)th bit directly as the mantissa.
   c) If n<23, take all the remaining bits starting from the (n-1)th bit, padding zeros to the low bits, as the mantissa.

26.2.7 Converting Floating-Point Numbers to Integers

1. Check whether the original data is a special number (0, NaN, $\pm\infty$);
2. Determine whether the conversion result overflows based on the exponent part e of the original data. If the exponent part e > 32+127, the conversion result overflows. Otherwise, proceed to the next step;
3. Take out the 23-bit decimal part m, add a leading 1 to the highest bit to form a 24-bit decimal m;
4. Shift the decimal m left by e bits, pad the highest (32-e) bits with 0s and the lowest e bits with 0s, resulting in 56 bits of data;
5. Right shift the result by 24 bits to obtain the final result.

26.2.8 Floating-Point Multiplication

1. Multiplication of special data:
   a) NaN multiplied by any number is NaN.
   b) 0 multiplied by infinity is NaN.
   c) 0 multiplied by any other number is 0.
2. Multiplication of normal data:
   a) The sign bit of the result is obtained by XOR-ing the sign bits of the two operands.
   b) The exponent part of the result is obtained by adding the exponent parts of the two operands and subtracting 127($e = e_0 + e_1 - 127$).
   c) The mantissa part of the result is obtained by multiplying the two mantissa parts (expanded to 24 bits each), resulting in a 48-bit data m. The result is checked for overflow. If overflow occurs, the exponent e is increased by 1. The exponent e is then checked for overflow. In either case, m is shifted right by 3

bits. If no overflow occurs, m is shifted right by 2 bits. The high 23 bits of m are taken as the mantissa of the result.

3. Overflow processing supports the 4 overflow handling modes specified in IEEE754, which can be configured through registers.

26.2.9 Floating-Point Addition

1. Checking for Special Numbers: If either operand is NaN, the result is NaN.
2. Normal Numbers:
   a) The sign bit of the result is determined by the sign bit of the operand with the larger absolute value.
   b) The exponents of the operands are compared. The difference in exponents, F, is calculated by subtracting the smaller exponent e_1 from the larger exponent e_0.
   c) The mantissa of the operand with the smaller exponent is shifted right by F bits. Then, the mantissas of both operands are expanded by one bit and added together.
   d) The exponent of the result is equal to e_0 if there is no overflow. If overflow occurs, the exponent is increased by 1, $e = e_0 + 1$.
   e) The mantissa of the result is obtained by adding the mantissas of the operands. The higher 2 bits of the resulting mantissa are discarded. If overflow occurs, the result is shifted right by 1 bit (equivalent to dividing by 2). The resulting mantissa is the final result.

26.2.10 Butterfly Operation

$$X_1'(k) = X_1(k) + W_N^k X_2(k)$$

$$X_2'(k) = X_1(k) - W_N^k X_2(k)$$

Where $X_1(k)$、$X_2(k)$ are inputs, $X_1'(k)$、$X_2'(k)$ are the outputs of the butterfly operation.

If the original data is complex, then we have:

$$X_1(k) = X_{1r}(k) + jX_{1i}(k)$$

$$X_2(k) = X_{2r}(k) + jX_{2i}(k)$$

$$W_N^k = W_{Nr}^k + jW_{Ni}^k$$

$$X_1'(k) = X_{1r}'(k) + jX_{1i}'$$

Therefore, we can obtain:

$$X_1'(k) = X_1(k) + W_N^k X_2(k)$$

$$= (X_{1r}(k) + jX_{1i}(k)) + (W_{Nr}^k + jW_{Ni}^k) * (X_{2r}(k) + jX_{2i}(k))$$

Extracting the real and imaginary parts, we obtain:

$$X'_{1r} = X_{1r} + W^k_{Nr}X_{2r} + W^k_{Ni}X_{2i}$$

$$X'_{1i} = X_{1i} + W^k_{Nr}X_{2i} - W^k_{Ni}X_{2r}$$

Similarly,

$$X'_{2r} = X_{1r} - W^k_{Nr}X_{2r} - W^k_{Ni}X_{2i}$$

$$X'_{2i} = X_{1i} - W^k_{Nr}X_{2i} + W^k_{Ni}X_{2r}$$

26.2.11 IIR Filter

IIR (infinite impulse response) filter is the most common type of linear digital filter. Its output at a given time depends on both its input and previously computed input values.

IIR filter is recursive because the difference equation involves feedback. As a result, its stability time is longer than that of FIR filters, and the impulse response may have infinite width. Therefore, it is important to consider the stability of the filter.

The transfer function of IIR filter in z-domain is as follows:

$$H(z) = \frac{\sum_{k=0}^{M} b_k z^{-k}}{a_0 + \sum_{k=1}^{N} a_k z^{-k}} = \frac{Y(z)}{X(z)}$$

The time-domain calculation formula (direct form I) of IIR filter is as follows:

$$y[n] = \sum_{k=0}^{M} b_k x[n-k] - \sum_{k=1}^{N} a_k y[n-k]$$

For a second-order IIR filter, where both M and N are 2 in the above equation, it is commonly designed with a_0 feedback coefficient of 1. Therefore, the above equation can be simplified as:

$$y[n] = b_0 \times x(n) + b_1 \times x(n-1) + b_2 \times x(n-2) - a_1 \times y(n-1) - a_2 \times y(n-2)$$

Where x(n) is the current input data, x(n-1) is the previous input data (one unit delayed in time), and x(n-2) is the input data from two units ago (two units delayed in time); y(n) is the current output data, y(n-1) is the previous output data (one unit delayed in time), and y(n-2) is the output data from two units ago (two units delayed in time).

26.2.12 FIR Filters

FIR (Finite Impulse Response) filters are also known as finite-length unit-impulse response filters and are a type of non-recursive filter. FIR filters with constant coefficients are a type of LTI (linear and time-invariant) digital filter. The finite impulse response signifies that there is no feedback in the filter. The relationship between the output of an FIR filter with a length of N and an input time series x[n] is given by a finite convolution sum, which has the following form:

$$y[n] = \sum_{k=0}^{N} a[k] * x[n-k]$$

In the above equation, a[k] represents the filter coefficients, and x[n-k] denotes a delayed version of x[n] by k cycles.

Figure of Direct-Form FIR Filter:

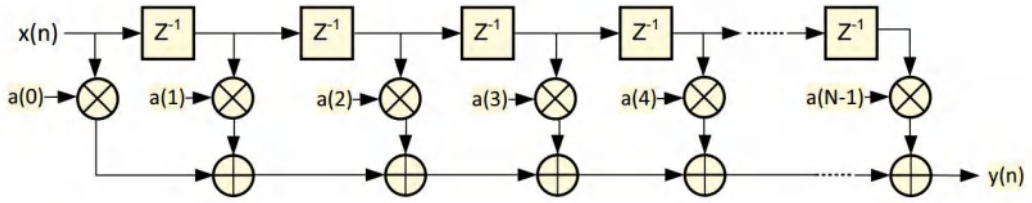


Figure 1-1: **Conventional Tapped Delay Line FIR Filter Representation**

The above equation represents an N-1 order FIR filter with N taps (coefficients). This filter is composed of N multipliers and N-1 accumulators. The input signal is time-varying, and the output of the FIR filter is the sum of the weighted (coefficients) inputs at each moment in time.

For example, a 4th order FIR filter has 5 coefficients. When implemented using a serial method, 5 multipliers and 4 adders are required for one calculation:

y[n] = a0*x[n] + a1*x[n-1] + a2*x[n-2]+ a3*x[n-3]+ a4*x[n-4]

26.2.13 Linear Interpolation

Given n points: $(1, y_1), \ldots, (n, y_n)$, find y(i) for x as the i-th output data abscissa.

Formula: ,[x]=x (round down)

Calculate the output data point by point, with the interpolation position increasing by step in each loop:

```
for i=1:1:out_len
    n=floor(t);
    y[i]= x[n]+ (t-n) * (x[n+1]-x[n]);
    t=t+step;
End
```

26.2.14 Lagrange Interpolation

Given n points: $(1, y_1), \ldots, (n, y_n)$, find y(i) for x as the i-th output data abscissa.

3-point Lagrange interpolation, which utilizes a quadratic function for each small interval.

Formula:

$$cur = round(x);$$

$$y(i) = \frac{x - cur}{2} * \left[(x - (cur + 1)) * y_{cur-1} + (x - (cur - 1) * y_{cur+1} \right] - (x - (cur - 1)) * (x - (cur + 1)) * y_{cur}$$

Calculate the output data point by point, with the interpolation position increasing by step in each loop:

```
for i=1:1:out_len
    n=floor(t);
    y[i]=(t-n)*0.5*((t-n-1)*x[n-1]+(t-n+1)*x[n+1]) - (t-n+1)*(t-n-1)*x[n]
```

t=t+step;

End

26.3 Arithmetic instruction

26.3.1 Integer to Floating Point (int2fp/int2fp_dma)

26.3.1.1 Single Data Conversion

Integer to Floating Point

This mode converts 32-bit (or 24-bit) signed integers input from the register into 32-bit single-precision floating-point format, and outputs to the register which can be read by the CPU.

Normalization processing can be applied to the converted floating-point number by dividing it by 2^n, where n can be configured from 0 to 32. If it is configured as 0, it means no normalization.

By default, the input data register is set up to receive a 32-bit signed integer as input, but for special applications, if the input integer is a 24-bit signed number, MAC_CTL0[28] needs to be configured as 1 and this mode needs to be selected.

Software configuration process:

1) Set MAC_CTL0[0] =1 to select the integer-to-floating-point single-point mode;
2) Set MAC_CTL0[16:14] to select the floating-point rounding mode;
3) Configure MAC_CTL0[21:17] to select the normalization level;
4) For 24-bit input data, set MAC_CTL[0] = 1;
5) Write the raw integer to be converted to register MAC_IN0;
6) Read register MAC_OUT0 to obtain the converted floating-point value.

Once the software has configured the mode, conversion is carried out by writing data to the MAC_IN0 register. The calculation result is then saved to the MAC_OUT0 register, so conversion results can be obtained simply by reading the result register after setting the original integer value.

Note that if the software requires continuous conversion, the above mode configuration needs to be executed only once. Before switching modes, each time just write the value to MAC_IN0, and conversion will be executed automatically.

26.3.1.2 Continuous Conversion of Multiple Data

This mode supports converting a whole section of integers in SRAM into floating-point numbers and writing the results back to SRAM. It should be noted that the raw data stored in SRAM are signed integers (either 32-bit signed integers or 24-bit signed integers). For special applications where a 24-bit integer takes up 4 bytes, with the valid data stored in the low 3-byte position and the highest byte being invalid, MAC_CTL [0] needs to be configured as 1.

The target address can be configured to be the same as the source data address, which will overwrite the original data after the conversion, saving SRAM space. Alternatively, if the target address is configured to be different from the source data address, the converted data will be written to another area in SRAM.

Software configuration process:

1) Configure register MAC_CTL0[1]=1 to select the integer-to-floating-point DMA mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode for the floating-point numbers;
3) Configure MAC_CTL0[21:17] to select the normalization level;
4) Configure register DMA_SRBADR to select the source data DMA start address;
5) Configure register DMA_TRBADR to select the target data DMA start address;
6) Configure register DMA_LEN to select the DMA length;
7) Set MAC_CTL1[0]=1 to initiate the conversion;
8) Wait for the flag bit MAC_FLG[3] to be set to 1, and the CPU can obtain the converted results from SRAM;

After converting the specified length of data, a completion flag will be generated. If the interrupt enable signal is configured, a completion interrupt will be generated. The software needs to clear the flag bit in the interrupt.

26.3.2 Floating-Point to Integer Conversion (fp2int/fp2int_dma)

26.3.2.1 Single Data Conversion

Floating to Integer Point

This mode converts a 32-bit floating-point number input from a register to a 32-bit signed integer format, outputs it to a register, and can be read by the CPU. It supports scaling the floating-point number by 2^n before conversion. Here, n can be configured from 0 to 32, and when it is configured as 0, it means not to scale.

Software configuration process:

1) Configure register MAC_CTL0 [2] =1 to select floating-point to integer single point mode.
2) Configure register MAC_CTL0[16:14] to select the rounding mode for the floating-point number
3) If you need to scale the floating-point number before conversion, configure MAC_CTL0[26:24]=n
4) Write the original floating-point number to be converted to register MAC_IN0.
5) Read register MAC_OUT0 to obtain the converted integer value.

After the software configures the mode, the conversion will start as soon as the MAC_IN0 register is configured. The result of the conversion is saved to register MAC_OUT0. Therefore, once the original value is configured, the converted result can be obtained by reading the result register directly.

Note that if the software needs to perform multiple consecutive conversions, the above mode configuration only needs to be executed once. Before switching modes, as long as MAC_IN0 register is written, the conversion will be executed.

26.3.2.2 Continuous Conversion of Multiple Data

This mode supports converting a whole section of floating-point numbers in SRAM into integers, with the result being written back into SRAM. The target address can be configured to be the same as the source data address, which will overwrite the original data after the conversion to save SRAM space. Otherwise, configuring the target address to be different from the source data address will write the converted data into another area of SRAM.

Software configuration process:

1) Configure register MAC_CTL0[3]=1 to select the floating-point to integer DMA mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode of the floating-point number;
3) If it is necessary to amplify the floating-point number before conversion, configure MAC_CTL0[26:24]=n;
4) Configure register DMA_SRBADR to select the source data DMA starting address;
5) Configure register DMA_TRBADR to select the target data DMA starting address;
6) Configure register DMA_LEN to select the DMA length;
7) Configure register MAC_CTL1[0]=1 to start the conversion;
8) Wait for the flag bit MAC_FLG [4], and the CPU can obtain the converted result from SRAM.

After converting the specified length of data, a completion flag will be generated, and if the interrupt enable signal is configured, a completion interrupt will be generated. The software needs to clear the flag bit in the interrupt.

26.3.3 Floating-Point Multiplication (fp_mult)

Floating-Point Multiplication

This mode performs a floating-point multiplication on the data in input registers MAC_IN0 and MAC_IN1. Four modes are supported for input and output data formats:

1) Input integer, output integer
2) Input integer, output floating-point number
3) Input floating-point number, output integer
4) Input floating-point number, output floating-point number

If the input is an integer, the hardware will first convert the integer to a floating-point format before performing the floating-point multiplication. The operation produces a floating-point format product. If the output format is chosen as integer, the hardware will convert the floating-point format product to integer format.

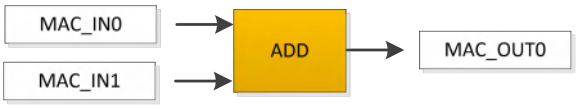
Software configuration process:

1) Configure register MAC_CTL0[4]=1 to select the floating-point multiplication mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode of the floating-point number;
3) Configure register MAC_CTL0[13:12] to select the input and output data mode;
4) Configure registers MAC_IN0 and MAC_IN1 (multiplicand and multiplier);
5) Wait for the flag bit MAC_FLG[9]=1, indicating that multiplication is complete;
6) Read register MAC_OUT0 to obtain the product.

In this mode, each time the MAC_IN1 register is configured, the multiplication operation is automatically started. Therefore, the software should first configure the MAC_IN0 register and then configure the MAC_IN1 register. Additionally, each time the MAC_IN1 register is configured, the flag bit of the previous operation is automatically cleared until the current calculation is complete, and the flag bit is set again.

Since input and output data formats are different, data conversion is necessary, so the time required for each floating-point multiplication operation depends on the selected mode.

26.3.4 Floating-Point Addition (fp_add)



Floating-Point Addition

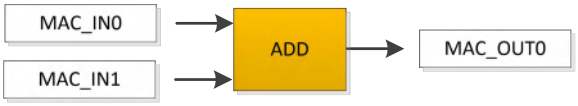
This mode performs a floating-point addition on the data in input registers MAC_IN0 and MAC_IN1. The data format of both input registers must be in floating-point format, and the output result is also in floating-point format.

Software configuration process:

1) Configure register MAC_CTL0[5]=1 to select the floating-point addition mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode of the floating-point number;
3) Configure registers MAC_IN0 and MAC_IN1 (addend and augend);
4) Read register MAC_OUT0 to obtain the sum.

In this mode, every time the MAC_IN1 register is configured, the addition operation is automatically started. Therefore, the software should first configure the MAC_IN0 register and then configure the MAC_IN1 register.

26.3.5 Floating-Point Subtraction (fp_sub)



Floating-Point Subtraction

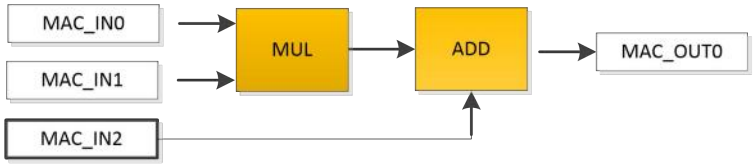
This mode performs a floating-point subtraction on the data in input registers MAC_IN0 and MAC_IN1. The data format of both input registers must be in floating-point format, and the output result is also in floating-point format.

Software configuration process:

1) Configure register MAC_CTL0[6]=1 to select the floating-point subtraction mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode of the floating-point number;
3) Configure registers MAC_IN0 and MAC_IN1 (minuend and subtrahend);
4) Read register MAC_OUT0 to obtain the difference.

In this mode, every time the MAC_IN1 register is configured, the subtraction operation is automatically started. Therefore, the software should first configure the MAC_IN0 register and then configure the MAC_IN1 register.

26.3.6 Floating-point Multiply-Addition Operation (fp_mlad)



Floating-point Multiply-Addition Operation

This mode performs a floating-point multiplication on the data in input registers MAC_IN0 and MAC_IN1, followed by addition with MAC_IN2. The resulting output is stored in MAC_OUT0. The input data format for the input registers must be in floating-point format, and the output result is also in floating-point format.

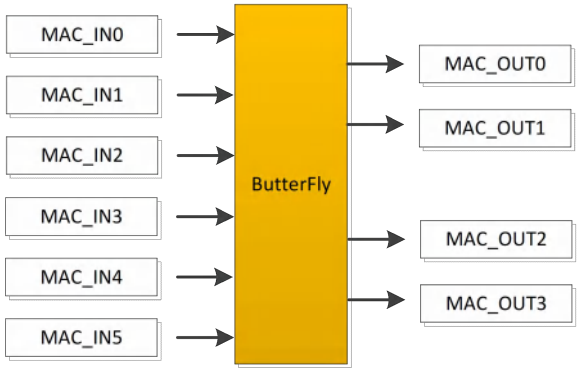
Software configuration process:

1) Configure register MAC_CTL0[7]=1 to select floating-point multiply-add mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode for floating-point numbers;
3) Configure registers MAC_IN0, MAC_IN1, and MAC_IN2 (multiplier, multiplicand, and addend);
4) Read register MAC_OUT0 to obtain the result of the multiply-add operation.

In this mode, each time the MAC_IN2 register is configured, the multiply-add operation is automatically started. Therefore, the software should first configure the MAC_IN0 and MAC_IN1 registers before configuring the MAC_IN2 register.

26.3.7 Floating-point Butterfly Operation (Single) (btfy/btfy_dma)

26.3.7.1 Single Data Conversion



Butterfly Operation

This mode performs a single butterfly operation on two original data inputs and one parameter input in the input registers and stores the result in a register for the CPU to read. In this mode, the original data inputs and the parameter input must be in floating-point format.

$$X'_{1r} = X_{1r} + W^k_{Nr}X_{2r} + W^k_{Ni}X_{2i}$$

$$X'_{1i} = X_{1i} + W^k_{Nr}X_{2i} - W^k_{Ni}X_{2r}$$

$$X'_{2r} = X_{1r} - W^k_{Nr}X_{2r} - W^k_{Ni}X_{2i}$$

$$X'_{2i} = X_{1i} - W^k_{Nr}X_{2i} + W^k_{Ni}X_{2r}$$

One butterfly operation is calculated using the formula: X_{1r}、X_{1i} and X_{2r}、X_{2i} are the real and imaginary parts of the two original data inputs,W^k_{Nr}、$W^k_{Ni}$are the real and imaginary parts of the parameter input.

Software configuration process:

1) Configure register MAC_CTL0[8]=1 to select butterfly single mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode for floating-point numbers;
3) Configure registers MAC_IN0/1/2/3/4/5 to input data;

MAC_IN0=X_{1r}

MAC_IN1=X_{1i}

MAC_IN2=X_{2r}

MAC_IN3=X_{2i}

MAC_IN4=W_{Nr}^{k}

MAC_IN5=W_{Ni}^{k}

4) Configure register MAC_CTL1[0]=1 to start the butterfly operation;
5) Wait for the flag bit MAC_FLG [5] to be set and read the results from MAC_OUT0/1/2/3.

MAC_OUT0=X'_{1r}

MAC_OUT1=X'_{1i}

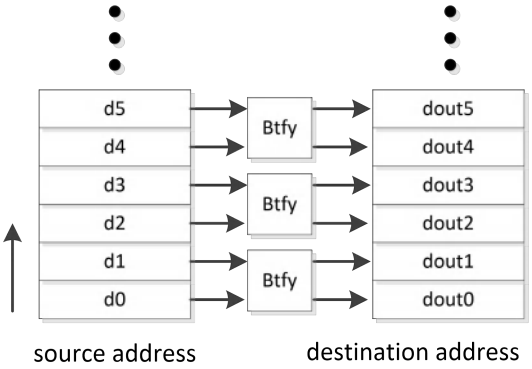
MAC_OUT2=X'_{2r}

MAC_OUT3=X'_{2i}

If interrupt enable signal is configured, an interrupt is generated after the single butterfly operation. Each time the register is configured to start the butterfly operation, the flag bit is automatically cleared.

26.3.7.2 Multiple Data Continuous Conversion

This mode calculates the butterfly operation on multiple sets of data in SRAM.



Two adjacent numbers in the same address are subject to a butterfly operation, and the result is written back to SRAM. As shown in the figure below, from a low address to a high address, two data are taken from the source data area for calculation and then written into the destination SRAM after each butterfly operation.

This mode supports having the source DMA address and the target DMA address be the same to overwrite the source data, which saves SRAM.

Software configuration process:

1) Configure register MAC_CTL0[9]=1 to select butterfly DMA mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode for floating-point numbers;
3) Configure register DMA_SRBADR to select the starting address of the source data's real part for DMA transfer;
4) Configure register DMA_SIBADR to select the starting address of the source data's imaginary part for DMA transfer;
5) Configure register DMA_PRBADR to select the starting address of the parameter table's real part for DMA transfer;
6) Configure register DMA_PIBADR to select the starting address of the parameter table's imaginary part for DMA transfer;
7) Configure register DMA_TRBADR to select the starting address of the target data's real part for DMA transfer;
8) Configure register DMA_TIBADR to select the starting address of the target data's imaginary part for DMA transfer;
9) Configure register DMA_LEN to select the number of data points (a power of 2);
10) Configure register MAC_CTL1[0]=1 to start the calculation;
11) Wait for the flag bit MAC_FLG [6] and retrieve the calculation result from SRAM.

When all the data has been calculated, a flag bit is generated. If interrupt enable is configured, an interrupt is generated. The software needs to clear the flag bit.

26.3.7.3 FFT (fp_fft)

In this mode, the hardware automatically performs a radix-2 FFT calculation on the specified data (in floating-point format) in SRAM, and stores the result back into SRAM while generating a completion flag. The data length can be configured to 64, 128, 256, 512, or 1024.

Since FFT operations require a parameter table, to speed up the FFT process, for 128/64-point FFTs, the hardware has built-in a parameter table allowing for the direct table lookup instead of accessing SRAM every time.

This mode supports having the source data and target data addresses be the same, allowing for data overwriting and reducing SRAM usage.

Software configuration process:

1) Configure register MAC_CTL0[10]=1 to select FFT mode;
2) Configure register MAC_CTL0[16:14] to select the rounding mode for floating-point numbers;
3) If using the internal parameter table, configure MAC_CTL0[27]=1; otherwise, the table is stored in SRAM and configure the DMA_PRBADR and DMA_PIBADR registers to select the starting addresses for the table's real part and imaginary part, respectively;
4) Configure the DMA_SRBADR register to select the starting address for the source data's real part for DMA transfer; configure the DMA_SIBADR to select the starting address for the source data's imaginary part for DMA transfer;
5) Configure the DMA_TRBADR register to select the starting address for the target data's real part for DMA transfer; configure the DMA_TIBADR register to select the starting address for the target data's imaginary part for DMA transfer;
6) Configure the DMA_LEN register to select the data length;
7) Wait for the completion flag bit MAC_FLG [7] to become 1, indicating that the FFT is complete.

26.3.7.4 Bit-Reverse Moving of Data (bitrev_move)

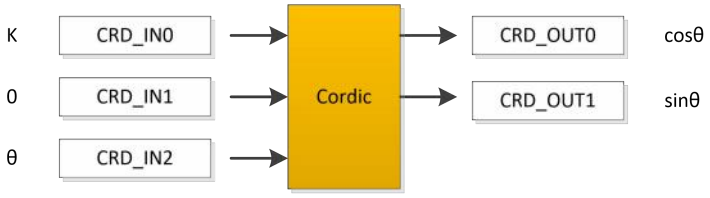
In this mode, the hardware automatically reorders a section of raw data in SRAM according to the bit-reverse algorithm and writes it to a specified location in SRAM.

The data length supports 4, 8, 16, 32, 64, 128, 256, 512, or 1024, and each data occupies 4 bytes in SRAM, stored aligned to the word in SRAM.

Software configuration process:

1) Configure register MAC_CTL0[11]=1 to select bit-reverse mode;
2) Configure the DMA_SRBADR register to select the starting address for the source data for DMA transfer;
3) Configure the DMA_TRBADR register to select the starting address for the target data for DMA transfer;
4) Configure the DMA_LEN register to select the data length;
5) Wait for the completion flag bit MAC_FLG [8] to become 1, indicating completion.

26.3.8 Sine-Cosine Calculation (sin_cos)



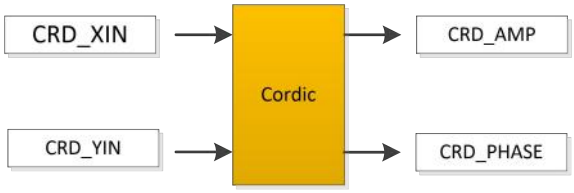
Sine-Cosine Calculation

This mode calculates the sin and cos functions given an input angle. The hardware uses the cordic rotation mode and configures $X_0 = \frac{1}{p} = K = 0.60725$, Y_0=0, $Z_0 = \theta$ to output the result$[\cos\theta, \sin\theta, 0]$.

Software configuration process:

1) Configure the CRD_ANGLE register for the input angle (register value = radian*(2^32)/(2*pi));
2) Configure CRD_CTL[1]=1 to start the operation;
3) Wait for the completion flag bit CRD_FLG [1], and read the CRD_COSINE/CRD_SINE registers to obtain the result.

26.3.9 Root-Mean-Square and Arctangent Calculation (fp_sqrt/fp_atan)



Root-Mean-Square

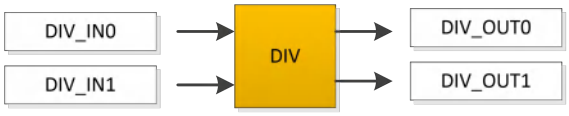
This mode calculates the root-mean-square of the input data CRD_XIN and CRD_YIN. The hardware uses the cordic vector mode, configures X_0=X, Y_0=Y, $Z_0 = 0$ to output $\left[P\sqrt{X_i^2 + Y_i^2},\ 0,\ \arctan(\frac{Y_i}{X_i})\right]$.

Software configuration process:

1) Configure the CRD_XIN register for the value of X;
2) Configure the CRD_YIN register for the value of Y;
3) Configure CRD_CTL[0]=1 to start the operation;
4) Wait for the completion flag bit CRD_FLG [0], and read the CRD_AMP/CRD_PHASE registers to obtain the result. CRD_AMP= $\sqrt{X_0^2+Y_0^2}/4*P$, $CRD_{PHASE}=\arctan(\frac{Y_0}{X_0})$ *2^31/pi

If interrupt enable is configured, an interrupt is generated after the computation is completed.

26.3.10 Floating-Point Divider (fp_div)



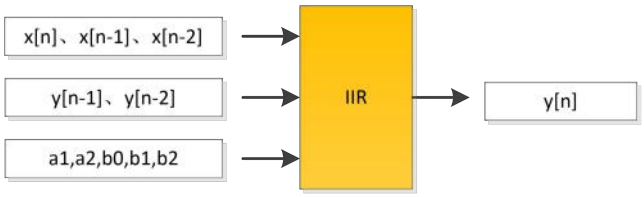
Division

This mode performs a floating-point division operation, taking in two floating-point numbers and outputting the quotient and remainder.

Software configuration process:

1) Configure the dividend into the DIV_IN0 register;
2) Configure the divisor into the DIV_IN1 register;
3) Configure MAC_CTL1[2]=1 to start the division operation;
4) Wait for the completion flag bit MAC_FLG[4], and read the DIV_OUT0 register to obtain the quotient.

26.3.11 IIR Filter



IIR Calculation

This mode performs an IIR filter calculation. Given floating-point inputs a_1、a_2、b_0、b_1、b_2、y[n-2]，y[n-1]，x[n]，x[n-1]，x[n-2], the IIR operation is executed and the output y[n] is produced.

26.3.11.1 Single Data Conversion

1) Configure MAC_CTL0[4:0]=13 (IIR_ONCE_MODE) to select IIR single mode;
2) Configure MAC_CTL0[9:7] to select the rounding mode for floating-point numbers;
3) Configure MAC_IN01/2/3/4/5, DIV_IN0/1, and MAC_OUT0/1 registers to input data.

(Note: MAC_IN0 must be configured last. After MAC_IN0 is written, hardware will automatically start the IIR operation)

MAC_IN1=x[n-1]
MAC_IN2=x[n-2]

MAC_IN3= b_0

MAC_IN4= b_1

MAC_IN5= b_2

DIV_IN0= a_1

DIV_IN1= a_2

MAC_OUT0=y[n]
MAC_OUT1=y[n-1]
MAC_IN0= x[n]

4) Wait for the flag bit MAC_FLG[10] (IIR_ONCE_DONE) to become set, and read the result from MAC_OUT0.

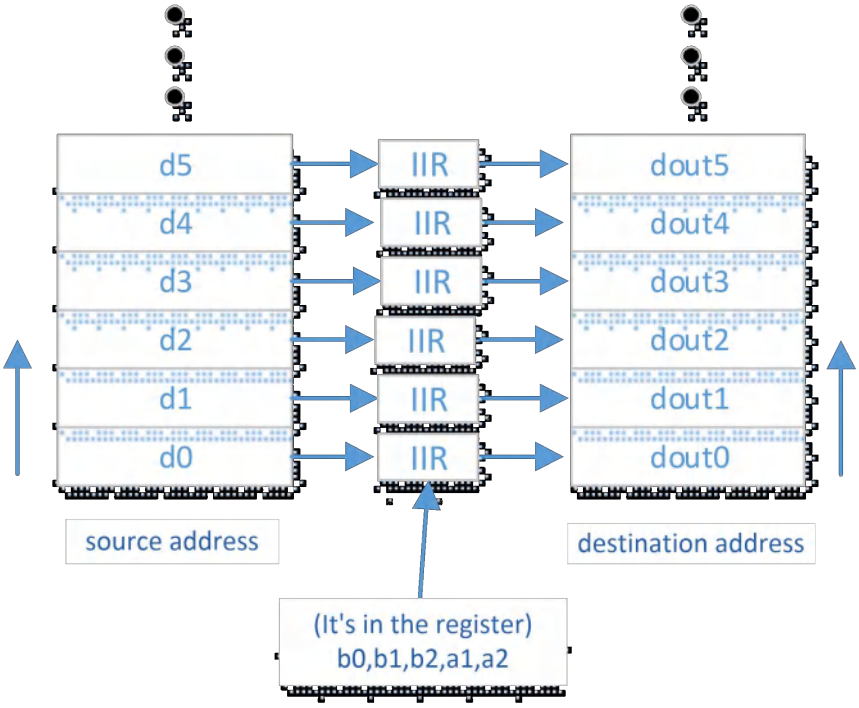
MAC_OUT0=y[n]

If interrupt enable is configured (FFT_IE [10].IIR_ONCE_IE=1), an interrupt is generated after the IIR operation. The software needs to clear the flag bit.

(Note: IIR uses DIV_IN0/1 to configure the parameters a1 and a2. DIV_IN0/1 cannot be changed during the IIR operation. Therefore, IIR and division cannot be used simultaneously.)

26.3.11.2 Multi-Data Continuous Conversion

This mode performs IIR operation on multiple sets of data in SRAM. Three adjacent numbers are taken from the source data area and subjected to IIR calculation.



The resulting output is then written back into the target SRAM area. As shown in the diagram, the data is taken from the source area from low to high addresses.

Software configuration process:

1) Configure MAC_CTL0[4:0]=14 to select IIR DMA mode;
2) Configure MAC_CTL0[9:7] to select the rounding mode for floating-point numbers;
3) Configure MAC_IN1/2/3/4/5, DIV_IN0/1, MAC_OUT0/1 to specify the input data;

   MAC_IN1=x[n-1]

   MAC_IN2=x[n-2]

   MAC_IN3= b_0

   MAC_IN4= b_1

   MAC_IN5= b_2

   DIV_IN0= a_1

   DIV_IN1= a_2

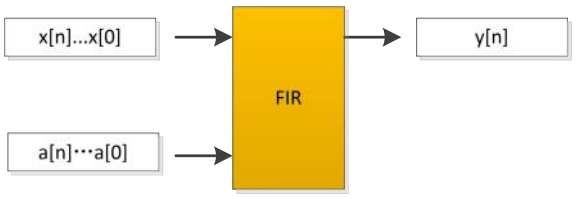
   MAC_OUT0=y[n]

   MAC_OUT1=y[n-1]
4) Configure DMA_SRBADR as the starting address for data x[n], DMA_TRBADR as the target address for data y[n], DMA_LEN as the data length, and DMA reads SRAM stepping as MAC_CTL1[3:1];
5) Configure MAC_CTL2 [0]=1 (DMA_EN) to start the operation (It is recommended to clear the bit first before writing).
6) Wait for the IIR_DMA_DONE flag bit MAC_FLG[11] to be set, and read the target SRAM address to obtain

y[n].

If interrupt enable signal is configured (FFT_IE [11].IIR_DMA_IE=1), an interrupt is generated after the IIR DMA operation. The flag bit needs to be cleared by software.

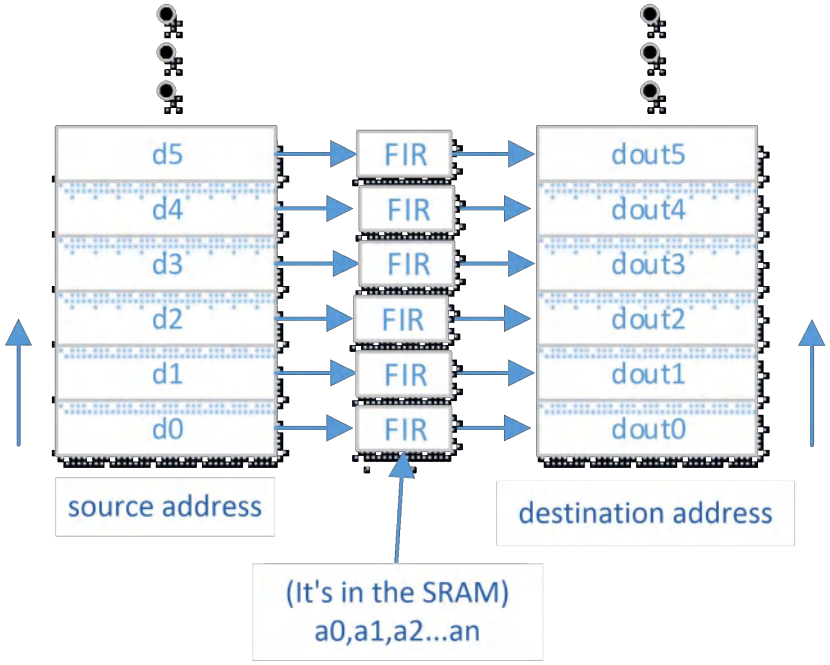
26.3.12 FIR Filter

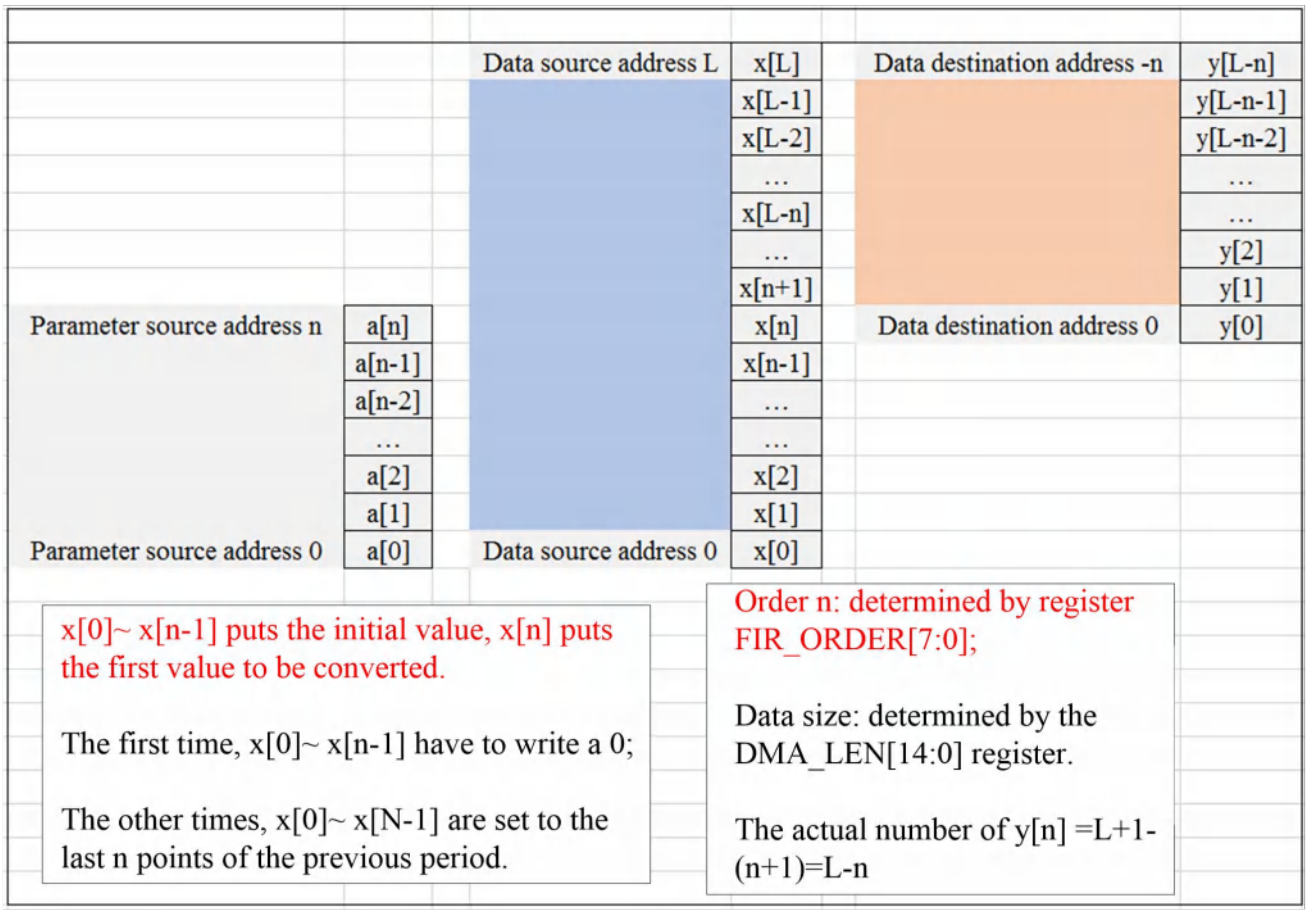


FIR Calculation

This mode performs FIR filtering, using the input floating-point data x[n]…x[0] and parameters a[n]…a[0] to perform FIR operation and produce output y[n].

This mode performs FIR operation on multiple sets of data in SRAM. N adjacent numbers are taken from the source data area and subjected to FIR calculation. The resulting output is then written back into the target SRAM area.





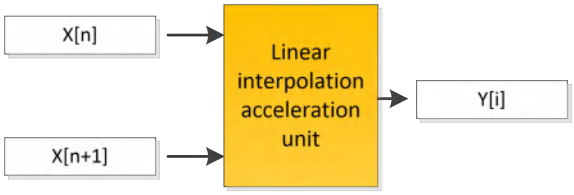
As shown in the diagram, the data is taken from the source area from low to high addresses.

Software configuration process:

1) Configure MAC_CTL0[4:0]=15 to select FIR DMA mode;
2) Configure MAC_CTL0[9:7] to select the rounding mode for floating-point numbers;
3) Configure the FIR order, DMA_SRBADR as the starting address for data x[n], DMA_PRBADR as the starting address for parameter a, DMA_TRBADR as the target address for data y[n], DMA_LEN as the data length, and DMA reads SRAM stepping as MAC_CTL1[3:1];
4) Configure MAC_CTL2 [0] =1 (DMA_EN) to start the operation (It is recommended to clear the bit first before writing).
5) Wait for the FIR_DMA_DONE flag bit MAC_FLG[11] to be set, and read the target SRAM address to obtain y[n].

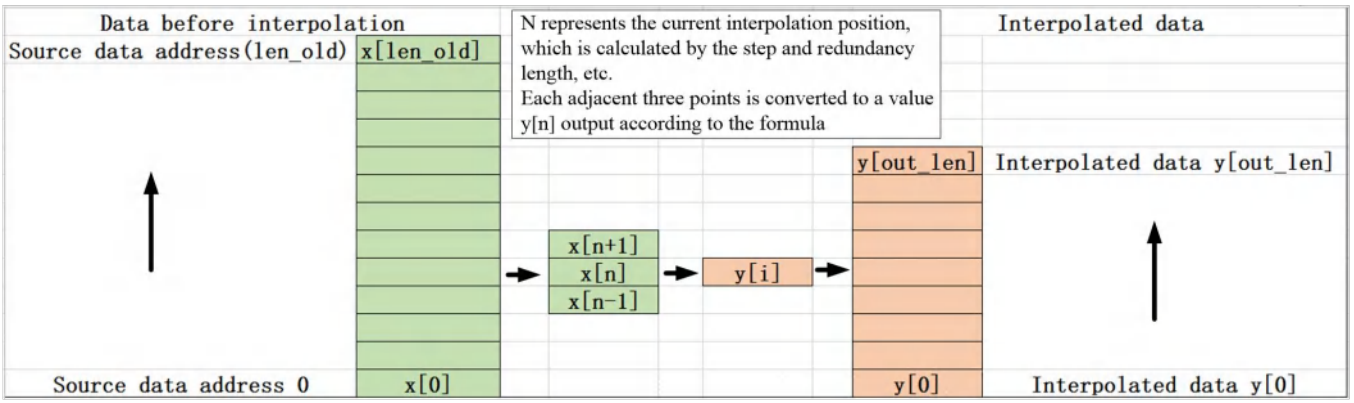
If interrupt enable signal is configured (FFT_IE [11].FIR_DMA_IE=1), an interrupt is generated after the FIR DMA operation. The flag bit needs to be cleared by software. (Note: dma_len cannot be less than fir_order, dma_len >=fir_order)

26.3.13 Linear Interpolation



This mode implements a linear interpolation acceleration algorithm. Every two adjacent points produce an output y[i] value based on a formula.

This mode performs linear interpolation operation on multiple sets of data in SRAM. Two adjacent numbers are taken from the source data area and subjected to linear interpolation calculation. The resulting output is then written back into the target SRAM area.



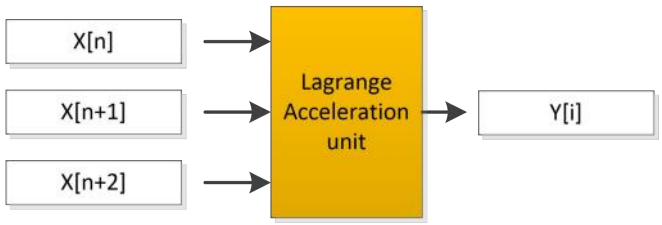
As shown in the above figure, from low to high address, every three numbers are extracted from the source data area, the linear interpolation calculation is performed, and then the result is written to the target SRAM.

Software configuration process:

1) Software calculates various parameters, including the actual available input data length ‘len’, the length of data after interpolation ‘out_len’, and the current interpolation position ‘t’;
2) Configure MAC_CTL0[4:0]=16 (LINE_INTP) to select linear interpolation mode;
3) Configure MAC_CTL0[9:7] to select the rounding mode for floating-point numbers;
4) Configure DMA_SRBADR as the starting address for data x[n], DMA_TRBADR as the target address for data y[i];
5) Configure MAC_IN5[31:0] (the last data from the previous cycle);
6) Configure MAC_CTL1[0] to select whether to use the last data from the previous cycle;
7) Configure INTP_LEN[12:0] to select the actual available input data length;
8) Configure DMA_LEN[10:0] to select the length of data after interpolation;
9) Configure INTP_LOC[31:0] to select the current interpolation position;
10) Configure INTP_STEP[31:0] to select the step;
11) Configure MAC_CTL2 [0]=1 (DMA_EN) to start the operation (It is recommended to clear the bit first before writing).
12) Wait for the LINE_INTP_DONE flag bit FFT_FLG[13] to be set, and read the target SRAM address to obtain y[n].
13) Read INTP_LOC [31:0] and set t=INTP_LOC [31:0]. Software calculates the redundant length ‘red_len’ as len-t+step after this interpolation operation is complete.
14) Depending on the specific situation, software can choose whether to save the last data. If necessary, write the value to MAC_IN5 [31:0] (the last data from the previous cycle).

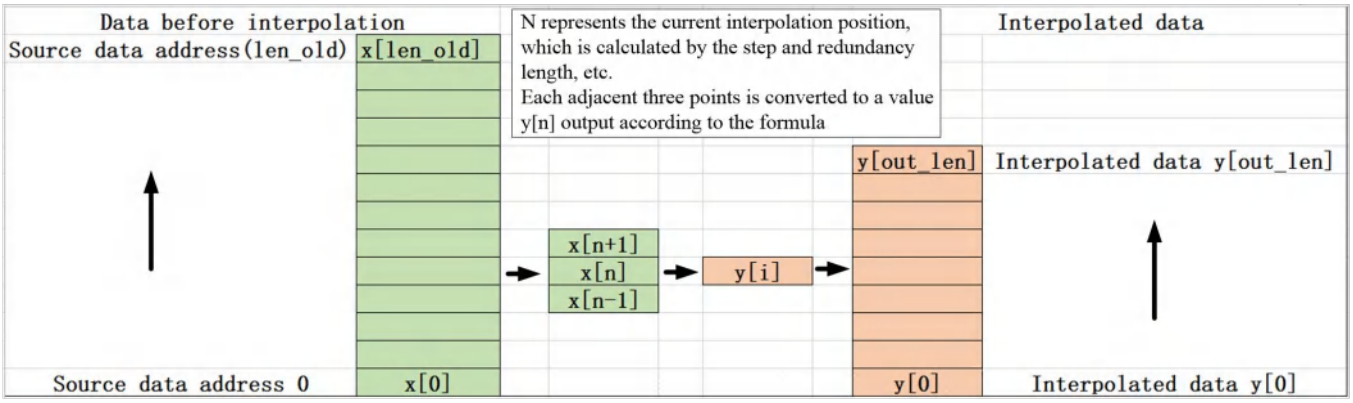
If interrupt enable signal is configured (FFT_IE [13].LINE_INTP_IE=1), an interrupt is generated after the linear interpolation operation. The flag bit needs to be cleared by software.

26.3.14 Lagrange Interpolation



This mode implements a Lagrange interpolation acceleration algorithm. Every three adjacent points produce an output y[i] value based on a formula.

This mode performs Lagrange interpolation operation on multiple sets of data in SRAM.



Three adjacent numbers are taken from the source data area and subjected to Lagrange interpolation calculation. The resulting output is then written back into the target SRAM area. As shown in the diagram, the data is taken from the source area from low to high addresses.

Software configuration process:

1) Software calculates various parameters, including the actual available input data length ‘len’, the length of data after interpolation ‘out_len’, and the current interpolation position ‘t’;
2) Configure MAC_CTL0[4:0]=17 (LAGR_INTP) to select Lagrange interpolation mode;
3) Configure MAC_CTL0[9:7] to select the rounding mode for floating-point numbers;
4) Configure DMA_SRBADR as the starting address for data x[n], DMA_TRBADR as the target address for data y[i];
5) Configure MAC_IN5[31:0] (the last data from the previous cycle);
6) Configure MAC_CTL1[0] to select whether to use the last data from the previous cycle;
7) Configure INTP_LEN[12:0] to select the actual available input data length;
8) Configure DMA_LEN[9:0] to select the length of data after interpolation;
9) Configure INTP_LOC[31:0] to select the current interpolation position;
10) Configure INTP_STEP[31:0] to select the step;
11) Configure MAC_CTL2 [0] =1 (DMA_EN) to start the operation (It is recommended to clear the bit first before writing).
12) Wait for the LAGRINTP_DONE flag bit MAC_FLG[14] to be set, and read the target SRAM address to

obtain y[n];

13) Read INTP_LOC [31:0] and set t=INTP_LOC [31:0]. Software calculates the redundant length 'red_len' as len-t+step after this interpolation operation is complete.
14) Depending on the specific situation, software can choose whether to save the last data. If necessary, write the value to MAC_IN5 [31:0] (the last data from the previous cycle).

If interrupt enable signal is configured (FFT_IE [14].LAGR_INTP_IE=1), an interrupt is generated after the Lagrange interpolation operation. The flag bit needs to be cleared by software.

26.4 Implementation Details

26.4.1 Integer to Floating-Point Conversion

Since the input integer width is 32 bits and the resulting floating-point number has a very small range of values for the exponent, there will be no overflow. Moreover, when normalizing, the highest value supported is 32, so no overflow processing is required.

Normalization involves subtracting n from the exponent and leaving the fractional part unchanged.

26.4.2 Floating-Point to Integer Conversion

Before converting, the floating-point number needs to be magnified to make the integer part large enough to ensure more effective bits.

Magnifying by 2^n involves adding n to the exponent and leaving the fractional part unchanged.

26.4.3 FFT Explanation

Software only needs to store the original data in SRAM in advance and configure the DMA starting address, target address, and data length. Hardware automatically performs computation by fetching data and produces the result of the butterfly. If the data length is 64, there will be 32 butterfly operations per stage (64/2=32), and a total of 6 stages in $\log_2 64 = 6$. Therefore, hardware automatically computes 32*6 butterfly operations and saves the result to the specified location in SRAM, generating a completion flag or interrupt.

For each butterfly operation, the hardware reads the SRAM four times to obtain the original data (the imaginary part of the original input data is zero in the first round), writes to the SRAM four times to save the butterfly operation result, and if the parameter table is stored in SRAM, reads the SRAM twice to obtain the parameters. Therefore, the number of SRAM cycles required to complete data of a specified length is:

$k_0 = \frac{n}{2} * log_2 n * (4+4) - \frac{n}{2} * 2$, Hardware parameter table hardening.

$k_0 = \frac{n}{2} * log_2 n * (4+4+2) - \frac{n}{2} * 2$, Parameter table stored in SRAM.

	Read/write SRAM cycles	
Data points	Hardware table	SRAM table

64	1472	1856
128	3456	4352
256	7936	9984
512	17920	22528
1024	39936	50176

Number of cycles required to read/write SRAM to complete the FFT

A single butterfly operation can be completed in as little as 10 clock cycles (if the parameter table is hardware-solidified) or 12 clock cycles (if the parameter table is stored in SRAM) when performing SRAM read/write and butterfly computation.

Clock cycle	1	2	3	4	5	6	7	8	9	10	11	12
Hardware behavior	R	R	R	R	R	R						
		H	H	H	H	H	H					
								Mul	Mul	Mul	MUl	
								Add	Add	Add	Add	
								Add	Add	Add	Add	
									R	R	R	R

So the total time is:

$k_0 = \frac{n}{2} * log_2 n * 10$, Hardware parameter table hardening.

$k_0 = \frac{n}{2} * log_2 n * 12$, Parameter table stored in SRAM.

Data points	FFT clock cycles		FFT time (us) 16M clock	
	Hardware table	SRAM table	Hardware table	SRAM table
64	1920	2304	120	144
128	4480	5376	280	336
256	10240	12288	640	768
512	23040	27648	1440	1728
1024	51200	61440	3200	3840

To achieve the fastest completion time for FFT, add the time to configure DMA and other mode registers to the calculation time shown in the table. The time in the table is based on the assumption that the SRAM is idle and accessed only by the FFT module. In reality, there may be other modes competing for access to the SRAM, which could result in an extended FFT time.

26.4.4 Explanation of Cordic

Arc tangent parameter table, ranging from arctan(1), 45 degrees, arctan(1/2), all the way up to arctan(1/2^n). All parameters need to be scaled proportionally, taking arctan (1) =2^n as the standard, and scaling the others by the same factor a. The scaling factor is a fixed-point operation that introduces error.

During each iteration process, x and y undergo shift processing (floor approximation), which also introduces errors. If rounded instead of truncated, the error will be reduced.

The number of iterations is determined by the parameter values after scaling. If the parameter value is 0, the iteration process ends.

26.4.4.1 Vector mode

Confirmation of bit width:

1. Firstly, the bit width of the input x and y is 32-bit.
2. In this mode, the input z=0, so the scaling factor of arctan is independent of the input and can be chosen arbitrarily. Only the desired output angle accuracy determines the scaling factor n of arctan.
3. Determine the number of iterations based on the scaling factor of arctan.
4. The final output angle accuracy is related to the scaling factor n of arctan. The output angle result must be divided by n to obtain the actual angle (since this angle is accumulated, z(i+1)=z(i)-arctan(1/2^i); both sides are multiplied by n). It is also possible to output the result by selecting the high bits (which is more accurate and produces shorter output results).

In the vector mode, the input x and y can be equally scaled, resulting in higher accuracy. Therefore, for small x and y, better accuracy can be achieved by scaling them before feeding into the CORDIC operation.

Firstly, pre-processing is required to move all angles to the first quadrant. If it is in the second quadrant, the initial angle z=90 degrees after moving to the first quadrant. If it is in the third quadrant, the initial angle z=180 degrees. If it is in the fourth quadrant, the initial angle z=270 degrees.

```
if(x<0){
    x=-x;
    y=-y;
    z=z-(1~3)pi/2*n;    // n is the scaling factor
}
```

26.4.4.2 Rotation mode

Confirmation of bit width:

1 The module input is in radians with a range of -π to π. Assuming the input radians are represented by n bits, the scaling factor for the input radians is p0=(2^n)/2pi.

2 According to the formula, z(i+1)=z(i)-arctan(1/2^i), the scaling factor of atan is the same as the scaling factor of the input angle z when doing addition and subtraction operations. atan_t(n)=p0*atan(n), and other parameter values are scaled by the same factor p0.

3 Normally, atan_t(1)=p0*atan(n)=2^(n-3), so the bit width of the parameter table is n-3. If the bit width of the parameter table is set longer to reduce the error of fixed-point arithmetic, the input data only needs to be right-shifted to achieve the same scaling factor when performing addition and subtraction operations. For example, if the bit width of atan during fixed-point arithmetic is n-3+5, the amplification before the

operation is::

x_in = {x_in,5'h0};
y_in ={y_in,5'h0};
z_in ={z_in,5'h0};

After iteration, select the high bits for output.

4 The output result after iteration is also scaled up by p0. The scaling factor of the output can be adjusted according to the bit width of the output data.

Implementation of rotation mode: Input X_0=k, Y_0=0, Z_0=θ. The input angle range is -pi~pi. Firstly, preprocess the angle and flip it to the range of 0: π/2. Then iterate according to the formula to obtain the result. The result is then multiplied by the gain factor K. The bit width of the input x and y is related to the number of iterations, as each iteration shifts 1 bit.

5

Implementation process of rotation mode:

Input $X_0 = k$, Y_0=0, $Z_0 = \theta$; The input angle range is -pi~pi.

1. Firstly, preprocess the angle and flip it to the 0: π/2 range.
2. Then iterate according to the formula to get the result.
3. And finally multiply the gain factor K.
4. The bit width of input x and y is related to the number of iterations because each bit is shifted 1 bit.

26.5 Register

26.5.1 Register List

Base Addres	0x40058000				
Offset Address	**Register Name**	**R/W**	**Byte Length**	**Reset Value**	**Description**
0x0	MAC_CTL0	R/W	4	0x0	MAC Control Register 0
0x4	MAC_CTL1	R/W	4	0x0	MAC Control Register 1
0x8	MAC_CTL2	R/W	4	0x0	MAC Control Register 2
0xC	MAC_IN0	R/W	4	0x0	MAC Input Register 0
0x10	MAC_IN1	R/W	4	0x0	MAC Input Register 1
0x14	MAC_IN2	R/W	4	0x0	MAC Input Register 2
0x18	MAC_IN3	R/W	4	0x0	MAC Input Register 3
0x1C	MAC_IN4	R/W	4	0x0	MAC Input Register 4
0x20	MAC_IN5	R/W	4	0x0	MAC Input Register 5
0x24	MAC_OUT0	R/W	4	0x0	MAC Output Register 0
0x28	MAC_OUT1	R/W	4	0x0	MAC Output Register 1
0x2C	MAC_OUT2	R/W	4	0x0	MAC Output Register 2
0x30	MAC_OUT3	R/W	4	0x0	MAC Output Register 3
0x34	DIV_IN0	R/W	4	0x0	Division Unit Input 0
0x38	DIV_IN1	R/W	4	0x0	Division Unit Input 1

0x3C	DIV_OUT0	R/W	4	0x0	Division Unit Output
0x40	DMA_SRBADR	R/W	4	0x0	DMA source data Base address of FFT real part
0x44	DMA_SIBADR	R/W	4	0x0	DMA source data Base address of FFT imaginary part
0x48	DMA_PRBADR	R/W	4	0x0	DMA source data Base address of the twiddle factors table real part
0x4C	DMA_PIBADR	R/W	4	0x0	DMA source data Base address of the twiddle factors table imaginary part
0x50	DMA_TRBADR	R/W	4	0x0	DMA target data Base address of FFT real part
0x54	DMA_TIBADR	R/W	4	0x0	DMA target data Base address of FFT imaginary part
0x58	DMA_LEN	R/W	2	0x0	DMA length configuration
0x5C	DSP_IE	R/W	2	0x0	FFT Interrupt Enable Register
0x60	DSP_FLG	R/W	2	0x0	FFT Flag Register
0x64	ALU_STA0	R/W	4	0x0	ALU Status Register 0
0x68	ALU_STA1	R/W	2	0x0	ALU Status Register 1
0x6C	CRD_CTL	WO	1	0x0	Cordic ControlRegiste
0x70	CRD_XIN	R/W	4	0x0	Cordic Vector mode data x input
0x74	CRD_YIN	R/W	4	0x0	Cordic Vector mode data y input
0x78	CRD_AMP	R	4	0x0	Cordic Vector mode Amplitude Output
0x7C	CRD_PHASE	R	4	0x0	Cordic Vector mode Phase Output
0x80	CRD_ANGLE	R	4	0x0	Cordic Rotation mode Angle Input
0x84	CRD_COS	R	4	0x0	Cordic Rotation mode Cosine Output
0x88	CRD_SIN	R	4	0x0	Cordic Rotation mode Sine Output
0x8C	CRD_IE	R/W	1	0x0	Cordic Interrupt Enable
0x90	CRD_FLG	R/W	1	0x0	Cordic Completion Flag Register
0x94	INTP_LEN	R/W	2	0x0	Interpolation Input Data Length Register
0x98	INTP_LOC	R/W	4	0x0	Current Interpolation Position Register
0x9C	INTP_STEP	R/W	4	0x0	Interpolation Algorithm Step Register

26.5.2 MAC_CTL0 (0x0)

Offset Address: 00H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:23	Reserved	--	R	0
22:21	I2F_PRE_EN	Integer to floating point preprocessing. If it is set to 1, it means that in every 4 bytes, the highest byte data is invalid, and the valid data is only 3 bytes. If it is set to 0, it means that 4 bytes are valid.	R/W	0
20	FFT_TB_EN	FFT uses a fixed parameter table saved by the chip, only 64 points and 128 points are valid. =0: Do not use the fixed parameter table saved by the chip =1: Use chip-saved fixed parameter table	R/W	0
19:15	F2I_MUL	Before converting a floating-point number to an integer, multiply the floating-point number by a factor. 0 The factor is equal to 1 n The factor is equal to 2^n	R/W	0
14:10	I2F_DIV	After converting the integer to a floating point number, divide the floating point number by a factor. 0 The factor is equal to 1 n The factor is equal to 2^n	R/W	0
9:7	ROUND_MODE	Configure rounding mode during floating point arithmetic. When rnd=000, the rounding mode is rounding to nearest. When rnd=001, the rounding mode is rounding toward zero. When rnd=010, the rounding mode is rounding to positive infinity. When rnd=011, the rounding mode is rounding to negative infiinity. When rnd=100, the rounding mode is rounding to nearst up. When rnd=101, the rounding mode is rounding away from zero,. Other: Reserved.	R/W	0
6	MUL_OUT_FM	Floating-point multiplication, output data format: =0: floating-point =1: integer	R/W	0
5	MUL_IN_FM	Floating point multiplication, input data format: =0: floating-point =1: integer	R/W	0
4:0	MODE_SEL	5'd0: All modes are disabled 5'd1: Integer to floating-point conversion, single enable	R/W	0

		5'd2: Integer to floating-point conversion, DMA enable 5'd3: Floating-point to integer conversion, single enable 5'd4: Floating-point to integer conversion, DMA enable 5'd5: Floating-point multiplication, mode enable 5'd6: Floating-point addition, mode enable 5'd7: Floating-point subtraction, mode enable 5'd8: Floating-point multiply-accumulate operation, mode enable (y = ax + b) 5'd9: Butterfly operation, single enable 5'd10: Butterfly operation, DMA enable 5'd11: FFT mode enable 5'd12: Bit Reverse mode enable 5'd13: Second-order IIR single operation, mode enable 5'd14: Second-order IIR DMA operation, mode enable 5'd15: N-order FIR DMA operation, mode enable 5'd16: Linear interpolation operation, mode enable 5'd17: Lagrange interpolation operation, mode enable 5'd18~31: All modes are disabled.		

26.5.3 MAC_CTL1 (0x04)

Offset Address: 04H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:12	Reserved	--	R	0
11:4	FIR_ORDER	FIR filter order configuration: 0~3: 3rd order; 4: 4th order; 5: 5th order; … 254: 254th order; 255: 255th order;	R/W	0
3:1	DMA_STEP	Step size for DMA read from SRAM, only effective for IIR, FIR DMA mode: 0:Step size 1; 1:Step size 2; ... 7: Step size 8;	R/W	0
0	INTP_LAST_EN	Interpolation mode uses the last data from the previous cycle, enable signal	R/W	0

26.5.4 MAC_CTL2 (0x08)

Offset Address: 08H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:3	Reserved	---	R	0

2	DIV_KICK	The division operation unit starts the enable signal	WO	0
1	BTFY_ONCE_KICK	Butterfly operation unit one-shot modetart signal Active at high level	WO	0
0	DMA_EN	DMA enable signal configuration bit: All DMA-related operations are started by configuring this bit to 1, and this bit will be automatically cleared to 0 after DMA completes the operations.	R/W	0

Note: 1.Bit1 and Bit2 are write-only bits.

Refer to chapter 21.3 for the operation instructions and specific configurations that can be implemented using the MAC unit.

26.5.5 MAC_IN0 (0x0C)

Offset Address: 08H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN0	Multiplication and addition unit data input port 0	R/W	0

26.5.6 MAC_IN1 (0x10)

Offset Address: 0CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN1	Multiplication and addition unit data input port 1	R/W	0

26.5.7 MAC_IN2 (0x14)

Offset Address: 10H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN2	Multiplication and addition unit data input port 2	R/W	0

26.5.8 MAC_IN3 (0x18)

Offset Address: 14H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN3	Multiplication and addition unit data input port 3	R/W	0

26.5.9 MAC_IN4 (0x1C)

Offset Address: 18H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN4	Multiplication and addition unit data input port 4	R/W	0

26.5.10 MAC_IN5 (0x20)

Offset Address: 1CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_IN5	Multiplication and addition unit data input port 5	R/W	0

26.5.11 MAC_OUT0 (0x24)

Offset Address: 20H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_OUT0	Multiplication and addition unit data output port 0	R/W	0

26.5.12 MAC_OUT1 (0x28)

Offset Address: 24H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_OUT1	Multiplication and addition unit data output port 1	R/W	0

26.5.13 MAC_OUT2 (0x2C)

Offset Address: 28H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_OUT2	Multiplication and addition unit data output port 2	R/W	0

26.5.14 MAC_OUT3 (0x30)

Offset Address: 2CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	MAC_OUT3	Multiplication and addition unit data output port 3	R/W	0

26.5.15 DIV_IN0 (0x34)

Offset Address: 30H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	DIV_IN0	Division unit data input port (dividend)	R/W	0

26.5.16 DIV_IN1 (0x38)

Offset Address: 34H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	DIV_IN1	Division unit data input port (divisor)	R/W	0

26.5.17 DIV_OUT0 (0x3C)

Offset Address: 38H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value

31:0	DIV_OUT0	Division unit output port (quotient)	R	0

26.5.18 DMA_SRBADR (0x40)

Offset Address: 3CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:0	DMA_SRBADR	DMA source data Base address: (Word address) FFT/BTFY_DMA mode: DMA source data Base address of FFT real part. I2F_DMA/F2I_DMA/BIT_REV mode: DMA source data Base address	R/W	0

26.5.19 DMA_SIBADR (0x44)

Offset Address: 40H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:0	DMA_SIBADR	DMA source data Base address: (Word address) FFT/BTFY_DMA mode: DMA source data Base address of FFT imaginary part.	R/W	0

26.5.20 DMA_PRBADR (0x48)

Offset Address: 44H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:0	DMA_PRBADR	DMA source data Base address: (Word address) DMA source data Base address of the twiddle factors table real part.	R/W	0

26.5.21 DMA_PIBADR (0x4C)

Offset Address: 48H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:0	DMA_PIBADR	DMA source data Base address: (Word address) DMA source data Base address of the twiddle factors table imaginary part.	R/W	0

26.5.22 DMA_TRBADR (0x50)

Offset Address: 4CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value

31:16	Reserved	--	R	0
15:0	DMA_TRBADR	DMA target data Base address: (Word address) FFT/BTFY_DMA mode: DMA target data Base address of FFT real part. I2F_DMA/F2I_DMA/BIT_REV mode: DMA target data Base address.	R/W	0

26.5.23 DMA_TIBADR (0x54)

Offset Address: 50H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:0	DMA_TIBADR	DMA target data Base address: (Word address) FFT/BTFY_DMA mode: DMA target data Base address of FFT imaginary part.	R/W	0

26.5.24 DMA_LEN (0x58)

Offset Address: 54H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	--	R	0
9:0	DMA_LEN	When the number of points is configured as n, length=(n+1)Word I2F_DMA/F2I_DMA/BTFY_DMA mode: Support any configuration. Bit-reverse mode: Only supports configuring the number of points as 4, 8, 16, 32, 64, 128, 256, 512 or 1024. FFT mode: Only supports configuring the number of points as 64, 128, 256, 512 or 1024.	R/W	0

26.5.25 DSP_IE (0x5C)

Offset Address: 5CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:15	Reserved	--	R	0
14	LAGR_DMA_IE	Lagrange Interpolation Completion Interrupt enable	R/W	0
13	LINE_DMA_IE	Linear Interpolation Completion Interrupt enable	R/W	0
12	FIR_DMA_IE	FIR DMA Calculation Completion Interrupt enable	R/W	0
11	IIR_DMA_IE	IIR DMA Calculation Completion Interrupt enable	R/W	0
10	IIR_ONCE_IE	Single IIR Operation Completion Interrupt enable	R/W	0
9	MULT_IE	Floating point multiplication interrupt enable	R/W	0
8	BITREV_IE	Bit-reverse mode interrupt enable	R/W	0
7	FFT_IE	FFT Mode Interrupt Enable	R/W	0
6	BTFY_DMA_IE	Butterfly DMA Interrupt Enable	R/W	0

5	BTFY_ONCE_IE	One time Butterfly Interrupt Enable	R/W	0
4	F2I_DMA_IE	Floating point to integer DMA interrupt enable	R/W	0
3	I2F_DMA_IE	Integer to floating point DMA interrupt enable	R/W	0
2	DIV_IE	Division unit interrupt enable	R/W	0
1	DMA_IE	DMA interrupt enable	R/W	0
0	MAC_IE	Multiplication and addition unit	R/W	0

Note: The above IE control bits, =1 enable interrupt, =0 disable interrupt.

26.5.26 DSP_FLG (0x60)

Offset Address: 60H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:15	Reserved	--	R	0
14	LAGR_DMA_DONE	Lagrange Interpolation Completion Interrupt Flag Write 1 to Clear 0	R/WC	0
13	LINE_DMA_DONE	Linear Interpolation Completion Interrupt Flag Write 1 to Clear 0	R/WC	0
12	FIR_DMA_DONE	FIR DMA Calculation Completion Interrupt Flag Write 1 to Clear 0	R/WC	0
11	IIR_DMA_DONE	IIR DMA Calculation Completion Interrupt Flag Write 1 to Clear 0	R/WC	0
10	IIR_ONCE_DONE	Single IIR Operation Completion Interrupt Flag Write 1 to Clear 0	R/WC	0
9	MULT_DONE	Floating-point multiplication complete interrupt flag Write 1 to clear 0	R/WC	0
8	BITREV_DONE	Bit-reverse mode interrupt flag Write 1 to clear 0	R/WC	0
7	FFT_DONE	FFT mode interrupt flag Write 1 to clear 0	R/WC	0
6	BTFY_DMA_DONE	Butterfly DMA Interrupt Flag Write 1 to clear 0	R/WC	0
5	BTFY_ONCE_DONE	Butterfly one time mode Interrupt Flag Write 1 to clear 0	R/WC	0
4	F2I_DMA_DONE	Floating point to integer DMA interrupt flag Write 1 to clear 0	R/WC	0
3	I2F_DMA_DONE	Integer to floating point DMA interrupt flag Write 1 to clear 0	R/WC	0
2	DIV_DONE	Division Unit Interrupt Flag Write 1 to clear 0	R/WC	0
1	DMA_DONE	DMA complete signal interrupt flag Write 1 to clear 0	R/WC	0
0	MAC_DONE	Multiplication and addition unit calculation (MUL	R/WC	0

		or BTFY_ONCE) completed Write 1 to clear 0		

26.5.27 ALU_STA0 (0x64)

Offset Address: 60H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:24	F2I_STATUS	Floating point to integer unit operation status flag The definition is the same as 'Multiplication and addition unit 0-operation status flag.	R	1
23:16	I2F_STATUS	Integer to floating point unit operation status flag The definition is the same as 'Multiplication and addition unit 0-operation status flag.	R	1
15:8	ADDSUB1_STATUS	Multiplication and addition unit 1-operation status flag The definition is the same as 'Multiplication and addition unit 0-operation status flag'	R	1
7:0	ADDSUB0_STATUS	Multiplication and addition unit 0-operation status flag bit0: Integer or floating point output is zero. bit1: floating point output is infinity. bit2: Floating point operation is invalid. It is also set to 1 when one of the inputs is NaN. bit3: floating point number less than minimum normalized number. bit4: floating point number greater than maximum normalized number. bit5: Integer or floating-point output is not equal to an infinitely precise result. bit6: The size of the rounded integer result is larger than the largest representable two integers with the same sign. bit7: Reserved.	R	1

26.5.28 ALU_STA1 (0x68)

Offset Address: 64H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	--	R	0
15:8	DIV_STATUS	The operation state of the division unit. The definition is the same as 'Multiplication and addition unit 0-operation status flag'	R	x
7:0	MUL_STATUS	Multiplication unit operation status. The definition is the same as 'Multiplication and addition unit 0-operation status flag'.	R	1

26.5.29 CRD_CTL (0x6C)

Offset Address: 68H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value

31:1	Reserved	--	R	0
1	CRD_ROT_KICK	cordic rotation mode start signal	WO	0
0	CRD_VEC_KICK	cordic vector mode enable signal	WO	0

Note: This register has no read function, it is a write-only register.

26.5.30 CRD_XIN (0x70)

Offset Address: 6CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	X_IN	Cordic Vector mode data x input	R/W	0

26.5.31 CRD_YIN (0x74)

Offset Address: 70H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	Y_IN	Cordic Vector mode data y input	R/W	0

26.5.32 CRD_AMP (0x78)

Offset Address: 74H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	AMP_OUT	Cordic Vector mode Amplitude Output $AMP\_OUT = \sqrt{X_0^2 + Y_0^2}/4*P$	R/	0

26.5.33 CRD_PHASE (0x7C)

Offset Address: 78H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	PHASE_OUT	Cordic Vector mode Phase Output $PHASE\_OUT = \arctan(\frac{Y_0}{X_0})$ *2^31/pi	R	0

26.5.34 CRD_ANGLE (0x80)

Offset Address: 7CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	ANGLE_IN	Cordic rotation mode input in radians in the range [-pi:pi] Enter -1*2^31 for -pi, enter 1*2^31 for pi ANGLE_IN =radian*2^31/pi	R/W	0

26.5.35 CRD_COSINE (0x84)

Offset Address: 80H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	COSINE_OUT	Cordic Vector mode Cosine Output COSINE_OUT=cos(angle)*(2^(31-2))/(2*pi) angle=radian*180/pi	R	0

26.5.36 CRD_SINE (0x88)

Offset Address: 84H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	SINE_OUT	Cordic Vector mode Sine Output SINE_OUT=sin(angle)*(2^(31-2))/(2*pi)	R	0

26.5.37 CRD_IE (0x8C)

Offset Address: 88H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	--	R	0
0	CRD_ROT_IE	Cordic Rotation Mode Completion Interrupt Enable Bit	R/W	0
0	CRD_VEC_IE	Cordic Vector Mode Completion Interrupt Enable Bit	R/W	0

26.5.38 CRD_FLG (0x90)

Offset Address: 8CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:1	Reserved	--	R	0
1	CRD_ROT_DONE	Cordic Rotation Mode Completion Flag Write 1 to clear 0	R/W	0
0	CRD_VEC_DONE	Cordic Vector Mode Completion Flag Write 1 to clear 0	R/W	0

26.5.39 INTP_LEN (0x94)

Offset Address: 94H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:13	Reserved	--	R	0
12:0	INTP_LEN	The actual available input data length for the interpolation algorithm，i.e., the number of x[n]. Points configuration n, length = (n+1) Word. (Integer type)	R/W	0

26.5.40 INTP_LOC (0x98)

Offset Address: 98H Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	INTP_LOC	Current Interpolation Position (floating-point) for Interpolation Algorithm	R/W	0

26.5.41 INTP_STEP (0x9C)

Offset Address: 9CH Reset Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:0	INTP_STEP	Step Size (floating-point) for Interpolation Algorithm	R/W	0

26.6 Software Operation Process

Please refer to the routine provided by Renergy Micro-Technologies Co., Ltd. for specific implementation. The following instructions are for learning reference only.

26.6.1 Full Program Description:

1. The ADC samples the data integer d0, which is stored in SRAM with a bit width in 24-bit binary complement format.
2. Data preprocessing: Normalization of ADC data (binary complement format) to signed floating-point format d1. The range of representation is -1 to 1.
3. FFT operation: Input to the FFT operation on all converted numbers d1, in complex format, where the real part is d1 and the imaginary part is 0. The FFT operation results in an FFT output. The output is a complex number, the real part Re and the imaginary part Im are floating point numbers.
4. Calculation of harmonic content:

   repeat(6){

   $$Y_0 = \sqrt{Re0 * Re0 + Im0 * Im0},$$

   for(n=1;n<42;n++){

   $$Y_n = \sqrt{Ren * Ren + Imn * Imn},$$

   Yin=k*Yn/Y0,

   }

   }

   Calculate the 41st harmonic content.

   Both current and voltage need to be done separately for harmonic content Yu and Yi.
5. Phase angle calculations and harmonic power::

   repeat(3){

   for(n=1;n<42;n++){

   Aun=atan(Ren/Imn),// For voltage data

   Ain=atan*(Ren/Imn),// For current data

   A=((Au-Ai)+A0*n)*180/pi,

   PFn=cos(A*pi/180)

   }

   }

   Calculate the phase angle 40 times without the fundamental frequency. Requires an accuracy of 0.01

degrees.

6. Calculation of harmonic power: Phn=FSA*Yun*Yin*PFn. The 41st harmonic is calculated and then accumulated, where the FSA is obtained externally.

26.6.2 Operation process:

1. Cache the ADC sampled data sdata0 to SRAM, with each point having 24-bit data.
2. Use i2f_dma mode to convert sdata1 in SRAM to the floating-point format and normalize it to obtain sdata2. Note that only the third byte of each word address in SRAM is valid at this point. Therefore, it is necessary to configure MAC_CTL0[28]=1, and ignore the highest byte..
3. Use bitrev_mode mode to do bit-reverse to transform sdata2 into sdata3.
4. Use the FFT calculation module to perform FFT calculation on sdata3 to obtain the result (the software needs to write the FFT calculation table to SRAM in advance).
5. Use the hardware CORDIC module, division module to calculate harmonic content and harmonic power.

27 Energy Integration Unit D2F(New)

27.1 Overview

The chip integrates 12 custom energy integration units, with power signals D2FP0~D2FP11 as inputs. The electric constant Hfconst4~7 can be set for integration based on the input power and electric constant Hfconst4~7. The electric energy is stored in the D2FE00~D2FE11 registers, where D2FP0~D2FP4 support pulse output, classified as D2F_ OUT0~D2F_ OUT4, as a check pulse output, supports electrical energy pulse interruption. When the output pulse period is greater than or equal to 160ms, the high level of the check pulse is fixed at 80ms, and the low level changes according to the cycle value. It will output an equal duty pulse when the output pulse period is less than 160ms.

Base address: 0x4005C000

27.2 Features

- 12 channels D2F
- D2F00~ D2F05 support output 5 pulses D2F_OUT0~D2F_OUT4
- Pulse output, if the output pulse period>=160ms, the pulse high level is fixed to keep 80ms, and the low level is changed according to the period value; period<160ms, it outputs equal duty pulse;
- Support pulse constant assignable; a total of 4 sets of pulse constant registers, of which HFONST4 is responsible for D2F00/03, HFONST5 is responsible for D2F01/04, HFONST6 is responsible for D2F02/05, and HFONST7 is responsible for D2F06~11;
- D2F00~D2F02 support automatic A-channel base wave active power integration, integration mode algebraic sum/forward/absolute/reverse is selectable (integration mode configuration is configured according to EMUCON5 register in EMU chapter), and output energy and pulse;
- D2F03~D2F05 support automatic B-channel base wave active power integration, integration mode algebraic sum/forward/absolute/reverse is selectable (integration mode configuration is configured according to EMUCON5 register in EMU chapter), and output energy and pulse;
- The power is a 32-bit signed number, i.e., the input range is ±2^31;
- Each integrator has its own interrupt status bit and interrupt enable bit;
- The mode of energy register can configure as accumulated or cleared after read type
- The integral clock is 32.768 KHz at the system clock 32.768 KHz; at other system clock frequencies, the integral clock is 921.6 KHz.

27.3 Usage Process

Software Processes:

1. Configure the MOD1_EN register D2F_EN bit to turn on the module clock;
2. Configure D2FCFG. d2f_disable=0 to enable the D2F module;
3. Configure the energy register type D2FCFG. eregCAR on demand;
4. Configure the D2F interrupt enable and pulse output port as required;
5. Configure the pulse constant register HFConstx;
6. Configure the D2FPxx as required to start the D2Fxx integrator.

Application 1: Customizing Power and Energy

The software fills the 32bit power value into D2FP00~D2FP11 registers, D2FPx is in binary complement format, the actual calculation of electrical energy hardware all transferred to the positive power calculation, the positive and negative direction of the electrical energy needs to be judged by the software itself; the D2F module integrates in accordance with the integration clock, and outputs the energy, pulses and interrupts.

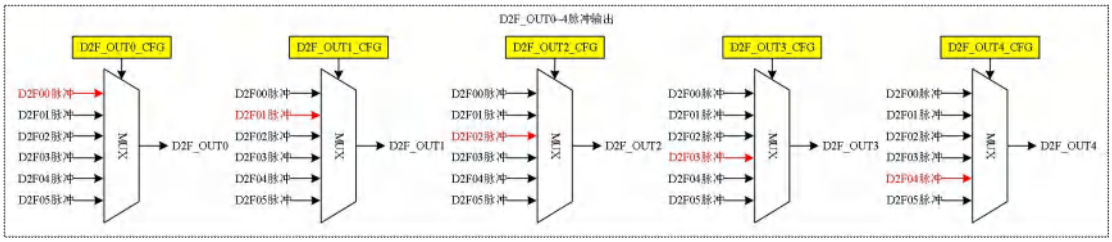
Application 2: Automatic output of base wave active energy

Configure HFConst4/5/6, configure EMUCON5.FPx_MOD to select the energy accrual method.

Configure EMUCON5.FEPx_AutoCalc=1 to enable the automatic output function of base wave active power, the hardware can automatically read the value of 32bit SPL_FPx register and fill it into D2FPx register to integrate according to the configured accumulation method, and output the power and pulse.

Note: The corresponding D2FPx in this mode does not support manual writing by software.

Customized D2F pulse output schematic:



27.4 Register list

base address	0x4005C000				
offset address	**Name**	**R/W**	**effective word length**	**reset value**	**Functional Description**
0x0	HFConst4	R/W	2	0x0	High Frequency Pulse Constant Register for D2F00/03
0x4	HFConst5	R/W	2	0x0	High Frequency Pulse Constant Register for D2F01/04
0x8	HFConst6	R/W	2	0x0	High Frequency Pulse Constant Register for D2F02/05
0xC	HFConst7	R/W	2	0x0	High frequency pulse constant register for D2F06~11
0x10	D2FCFG	R/W	1	0x0	D2F Configuration Register
0x14	D2FOUT_CFG	R/W	3	0x43210	Customizing the D2F Pulse Output Configuration Registers
0x18	IE	R/W	2	0x0	D2F Interrupt Enable Register
0x1C	IF	R/W	2	0x0	D2F Interrupt Flag Register
0x20~0x4C	D2FFCnt00~ D2FFCnt11	R/W	2	0x0	D2F Fast Pulse Counter
0x50~0x7C	D2FP00~D2FP11	R/W	4	0x0	D2F Power Input Register
0x80~0xAC	D2FE00~D2FE11	R	3	0x0	D2F Custom Energy Register

Note: The module registers do not support bitband operations.

27.5 Register Definition

27.5.1 Customize D2F high-frequency pulse constant registers HFConst4/5/6(0x00~0C)

D2F High Frequency Pulse Constant Register

Offset Address：00H；Word Length：4 bytes；Default Value：0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	HFConst4	Customize the pulse constants for power registers D2FE00/03 and custom pulses D2F_OUT0/D2F_OUT3. The HF pulse constant registers are 16-bit unsigned numbers.	R/W	0

Offset address：04H；Word length: 4 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	HFConst5	Customize the pulse constants for power registers D2FE01/04 and custom pulses D2F_OUT1/D2F_OUT4. The HF pulse constant registers are 16-bit unsigned numbers.	R/W	0

Offset address: 08H; Word length: 4 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	HFConst6	Customize the pulse constants for power registers D2FE02/05 and custom pulses D2F_OUT2/D2F_OUT5. The HF pulse constant registers are 16-bit unsigned numbers.	R/W	0

Offset address: 0CH; Word length: 4 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	R	0
15:0	HFConst7	Customize the pulse constants of the electrical energy registers D2FE06~11. The high frequency pulse constant register is a 16-bit unsigned number.	R/W	0

HFConst4/5/6/7 are the pulse constants of 12 customized electrical energy registers D2FE00-D2FE11 and 6 customized pulses D2F_OUT0~D2F_OUT5, the correspondence is shown in the table above.

The high frequency pulse constant register is a 16-bit unsigned number.

The clock for the D2F integration of the metering channel is 921.6 KHz, and the clock for the custom D2F integration is also 921.6 KHz;

If you want to ensure that the custom D2F and the metering channel have the same pulse rate out of the meter, assuming that the meter pulse constants EC are defined exactly the same for both, then you have to satisfy that the HFConst registers for both are the same.

Directly read the chip's power register value (32bit, e.g. PA, etc.), fill in the power register D2FP, and then the pulse output D2F_OUT can be aligned with the corresponding pulse output speed of the chip's metering channel.

If the defined pulse constants are different, both by adjusting the HFConst and customizing the power register fill values are possible.

27.5.2 Custom D2F Configuration Register D2FCFG(0x10)

D2F Configuration Register

Offset address: 10H; Word length: 1 byte; Default value: 0x2

Bit	Name	Description	R/W	Reset Value
31:2	Reserved	Reserved	R	0
1	D2F_DISABLE	D2F module enable =0, enable D2F module =1, resets all counters and number arithmetic units without resetting register values. The default value is 1.When starting the integration, the bit should be configurated to 0 first, and then keep the bit at 0, and write the D2FP register directly to start the integration immediately.	R/W	1
0	ERegCAR	Energy register type select. ＝0, cleared after read. ＝1, cumulative type. The default value is 0。	R/W	0

27.5.3 Custom D2F Pulse Output Configuration Register D2FOUT_CFG(0x14)

Customizing the D2F Pulse Output Configuration Registers

Offset address: 14H; Word length: 3 bytes; Default value: 0x43210

Bit	Name	Description	R/W	Reset Value
31:19	Reserved	Reserved	R	0
18:16	D2F_OUT1_CFG	Pulse type selection register for D2F_OUT1 output, with the same configuration options as D2F_OUT0_CFG, default output D2F01 pulse.	R/W	100
15	Reserved	Reserved	R	0
14:12	D2F_OUT1_CFG	Pulse type selection register for D2F_OUT1 output, with the same configuration options as D2F_OUT0_CFG, default output D2F01 pulse.	R/W	011
11	Reserved	Reserved	R	0
10:8	D2F_OUT1_CFG	Pulse type selection register for D2F_OUT1 output, with the same configuration options as D2F_OUT0_CFG, default output D2F01 pulse.	R/W	010
7	Reserved	Reserved	R	0
6:4	D2F_OUT1_CFG	Pulse type selection register for D2F_OUT1	R/W	001

		output, with the same configuration options as D2F_OUT0_CFG, default output D2F01 pulse.		
3	Reserved	Reserved	R	0
2:0	D2F_OUT0_CFG	Pulse type selection register for D2F_OUT0 output: = 000, D2F00 pulses; = 001, D2F01 pulses; = 010, D2F02 pulse; = 011, D2F03 pulse; = 100, D2F04 pulse; = 101, D2F05 pulse; = Other, reserved.	R/W	000

27.5.4 Customized D2F interrupt enable register IE(0x18)

D2F Interrupt Enable Register

Offset Address: 18H; Word Length: 2 bytes; Default Value: 0x0

Bit	Name	Description	R/W	Reset Value
31:12	Reserved	Reserved	R	0
11	D2F11IE	Energy integral unit D2F11 interrupt enable	R/W	0
10	D2F10IE	Energy integral unit D2F10 interrupt enable	R/W	0
9	D2F09IE	Energy integral unit D2F9 interrupt enable	R/W	0
8	D2F08IE	Energy integral unit D2F8 interrupt enable	R/W	0
7	D2F07IE	Energy integral unit D2F7 interrupt enable	R/W	0
6	D2F06IE	Energy integral unit D2F6 interrupt enable	R/W	0
5	D2F05IE	Energy integral unit D2F5 interrupt enable	R/W	0
4	D2F04IE	Energy integral unit D2F4 interrupt enable	R/W	0
3	D2F03IE	Energy integral unit D2F3 interrupt enable	R/W	0
2	D2F02IE	Energy integral unit D2F2 interrupt enable	R/W	0
1	D2F01IE	Energy integral unit D2F1 interrupt enable	R/W	0
0	D2F00IE	Energy integral unit D2F0 interrupt enable	R/W	0

This register is the D2F interrupt enable register. When this event occurs, the corresponding D2FIF is set and a D2F interrupt is generated if configured to 1 in the corresponding interrupt allow bit. Interrupt number 4.

27.5.5 Custom D2F Interrupt Flag Register IF(0x1C)

D2F Interrupt Flag Register

Offset address: 1CH; Word length: 2 bytes; Default value: 0x0

Bit	Name	Description	R/W	Reset Value
31:12	Reserved	Reserved	R	0
11	D2F11IF	Energy integral unit D2F11 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0

10	D2F10IF	Energy integral unit D2F10 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
9	D2F09IF	Energy integral unit D2F9 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
8	D2F08IF	Energy integral unit D2F8 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
7	D2F07IF	Energy integral unit D2F7 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
6	D2F06IF	Energy integral unit D2F6 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
5	D2F05IF	Energy integral unit D2F5 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
4	D2F04IF	Energy integral unit D2F4 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
3	D2F03IF	Energy integral unit D2F3 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
2	D2F02IF	Energy integral unit D2F2 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
1	D2F01IF	Energy integral unit D2F1 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0
0	D2F00IF	Energy integral unit D2F0 energy pluse flag. Write 1 and cleared.If the corresponding bit is D2FIE=1, cleared and clear the interrupt at the same time.	R/W	0

This register is the D2F event status register, and when the D2FE energy register is added to 1, the corresponding flag bit is set to 1. When the corresponding interrupt allow bit is configured to 1, the status position 1 causes the generation of CPU EMU interrupt 1.

27.5.6 Customized D2F Fast Pulse Counter (0x20~0x4C)

Offset address	20H	24H	28H	2CH	30H	34H
Register	D2FFCnt00	D2FFCnt01	D2FFCnt02	D2FFCnt03	D2FFCnt04	D2FFCnt05
Default	0x0	0x0	0x0	0x0	0x0	0x0

Offset address	38H	3CH	40H	44H	48H	4CH
Register	D2FFCnt06	D2FFCnt07	D2FFCnt08	D2FFCnt09	D2FFCnt10	D2FFCnt11
Default	0x0	0x0	0x0	0x0	0x0	0x0

The fast pulse counter register is a 2-byte unsigned number that is readable and writable.

When two times the absolute value of the count value of the fast pulse count register D2FFCntx is greater than or equal to the corresponding HFConst, there will be a pulse overflow accordingly, and the value of the energy register will be increased by 1 accordingly.

27.5.7 Customize D2F power register (0x50~0x6C)

Offset address	50H	54H	58H	5CH	60H	64H
Register	D2FP00	D2FP01	D2FP02	D2FP03	D2FP04	D2FP05
Default	0x0	0x0	0x0	0x0	0x0	0x0
Offset address	68H	6CH	70H	74H	78H	7CH
Register	D2FP06	D2FP07	D2FP08	D2FP09	D2FP10	D2FP11
Default	0x0	0x0	0x0	0x0	0x0	0x0

The power input registers D2FP00- D2FP11 are in binary complement format, 32-bit signed numbers where the highest bit is the sign bit, and can be read and written.

When the power value is written to the D2FP register, the power will be integrated according to the corresponding pulse constant HFConst, and the integrated power is stored in the D2FE00~D2FE11 registers, in which D2FE00~D2FE05 can output pulses, and the corresponding pulses are D2F_OUT0~D2F_OUT5, respectively, which can be configured from the IO ports according to the GPIO multiplexed configuration. Output. The pulses are held at a fixed high level for 80ms according to the meter requirements, and the low level is varied according to the period value; if the period is less than 160ms, then equal duty pulses are output.

27.5.8 Customized D2F Energy Register (0x80~0xAC)

Offset address	80H	84H	88H	8CH	90H	94H
Register	D2FE00	D2FE01	D2FE02	D2FE03	D2FE04	D2FE05
Default	0x0	0x0	0x0	0x0	0x0	0x0

Offset address	98H	9CH	A0H	A4H	A8H	ACH
Register	D2FE06	D2FE07	D2FE08	D2FE09	D2FE10	D2FE11
Default	0x0	0x0	0x0	0x0	0x0	0x0

The customized electrical energy parameters are 24bit unsigned numbers, read-only, representing the number of accumulations of the corresponding pulse. The energy represented by the smallest unit of the register is 1/EC kWh, where EC is the meter constant.

The energy register overflows from 0xFFFFFF to 0x000000, which is managed by the user's software at its own discretion, and is not handled by the hardware.

The custom energy register can be selected to be either cumulative or clear-after-read, and is controlled by the D2FCFG configuration register.

28 Measurement Error Temperature Compensation Module ECT (new)

28.1 Overview

The main factors affecting the temperature characteristics of whole meter metering accuracy include:

- Current sampling circuits (manganese copper, current transformers and sampling resistors, etc.)
- Voltage sampling circuits (resistor column divider, voltage transformer, etc.)
- ADC Temperature Coefficient
- Temperature coefficient of reference voltage, etc.

The temperature characteristics of the measurement accuracy of the whole meter are synthesized by the above factors, and experience has shown that under the conditions of fixed external sampling circuit and ADC, it is difficult to obtain a refined and ideal temperature compensation curve by single optimization of the temperature coefficient of the reference voltage Trim value. In practical applications, the actual measurement of the entire meter temperature curve, calibrated segmented linear fitting K coefficient, on-site temperature measurement, real-time software calculations and adjust the error compensation gain coefficient method.

The main purpose of the ETC (Error Temprature Compensate) module is to solve the above problem, by measuring the temperature at regular intervals and updating the gain registers of the metering channels in real time to achieve the effect of automatic temperature compensation. The K coefficients described above are calibrated by the software and configured to the ETC module for better metering accuracy.

28.2 Calculation formula for temperature compensation gain coefficient

Knowing that the error temperature compensation linear fit coefficient for the high temperature section is HT_KI and the measured temperature is T, find the formula for the error temperature compensation gain co efficient HT_IGAIN.

Phase A current as an example, high temperature section error temperature compensation linear fitting co efficient for HT_KIA, current through the error temperature compensation gain before I, gain compensation af ter I', error temperature compensation gain coefficient for: HT_IAGAIN, compensation formula for:

$$I'=I(1+ETCHT\_IAGAIN)=\frac{I}{1+INF_{HT\_T'}}=\frac{I}{1+HT\_KIA(T'-25℃)}$$

Following the above equation can be deduced:

$$ETCHT\_IAGAIN=\frac{-HT\_KIA(T'-25℃)}{1+HT\_KIA(T'-25℃)}$$

Similarly the low temperature section error temperature compensation gain can be obtained:

$$ETCLT\_IAGAIN=\frac{-LT\_KIA(T'-25℃)}{1+LT\_KIA(T'-25℃)}$$

Voltage channels are in order.

28.3 Specificities

- Supports automatic temperature compensation for U/IA/IB 3-channel errors
- Each channel has independent compensation coefficients for high and low temperature sections
- Three working modes are supported:
  - Manual mode, CPU writes gains directly

- Single auto mode, cpu configured temperature value for temperature compensation
- Cyclic automatic mode, can realize timed temperature compensation throughout the software without intervention

- Cyclic automatic mode temperature compensation period 1s-256s configurable
- Support temperature anti-shaking function, the temperature compensation gain coefficient calculation will be activated only when |temperature difference between two measurements| > the set temperature threshold.
- Supports temperature protection near 25° C, and the temperature protection zone is configurable
- Support temperature overrun protection function, temperature compensation lower limit and upper limit can be configured, optional temperature compensation calculation and update ECT temperature compensation gain register when temperature overrun.
- Support error overrun protection function, error overrun threshold can be configured, support error overrun alarm interrupt, overrun temperature gain coefficient is not updated to EMU channel temperature gain coefficient register.
- Supports ECT temperature-compensated gain coefficient update interrupts

28.4 Functional Description

28.4.1 functional block diagram

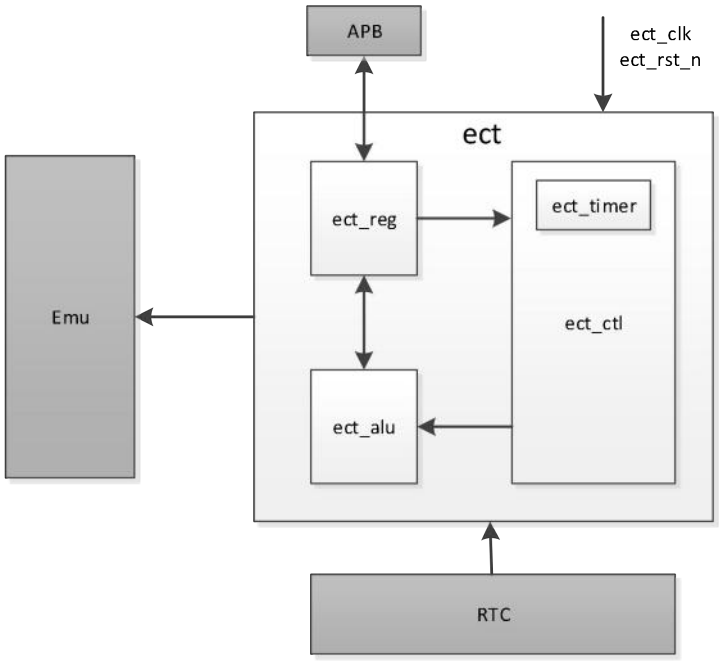


Figure ECT Functional Block Diagram

as shown in the figure, ECT（Error Temprature Compensation）module include：

Ect_reg: register module

Ect_ctl: High and low temperature judgment, threshold judgment, error judgment, etc.

Ect_alu：gain calculation unit

28.4.2 Operating mode

ECT supports three operating modes: manual mode, single automatic mode, and cyclic automatic mode. The three operating modes correspond to different workflow and software control methods.

- **Manual mode**
  1) CPU reads the temperature value from the RTC ->
  2) Software calculates gain->
  3) Software fills the TEMP_UD and XXGAIN registers

  Note: The hardware is not labeled to indicate manual mode, except that the TEMP_UD and XXGAIN registers are left with CPU-configurable options
- **Single automatic mode**
  1) CPU fill temperature value ->
  2) Temperature protection event judgment and processing->
  3) High Temperature Segment Low Temperature Segment Judgment->
  4) Temperature overrun event judgment and treatment->
  5) Temperature stabilization, temperature threshold and startup calculation unit judgment->
  6) Start the calculation unit to complete the calculation of the temperature complementary gain coefficient->
  7) Error out-of-bounds event judgment and interrupt output->
  8) ECT Temperature Complementary Gain Coefficient Register Update ->
  9) TEMP_UD output
- **Cyclic automatic mode**

  Automatic temperature reading from RTC -> Event processing -> Calculate gain

  ECT starts the ECT_Timer timer, and ECT cycles the above process week by week at the period set by ECT_Timer_SET.

  The difference with the single automatic is the temperature source is different, the single automatic temperature value needs to be written into the register by the CPU, while the cycle automatic is to get the temperature value from the RTC automatically.

28.4.3 Temperature protection

When the PROT_EN=1 temperature protection function of the CTRL register is turned on, if the absolute temperature value obtained by subtracting 25° C from the detected temperature is less than the 25° C temperature protection threshold set in the PROT_TEMP register, then the automatic temperature compensation temperature protection event is triggered, i.e.

|TEMP - 25°C| < PROT_TEMP , triggers an automatic warming temperature protection event.

ECT stops the calculation of the automatic temperature complement coefficients after This event occurs and clears all gain coefficient xxGAIN registers to zero with the TEMP_PROT_IF flag set.

If the clearing action causes an update of xxGAIN to occur, TEMP_UD is also updated to the current detected temperature value and the corresponding channel flags of GAINUD[2:0] are set.

28.4.4 High and low temperature segmentation judgment

If no temperature protection event occurs, the control unit next makes a high and low temperature segment judgment, again compared to 25° C.

Temperature <25 ℃ , judged as low temperature section, the subsequent process uses a set of registers and judgment criteria for low temperature section, including low temperature section K coefficient register, low temperature crossing threshold register LT_LL, low temperature section temperature threshold register LT_GAP.

Temperature ≥ 25° C is judged to be a high temperature section, and the subsequent process uses a set of registers and judgment criteria for the high temperature section, including the high temperature section K coefficient

register, the high temperature crossing threshold register HT_LL, and the low temperature section temperature threshold register HT_GAP.

28.4.5 Temperature out-of-bounds event handling

After the high-temperature section and low-temperature section are determined, the control unit will next carry out the temperature crossing event judgment and processing.

Temperature overrun event is defined as follows: In auto-temperature compensation mode, when CTRL register TEMPEL_PORT_ EN=1, temperature overrun protection function is turned on, and the temperature overrun event occurs when TEMP > upper limit of auto-temperature compensation temperature set by HT_UL or TEMP < lower limit of auto-temperature compensation temperature set by LT_LL, the flag bit TEMP_EL_IF will be set.

When a temperature overrun event occurs, the CTRL register TEMPEL_GAINCAL_EN bit can be used to select whether or not to stop the calculation of the automatic next temperature compensation coefficient.

If TEMPEL_GAINCAL_EN=1, the next step of temperature threshold determination will be initiated;

If TEMPEL_GAINCAL_EN=0, the round of warming is over.

28.4.6 Temperature stabilization

The temperature threshold judgment function is activated if no temperature protection and temperature overrun event occurs, or if a temperature crossing event occurs but TEMPEL_GAINCAL_EN=1.

When the absolute value of the current temperature minus the last updated temperature value is greater than or equal to the temperature setting threshold for the low or high temperature section, the ECT calculation unit is activated to calculate the temperature complementary coefficient, i.e.

|TEMP - TEMP_UD| ≥ LT_GAP/HT_GAP, it meets the calculation conditions and starts the ECT calculation unit to calculate the temperature gain coefficient of the temperature section of the warming patch, and after the calculation is completed, it carries out the judgment of error out-of-bounds event and processing. Otherwise, this round of temperature compensation ends.

28.4.7 Gain factor calculation

$$\mathrm{ECT\_TxGAIN} = \frac{-LT\_KIx * (T - 25)}{1 + LT\_KIx * (T - 25)}$$

LT_KIx is the low-temperature segment Ix channel error automatic temperature compensation linear fitting coefficient, see the LT_KIx register description; T is the measured temperature value TEMP of this compensation. High-temperature segment use high-temperature segment compensation K coefficient HT_KIx.

28.4.8 Error out-of-bounds event handling

When the temperature complement error protection function is turned on, if the gain coefficient of a channel's high temperature section or low temperature section calculated by the calculation module exceeds the threshold set by PROT_xxGAIN, an error out-of-bounds event occurs for that channel.

When an error out-of-bounds event occurs on a channel, the error out-of-bounds flag ERR_EL_xx is set for that channel. Any one bit flag set will cause ERREL_IF to be set, and if the ERREL_IE interrupt is enabled, any one bit flag set will generate an ERREL_IF interrupt, clear the interrupt, and will clear the ERR_EL_xx flag bit.

28.5 Register description

28.5.1 Register list

Module name	Physical address	Mapping address
ECT	0x40078000	0x40078000
Register name	**Address offset**	**Descriptive**
WREN	Offset+0x0	Write Enable Register

CTRL	Offset+0x4	Control register
EN	Offset+0x8	Module Enable Register
STATUS	Offset+0xC	Status register
IE	Offset+0x10	Interrupt Enable Register
LT_SET	Offset+0x14	Low Temperature Segment Threshold Configuration Register
HT_SET	Offset+0x18	High Temperature Segment Threshold Configuration Register
TIMER_SET	Offset+0x1C	Cycle period Configuration Register
PROT_TEMP	Offset+0x20	25 ° C Temperature Protection Threshold Configuration Register
PROT_IAGAIN	Offset+0x24	IA Channel Error Protection Threshold Registers
PROT_IBGAIN	Offset+0x28	IB Channel Error Protection Threshold Registers
PROT_UGAIN	Offset+0x2C	U-channel error protection threshold registers
LT_KIA	Offset+0x30	Low Temperature Section IA Channel K-Factor Registers
LT_KIB	Offset+0x34	Low Temperature Section IB Channel K-Factor Registers
LT_KU	Offset+0x38	K-factor register for U-channel in low-temperature section
HT_KIA	Offset+0x3C	High Temperature Section IA Channel K-Factor Registers
HT_KIB	Offset+0x40	High temperature section IB channel K-factor registers
HT_KU	Offset+0x44	High temperature section U-channel K-factor register
TEMP	Offset+0x48	Current Temperature Register
IAGAIN	Offset+0x4C	IA Channel Gain Compensation Register
IBGAIN	Offset+0x50	IB Channel Gain Compensation Register
UGAIN	Offset+0x54	U-channel gain compensation register
TEMP_UD	Offset+0x58	Temperature register for current compensation

28.5.2 WREN（0x0）

Configuring the Write Enable Register

Bit	Name	Description	R/W	Reset

				Value
31:8	reserved	Reserved bit	R/W	0
7:0	WREN	Write enable for other registers; Write 0xEA, the rest of the registers are writable; write other values are not writable	R/W	0

28.5.3 CTRL（0x4）

Control register

Bit	Name	Description	R/W	Reset Value
31:8	Reserved	Reserved	RO	0
7	TEMPEL_PORT_ EN	0: Temperature overrun protection is disabled 1: Enable the temperature overrun protection function	R/W	0
6	TEMPEL_GAINCAL_EN	0: Temperature overrun event occurs, the calculation engine does not calculate the temperature complementary gain coefficient and only reports the temperature crossing event. 1: Temperature out-of-bounds event occurs, not only the temperature out-of-bounds event is reported, but also the calculation engine is started to calculate the temperature complementary gain coefficient and write it to the corresponding temperature complementary gain coefficient register, and trigger the GAIN_UD flag to be set. Note: This configuration bit is only valid when TEMPEL_PORT_ EN=1.	R/W	0
5	ERREL_PROT_EN	0: Disable the protection function of temperature compensation error overruns 1：Enable the protection function of temperature compensation error overruns	R/W	0
4	PORT_EN	0: Disables the temperature compensation temperature zone protection function. 1: Enable the temperature compensation temperature zone protection function. The bit is mainly protected to remain stable near 25° C.	R/W	0
3:1	CH_SEL	Automatic temperature compensation channel selection configuration: CH_SEL[2:0] corresponds to U, IB and IA channels. 0: {IA,IB,U} channel auto-temperature compensation is not selected. 1: Select {IA,IB,U} channel auto-tempering	R/W	0

0	MODE	Automatic temperature compensation mode configuration: 0：Single Automatic temperature compensation mode ECT_TEMP register is readable and writable, the CPU writes the temperature for a single automatic temperature compensation，if the temperature compensation conditions are met, the temperature compensation gain register is automatically adjusted in a single pass. 1：Cyclic automatic temperature compensation mode; The temperature value is automatically read from the RTC to cycle the temperature compensation according to the period set in the ECT_Timer_SET register. if the temperature compensation conditions are met, the temperature compensation gain register period is automatically adjusted.	R/W	0

28.5.4 EN（0x8）

Module Enable Register

Bit	Name	Description	R/W	Reset Value
31:8	reserved	Reserved	R/W	0
15:0	EN	Write enable for the remaining registers; Write 0x685E to enable ECT temperature compensation Write other, disable ECT temperature compensation	R/W	0

28.5.5 STATUS（0xC）

Status register

Bit	Name	Description	R/W	Reset Value
31:11	Reserved	Reserved	R	0
10	ERR_EL_U	U-channel automatic temperature compensation error out-of-bounds status bit	R	0
9	ERR_EL_IB	IB channel automatic temperature compensation error out-of-bounds status bit	R	0
8	ERR_EL_IA	IA channel automatic temperature compensation error out-of-bounds status bit	R	0
7	GAINUD_U	U-channel gain factor update flag	R	0
6	GAINUD_IB	IB channel gain factor update flag	R	0
5	GAINUD_IA	IA channel gain factor update flag	R	0
5	TEMP_JIT_IF	Temperature jitter interrupt flag, write 1 to clear it	RW1C	0
4	TEMP_EL_IF	Temperature out-of-bounds interrupt flag, write 1 to clear it	RW1C	0
3	TEMP_PROT_IF	Temperature protection interrupt flag, write 1 to clear	RW1C	0
2	DONE_IF	Auto-Tempering complete round of gain calculation interrupt flag, write 1 to clear	RW1C	0

1	ERREL_IF	Gain error out-of-bounds interrupt flag, write 1 to clear the interrupt, clearing the interrupt will also request the ERR_EL_XX flag bit.	RW1C	0
0	GAINUD_IF	Temperature compensated gain factor update interrupt flag, clear by writing 1	RW1C	0

28.5.6 IE（0x10）

Interrupt Enable Register

Bit	Name	Description	R/W	Reset Value
31:6	Reserved	Reserved	R	0
5	TEMP_JIT_IE	Temperature jitter interrupt enable	RW	0
4	TEMP_EL_IE	Temperature out-of-bounds interrupt enable	RW	0
3	TEMP_PROT_IE	Temperature protection interrupt enable	RW	0
2	DONE_IE	Auto-tempering complete round of gain calculation interrupt enable	RW	0
1	ERREL_IE	Gain error out-of-bounds interrupt enable	RW	0
0	GAINUD_IE	Temperature-complementary gain factor update interrupt enable	RW	0

28.5.7 LT_SET（0x14）

Low Temperature Segment Threshold Configuration Register

Bit	Name	Description	R/W	Reset Value
31:26	Reserved	Reserved	RO	0
25:16	LT_LL	Temperature lower limit value configuration for error temperature compensation in low temperature section (<25℃ is low temperature section, the same below).TEMP_EL enable, the detection temperature is lower than this temperature point, the automatic temperature compensation temperature out of bounds event occurs. This register is a binary signed number, with the highest bit being the sign bit, and is configured to scale as low as 0.25° C. The default is -40°C. The default is -40° C.	R/W	0x360
15:10	Reserved	Reserved	R/W	0
9:0	LT_GAP	When the detection temperature is in the low-temperature segment (<25° C), the threshold temperature set by |TEMP - TEMP_UD| ≥ LT_GAP is satisfied, and automatic temperature compensation is activated. Configure the minimum for the scale to be 0.25° C. The default is 5° C.	R/W	0x14

28.5.8 HT_SET（0x18）

High Temperature Segment Threshold Configuration Register 器

Bit	Name	Description	R/W	Reset Value
31:26	Reserved	Reserved	RO	0
25:16	HT_UL	High temperature section (≥ 25 ℃ for high temperature section, the same below) error temperature compensation of the temperature upper limit value configuration, if TEMP_EL enable, the detection temperature is higher than the temperature point, the automatic temperature compensation temperature overrun event occurs. This register is a binary signed number, the highest bit is the sign bit, the configuration of the minimum for the scale of 0.25 ℃, the default value of 85 ℃.	R/W	0x154
15:10	Reserved	Reserved	R/W	0
9:0	HT_GAP	When the detection temperature is in the high temperature range (≥25° C), automatic temperature compensation is activated when the threshold temperature set by |TEMP - TEMP_UD |≥ HT_GAP is satisfied. Configure the minimum for the scale to be 0.25° C. The default is 5° C.	R/W	0x14

28.5.9 TIMER_SET（0x1C）

Cycle Period Configuration Register

Bit	Name	Description	R/W	Reset Value
31:8	Reserved	Reserved	RO	0
7:0	Timer_Cyc	Unit: s. After starting cyclic auto temperature compensation, the auto temperature compensation unit detects the temperature at regular intervals of (Timer_Cyc + 1)s. Default value: 0x9. Maximum setting is 256s.	R/W	0x9

28.5.10 PROT_TEMP（0x20）

25℃ Temperature Protection Threshold Configuration Register

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	RO	0
9:0	PROT_TEMP	Automatic Temperature Complementary Temperature Protection Area Setting. When PORT_EN is enabled, if |TEMP - 25°C| < Protection Temperature Threshold set by PROT_TEMP, the Auto Temperature Complementary Temperature Protection	R/W	0x8

		event is triggered. Configure the minimum for a scale of 0.25° C. The default setting is at 2° C		

28.5.11 PROT_IAGAIN（0x24）

IA channel error protection threshold registers

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	PROT_IAGAIN	Automatic temperature compensation error protection threshold setting. When the absolute value of the IA channel compensated current channel gain coefficient is greater than the set threshold, i.e., |IAGAIN| > PROT_IAGAIN, a temperature compensation error crossing event occurs for that current channel. It is typically set at 1%*2^15.	R/W	0x147

28.5.12 PROT_IBGAIN（0x28）

IB Channel Error Protection Threshold Registers

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	PROT_IBGAIN	Automatic temperature compensation error protection threshold setting. When the absolute value of the current channel gain coefficient compensated by the IB channel is greater than the set threshold, i.e., |IBGAIN| > PROT_IBGAIN, a temperature compensation error overrun event occurs for that current channel. It is typically set at 1%*2^15.	R/W	0x147

28.5.13 PROT_UGAIN（0x2C）

U-channel error protection threshold registers

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	PRO_UGAIN	Voltage channel automatic warm-up error protection threshold setting. When the absolute value of the current channel gain coefficient compensated by the U-channel is greater than	R/W	0x147

		the set threshold, i.e., |UGAIN| > PROT_UGAIN, a temperature compensation error overrun event occurs for that voltage channel. Generally set at 1%*2^15.		

28.5.14 LT_KIA（0x30）

Low Temperature Section IA Channel K-Factor Registers

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	LT_KIA	LT_KIA register for the linear fit coefficient of the temperature complement of the IA channel error in the low-temperature section. According to the user in the school table stage measured Ix channel characteristics of the low-temperature section, to find the value, and written to the EEPROM to save, power-on, by the CPU to write the register. Current channel gain correction, scanning -40 ℃ ~25 ℃ nominal current temperature curve, take the most suitable once linear fit temperature point T ', measured 25 ℃ current value for Ix (25 ℃), the current value of the fit temperature T ' Ix (T '); so that the entire low-temperature section of the temperature curve away from the straight line spacing between the connection of Ix (25) and Ix (T ') to minimize, it is obtained The formula for LT_KIx: LT_KIx = ERR / (T'-25), where ERR = (Ix(T') - Ix(25° C)) / Ix(25° C) The highest bit is the sign bit, full scale is 0.022, and the default value is 0	R/W	0

28.5.15 LT_KIB（0x34）

Low Temperature Section IB Channel K-Factor Registers

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	LT_KIB	LT_KIB register for the low-temperature segment IB channel error temperature-compensated linear fit coefficients. The formula is the same as LT_KIA.	R/W	0

28.5.16 LT_KU（0x38）

K-factor register for U-channel in low-temperature section

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	LT_KU	LT_KU register for the linear fit coefficient of the temperature complement of the U-channel error in the low-temperature section. The formula is the same as LT_KIA.	R/W	0

28.5.17 HT_KIA（0x3C）

High Temperature Section IA Channel K-Factor Registers

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	HT_KIA	High Temperature Section IA Channel Error Temperature Compensation Linear Fit Coefficient HT_KIA register. According to the user in the school table stage measured the high temperature section characteristics of the Ix channel, to find the value, and written to the EEPROM to save, power on, by the CPU to write the register. After the current channel gain correction, scan the 25℃ ~85℃ nominal current temperature curve, take the most suitable one-time linear fitting temperature point T', measured 25℃ current value is Ix (25), the current value of the fitting temperature T' Ix (T'); so that the entire high temperature section temperature curve from Ix (25) and Ix (T') connected to the straight line with the smallest spacing, you get The formula for HT_KIx: HT_KIx = ERR / (T'-25), where ERR = (Ix(T') - Ix(25° C)) / Ix(25° C) The highest bit is the sign bit, full scale is 0.022, and the default value is 0	R/W	0

28.5.18 HT_KIB（0x40）

High temperature section IB channel K-factor registers

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	HT_KIB	High Temperature Section IB Channel Error Temperature Compensation Linear Fit Coefficient HT_KIB Register. The formula is the same as HT_KIA.	R/W	0

28.5.19 HT_KU（0x44）

High temperature section U-channel K-factor register

Bit	Name	Description	R/W	Reset Value
31:17	Reserved	Reserved	RO	0
16:0	HT_KU	HT_KU register for the linear fit coefficient of the temperature complement of the U-channel error in the high-temperature section. The formula is the same as HT_KIA.	R/W	0

28.5.20 TEMP（0x48）

Current temperature value register

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	RO	0
9:00	TEMP	1. This register holds the temperature value for this read from the RTC Binary complement representation, 10 valid bits, Bit9 is the sign bit; the minimum scale is 0.25 degrees. The conversion formula to actual temperature is: T = TEMP/4. 2. The user can fill in this temperature value for gain calculation via software in single-shot automatic mode.	R/W	0x9

28.5.21 IAGAIN（0x4C）

IA Channel Gain Compensation Register

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	IAGAIN	Temperature-compensated gain coefficients for the IA channel, after EMU metering channel gain correction. Calculation formula: Take the low-temperature segment, for example. IxGAIN = -LT_KIx * (T-25) / (1 + LT_KIx * (T-25)). Where LT_KIx is the linear fitting coefficient of the automatic temperature compensation for the Ix channel error in the low temperature section, and T is the measured temperature value for this compensation. The high temperature section uses the high temperature section compensation K factor HT_KIx with the same formula. Whether to use the high or low temperature range is automatically determined by the hardware. The highest bit is the sign bit, the full scale is 1, the default value is 0.	R/W	0

28.5.22 IBGAIN（0x50）

IB Channel Gain Compensation Register

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	IBGAIN	Temperature-compensated gain coefficients for the IB channel, after EMU metering channel gain correction. The formula is the same as IAGAIN. The highest bit is the sign bit, the full scale is 1, and the default value is 0.	R/W	0

28.5.23 UGAIN（0x54）

U-channel gain compensation register

Bit	Name	Description	R/W	Reset Value
31:16	Reserved	Reserved	RO	0
15:0	UGAIN	Temperature-compensated gain coefficients for the U-channel, after EMU metering channel gain correction. The formula is the same as IAGAIN. The highest bit is the sign bit, the full scale is 1, and the default value is 0.	R/W	0

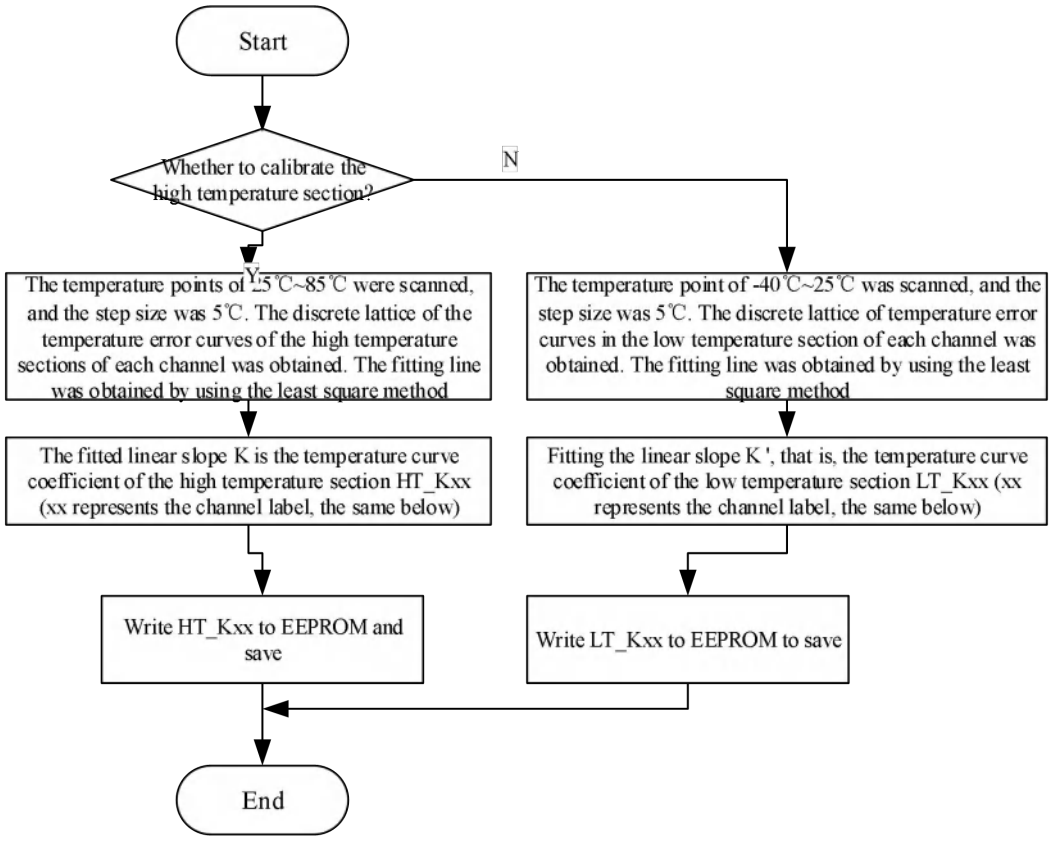
28.5.24 TEMP_UD（0x58）

Temperature register for current compensation

Bit	Name	Description	R/W	Reset Value
31:10	Reserved	Reserved	RO	0
9:00	TEMP_UD	This register holds the most recent update to the temperature compensation coefficient register group temperature value. Single and cyclic automatic temperature compensation modes are automatically written by the ECT after updating the temperature compensation coefficient register set. For manual mode, this register is filled in by software.	R/W	0x64

28.6 Application process

28.6.1 Temperature compensation K-factor calibration



28.6.2 Manual temperature compensation mode

1. The user obtains a discrete curve of "Temperature effect of RMS relative to 25°C (%) - Temperatur e" by taking several temperature measurements;
2. Divide the high and low temperature segments according to the 25°C demarcation, and do the li near fitting of the high and low temperature segments based on the discrete points measured in ste p 1, and the formula for the fitting coefficient, K, is calculated as follows:

$$K=\frac{\sum_{i=1}^{n} y_i(x_i-25)}{\sum_{i=1}^{n}(x_i-25)^2}$$

3. The user gets the temperature value by reading RTC_TEMP and determines the error temperature compensation gain coefficient based on the high and low temperature segment division and the corresponding temperature compensation linear fitting coefficient K;
4. Fill in the TEMP_UD register and the xxGAIN register;

Continue to manually temperature compensation and repeat steps 3 to 4.

28.6.3 Single automatic temperature compensation mode

1、 Configure CH_SEL to enable U/IB/IA which channel is automatically temperature compensation;
2、 Configure MODE=0 to select the temperature compensation mode as single automatic temperature c

ompensation mode;

3、 Configure the LT_SET/HT_SET registers to configure the high and low temperature segment thresholds;

4、 Configure the corresponding protected area setting registers PROT_TEMP/PROT_xxGAIN;

5、 Configure the appropriate event interrupt;

6、 Enter the calibrated temperature complementary linear fit K coefficients into the LT_Kxx/HT_Kxx registers;

7、 Configure EN=0x685e to initiate ECT temperature compensation;

8、 Query the DONE_IF flag, when DONE_IF is set to 1, a round of temperature compensated gain coefficient calculation is completed, and the ECT module returns to standby status;

28.6.4 Cyclic automatic temperature compensation mode

1、 Configure CH_SEL to enable U/IB/IA which channel is automatically temperature compensation;

2、 Configure MODE=1 to select the temperature compensation mode as cyclic automatic temperature c ompensation mode;

3、 Configure the LT_SET/HT_SET registers to configure the high and low temperature segment thresholds;

4、 Configure Timer_SET to set the automatic cyclic temperature compensation period;;

5、 Configure the corresponding protected area setup registers PROT_TEMP/PROT_xxGAIN;

6、 Configure the appropriate event interrupt;

7、 Enter the calibrated temperature complementary linear fit K coefficients into the LT_Kxx/HT_Kxx registers.

8、 Configure EN=0x685e to initiate ECT temperature compensation;

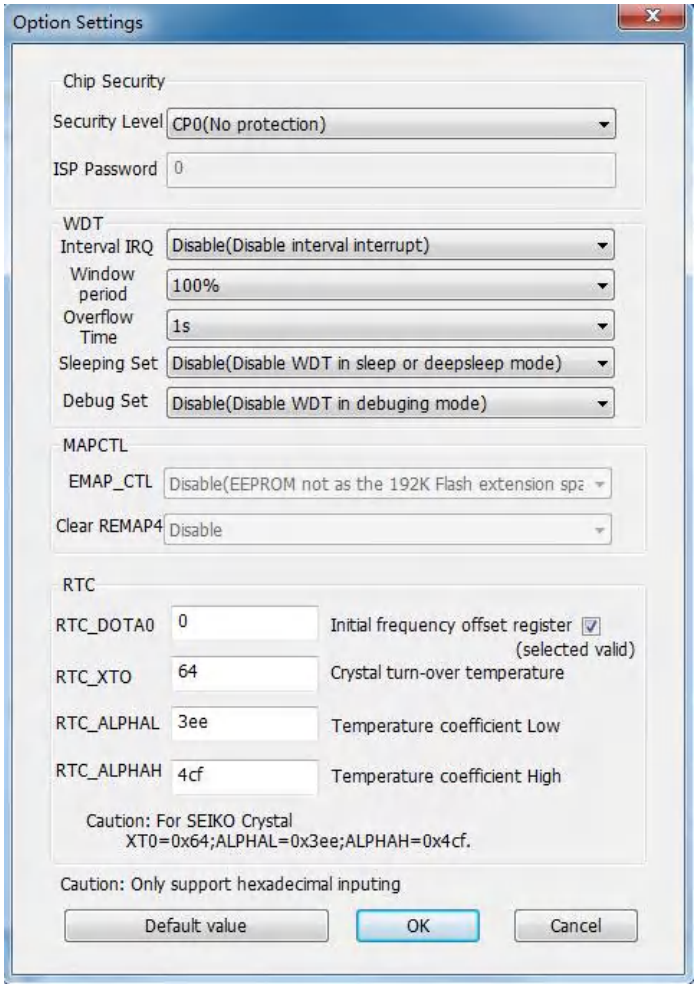
9、 Query the DONE_IF flag, and when DONE_IF is set to 1, complete one round of temperature com pensated gain coefficient calculation;

10、Start the calculation of the next temperature compensation gain coefficient according to the Timer_S ET setting period.

29 Option Byte

It built in an area of option byte, when the chip is reset, it will automatically configure option byte and perform specific function. Option byte includes protection of the chip, WDT, EMAP and RTC setting.

Programming of option byte can be setting by the programming tool from Renergy (MINIPRO programming unit or ISP programming tools), Taking the MINIPRO programmer as an example, the option bytes can be set by opening the programming option dialog box, as shown in the following figure (see the《MINIPRO instruction manual of programming unit》for detailed operation methods).



29.1 Chip Protection Settings

Protect function of option byte can protect built-in Flash ,user can protect the chip by protection lever setting and ISP password setting. The following protection levels are provided:

Protection level	Name	Description
0	CP0	Without any protection (no password is required for ISP access)
1	CP1	SWD Interface can access chip, password is required for ISP access
2	CP2	Disable access chip by SWD Interface, password is required for ISP access

3	CP3	Disable access chip by SWD and ISP Interface(ISP only provides the function of erasing the whole FLASH (under this protection level, the erasing operation will make the chip 's protection level CP0))

29.2 WDT Setting

Option byte provide interval interruption of WDT, window open cycle, overflow time, CPU sleep setting, CPU debug setting， See detailed meaning on the section of WDT. As shown in the table below:

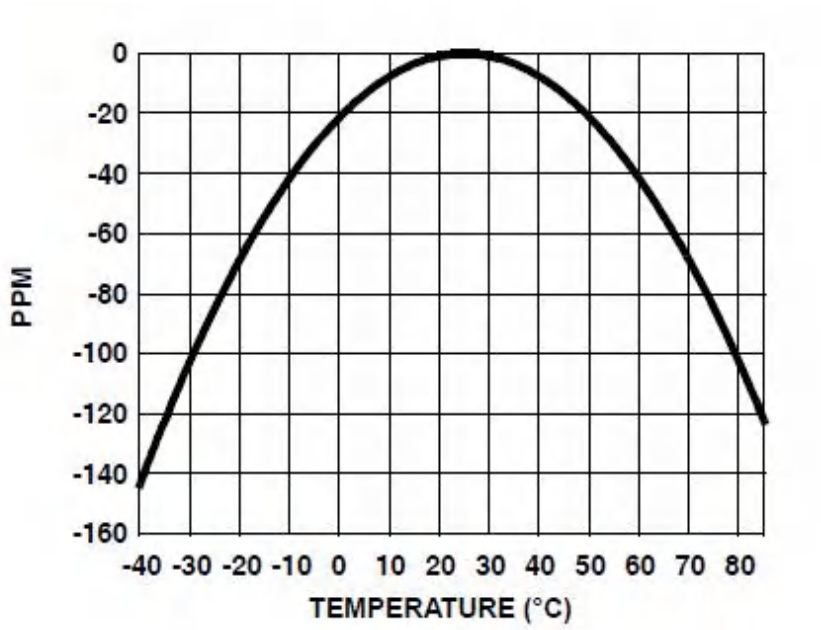
Name	Description	default
Interval interrupt	0：Disable (Disable interrupt of intervals) 1：Enable (When reaches 75% of the spills, interval interrupt occurs)	0
Window open cycle	0：25% 1：50% 2：75% 3：100% During the window open, write 0xBB to WDTE register, watchdog reset and count again; During the window close, write 0xBB to WDTE register, The internal reset signal generate.	3
Overflow time	0：16ms 1：32ms 2：128ms 3：512ms 4：1s 5：2s 6：4s 7：8s	4
CPU sleep setting	0: Disable (When CPU is sleep or deepsleep, WDT is off) 1: Enable (When CPU is sleep or deepsleep, WDT is on)	0
CPU debug setting	0：Disable（When CPU in a state of commissioning, WDT is off） 1：Enable（When CPU in a state of commissioning, WDT is on） Notes: The CPU in the debugging state means that the user stops Cortex M0 through the debugging interface (the PC pointer stops counting).	0

29.3 RTC Setting

The RTC of the SOC has a built-in automatic temperature compensation function that automatically compensates the temperature of the 32k crystal to provide an accurate second pulse output in the range of-25 °C to 70 °C.

Among them, the temperature frequency curve of the crystal as shown below, This is a quadratic curve with a vertex of 25 degrees. (f=f0-alpha*(T-T0)), T0 is 25 degrees). However, The alpha of quadratic curve is different between the high temperature section (25 ℃ ~ 85 ℃) and low-temperature (-25 ℃ ~ 70 ℃), so the option bytes provide separately the parameter RTC_ALPHAL and RTC_ALPHAH ,Each of them is filled with round (alpha * 32768) ,which means rounding operation.

If the choice is high consistency crystals (VT-200-F) provided by Seiko, then ALPHAL = 0x3ee, ALPHAH = 0x4cf.



30 Programming Support

SoC support the built-in programming of the internal FLASH .

It is recommended that customers call the Renergy library function to implement the IAP function ; using the Renergy programmer to complete the ISP function.

30.1 Overview

SoC programming system has the following features:

- ◎ Built in the FLASH content protection mechanisms
- ◎ Supports ISP programming mode;
- ◎ Support IAP programming mode;
- ◎ Support downloads recording mode by SWD;
- ◎ support volume production recording mode;

30.2 Flash Protection Mechanisms

Flash protection is to allow users to enable different levels of security to restrict the access to the on-chip Flash and ISP. Protection mechanisms protect the different level of protection in the following table. Users can set chip protection class by set the “option byte”.

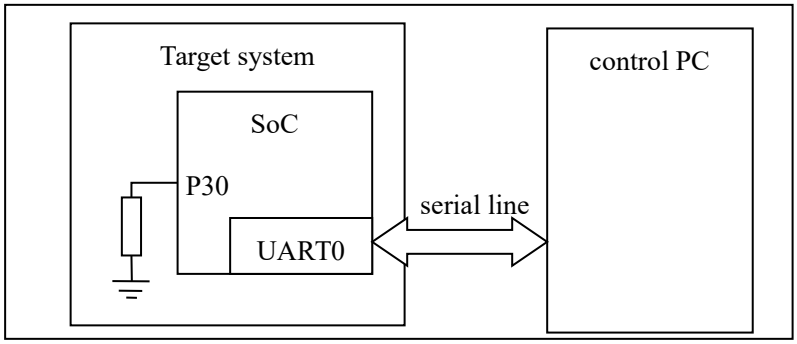
Table 19- 1 The protection level of SoC

Protect level	Name	description
0	CP0	Without any protection (no password is required for ISP access)
1	CP1	SWD Interface can access chip, password is required for ISP access
2	CP2	Disable access chip by SWD Interface, password is required for ISP access
3	CP3	Disable access chip by SWD and ISP Interface (ISP only have the function of the whole erase FLASH (Erase operation will reduce the protection level to CP0 in CP3)
4	CP4	Prohibit access to the chip through the SWD and ISP interfaces (ISP only responds to CMD_UN and CMD_AL commands, the setting of this level of protection needs to be confirmed with the customer and set carefully; when set and burned through the programmer, there is no way to erase, program, or read the FLASH except the IAP interface of the user's code).

30.3 In System Programming (ISP)

The user can pull P30 signal to low, and reset the SoC, let SoC into the ISP mode. ISP mode of connection diagram as shown in figure 18-1.

Figure 18-1 ISP hardware configuration diagram



ISP major process:

1. According to the connection diagram configuration and connect the target system and control host;
2. Reset the target system;
3. Control host configuration of serial port for a start bit, 8 data bits, 1 stop bit;
4. Control the host to send “e”;
5. The target system response “Synchnonized /r/n”;
6. Control the host to send “Synchnonized /r/n”;
7. The target system response “7373(1843)/r/n”;(If the current system frequency is 7.3728M,send 7373;If the current system frequency is1.8432M,send 1843)
8. Control host can perform the corresponding ISP commands according to need;

30.3.1 ISP Communications Protocol

All command of ISP send in the form of a ASCII text. Text use (/r) or (/n) as end mark.

All ISP response is < CR > < LF > the end of the ASCII string sent.

The data were sent and received in the original format (not converted to ASCII).

- Command format

  command parameter0 parameter1 ... parametern/r/n

  {DATA}

- Response format

  Return code/r/n

  Response 0/r/n

  Response 1/r/n

  ...

  Response /r/n

  {DATA}

- Data format

After starting the orders of WM and RM, the data transmission of ISP will start up. The data transmits in a unit of line, and the maximum of 32 bit data in a line is 16(If the number of the data less than 16, the actual number will be sent); Each transmission completes 1 Block (1 Block contains a maximum of 32 rows (less than 32 rows, the corresponding number of rows)) data, and sends a check row (the negative complement of the cumulative checksum of the Block data (calculated in word))。

When chip received a complete block of data, the data will be verified. If the check is passed, send a "OK / r / n" command; If the validation is error or the data packets is illegal, then sent a "RS / r / n" command. If the programmer receives “RS/r/n” command, you need to re-send the Block data.

Forms of data transfer:

When the row data is 0x7e, it means 0x7d, 0x5e sent; when the row data is 0x7d, it means 0x7d, 0x5d sent

Data line format: (B behalf transmit data Byte, hexadecimal)

Table 19- 2 ISP data transmission format

The first row	**1**	**2**	**3**	**4**	**5**	**6**	**……**	**64**	**65**	**The last row**
0x7e	Num	B0	B1	B2	B3	B4	……	B62	B63	0x7e

Check line format: (ASCII code. S represent the cumulative checksum SUM)

Table 19- 3 ISP data validation format

The first row	**1**	**2**	**3**	**4**	**5**	**The last row**
0x7e	0xff	S0	S1	S2	S3	0x7e

30.3.2 SoC resources used

ISP uses the RAM within the range 0x10001000 to 0x10002800 on chip, Stack is located at the top of RAM. Flash can use the RAM within the scope 0x10000000-0x10001000 (4KB) for programming.。

30.3.3 ISP Command

Each ISP command supports specific status code. When receive the undefined command,command processing program sends the return code INVALID_COMMAND.

Command and return code are ASCII format. Only when receives the ISP command execution is completed, the ISP command processor will send CMD SUCCESS, this time the host can send a new ISP commands.

ISP command can be divided into three types:

1. Normal command: Only under the CP0, or CP1, CP2 and password is right, it can be access
2. UN command Under the CP0, CP1, CP2 level of protection (password does not provide), it can be access
3. In any case, FC, AL command can access

Table 19- 4 ISP命令

Command	Instruction	Nature
Baud rate setting	BS <Baud rate> <stop bit>	Normal command
Echo	RD〈switch settings〉	Normal command
Write memory	WM <Address> <Byte size> <Mode>	Normal command
Read memory	RM <Address> <Byte size> <Mode>	Normal command
Flash page erase	FP <Page address>	Normal command
Flash block erase	FS <Block address>	Normal command
Flash chip erase	FC	special command
Flash Block Check Empty	FQ <block address>	Normal command
FLASH Programming	FW <FLASH Address> <RAM Address> <Byte Length	Normal command
Memory Comparison	MC <address 1> <address 2> <byte length>	Normal command
Running	GO <Address>	Normal command
Unlock	UN <password>	special command
Access to confidential	AL	special command

level		
Enable PFPM	PM <switch settings>	Normal command
Reset by software	RS	Normal command
Enable NVM(FLASH)	NV <NVM option>	Normal command

- Baud rate setting

Table 19- 5 ISP Baud Rate Setting Commands

Command	BS <Baud rate> <stop bit>
Input	Baud rate:9600 or 19200 or 38400 or 57600 or 115200 Stop bit:1 or 2
Return code	CMD_SUCCESS or INVALID_BAUD_RATE or INVALID_STOP_BIT or INVALID_PARAM
Annotation	Change ISP communication serial frame format, including baud rate and stop bit. Serial port start bit is 1, data bit is 8. New frame format is effective After return CMD SUCCESSS.
Example	“BS 9600 2” Serial port baud rate will be set as 9600bps, two stop bits.

- Echo

Table 19- 6 ISP Echo Commands

Command	RD <switch settings>
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Command and data echo. Default is on. When echo on, SoC send command and data which to receive back to host.
Example	“RD 0” echo off.

- Write memory

Table 19- 7 ISP Write memory Commands

Command	WM <Address> <Byte size> <mode>
Input	Address: address to start, it should be 32 bits; Byte size: the number of bytes, must be in multiples of four; mode:0 as a serial port,1 as parallel
Return code	CMD_SUCCESS or FM_MODE_ERROR or ADDR_NOT_ALIGN or COUNT_ERROR or COUNT_ERROR or ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	Write data to SRAM
Example	Use the serial port to write 0x12345678 to address 0x10000300:. 1. ASCII code sent: "WM 268436224 4 0" 2. Binary sending: Data line: 7e 04 78 56 34 12 7e Checksum line 7e ff 88 a9 cb ed 7e

- Read memory

Table 19- 8 ISP Read memory Commands

Command	RM <Address> <Byte size> <Mode>
Input	Address: address to read, it should be 32 bits; Byte size: To compare the number of bytes, must be in multiples of four; mode:0 as a serial port,1 as parallel

Return code	CMD_SUCCESS or FM_MODE_ERROR or ADDR_NOT_ALIGN or COUNT_ERROR or COUNT_ERROR or ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	Read the content of SARM of SoC
Example	“RM 268436224 4 0” Read the content which SRAM address is 0x10000300 via a serial port

- Flash page erase

Table 19- 9 ISP Flash page erase Commands

Command	FP <Page address>(FPGA version is 0 to 3071)
Input	Page address: Optional between 0 to 1535
Return code	CMD_SUCCESS or INVALID_PAGE or INVALID_PARAM
Annotation	Erase the content of the specify page of Flash of SoC
Example	“FP 0” Erase the content of the page 0

- Flash block erase

Table 19- 10 ISP Flash block erase Commands

Command	FS <Block address>
Input	Block address: Optional between 0 to 47
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Erase the content of the specify block of EEPROM of SoC
Example	“FS 0” Erase the content of the block 0

- Flash chip erase

Table 19- 11 ISP Flash chip erase Commands

Command	FC
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	Erase all the content of Flash of SOC.
Example	“FC” erase all the content of Flash.

- Flash block blank check

Table 19- 12 ISP Flash block blank check Commands

Command	FQ <Block address>
Return code	CMD_SUCCESS or INVALID_SECTOR or INVALID_PARAM
Annotation	Check if the content of the specify block of EEPROM is empty (Unprogrammed after erase it)
Example	“FQ 1” Check if the content of the 1 block is empty
Command	FQ <Block address>

- Flash Programming

Table 19- 13 ISP Flash Programming Commands

Command	FW <FLASH address> <RAM address> <Byte size>
Input	FLASH address: target address of FLASH to write RAM address: the SRAM address of source buffer Byte size: the number of bytes written(If Byte size is different from number of bytes of Flash page, the rest of this Flash will be set as 0

Return code	CMD_SUCCESS or COUNT_ERROR or SRC_ADDR_NOT_ALIGN or SRC_ADDR_NOT_MAPPED or DST_ADDR_NOT_ALIGN or DST_ADDR_NOT_MAPPED or INVALID_PARAM
Annotation	It is used to program FLASH.
Example	"FW 402653184 268436224 128" copies 128 bytes starting at SRAM address 0x10000300 to FLASH address 0x18000000 (ISP mode, REMAP is 3, FLASH mapped address at this time)

- Memory compare

Table 19- 14 ISP Memory compareCommands

Command	MC <Address1> <Address2> <byte size>
Input	Address1(DST): Starting address of to compare the memory region 1, it should be with the word alignment; Address2(SRC): Starting address of to compare the memory region 2, it should be with the word alignment; Byte size: To compare the number of bytes, must be in multiples of four;
Return code	CMD_SUCCESS or COUNT_ERROR or SRC_ADDR_NOT_ALIGN or SRC_ADDR_NOT_MAPPED or DST_ADDR_NOT_ALIGN or DST_ADDR_NOT_MAPPED or COMPARE_ERROR or INVALID_PARAM
Annotation	This command is used to compare the content of the two regions of memory.
Example	“MC 268436224 268436224 4” Compare 4 bytes data which SRAM address is 0x10000300 with 4 bytes data which SRAM address is 0x10000300

- Running

Table 19- 15 ISP Running Commands

Command	GO <Address>
Input	Address: Address of Code execution start Flash or RAM. This address must be Thumb address
Return code	CMD_SUCCESS or ADDR_NOT_THUMB or ADDR_NOT_MAPPED orINVALID_PARAM
Annotation	This command is used to execute the program in RAM or Flash.Once successfully execute the command, it could no longer return to the ISP command handler.
Example	“GO 5” Jump to address 0 x00000004 to execute

- Unlocked

Table 19- 16 ISP Unlocked Commands

Command	UN
Input	Password:32bit Hexadecimal number
Return code	CMD_SUCCESS or INVALID_PASS or INVALID_PARAM
Annotation	This command is used to unlock ISP.
Example	“UN 567” Enter the password 567 to unlock the ISP

- Access to confidential level

Table 19- 17 ISP Access to confidential level Commands

Command	AL
Input	NC

Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command is used to access to confidential level of ISP
Example	“AL” will return confidential level of SoC

- Enable PFPM

Table 19- 25 ISP Enable PFPMCommands

Command	PM <Switch Setting>
Input	Switch setting: 0 (off) or 1 (on)
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command enables/disables PFPM (Parallel Programming Mode)
Example	"PM 1" will enable the PFPM

- Reset by software

Table 19- 26 ISP Reset by software Commands

Command	RS
Input	NC
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command enable reset by software
Example	“RS” will enable reset by software

- Enable NVM

Table 19- 27 ISP Enable NVM Commands

Command	NV <NVM option>
Input	NVM option:0(Flash)or 1(EEPROM)
Return code	CMD_SUCCESS or INVALID_PARAM
Annotation	This command boots the flash code
Example	“NV 0” Enable Flash write, programming.

30.3.4 ISP Return Code

Table 19- 18 ISP Return Code

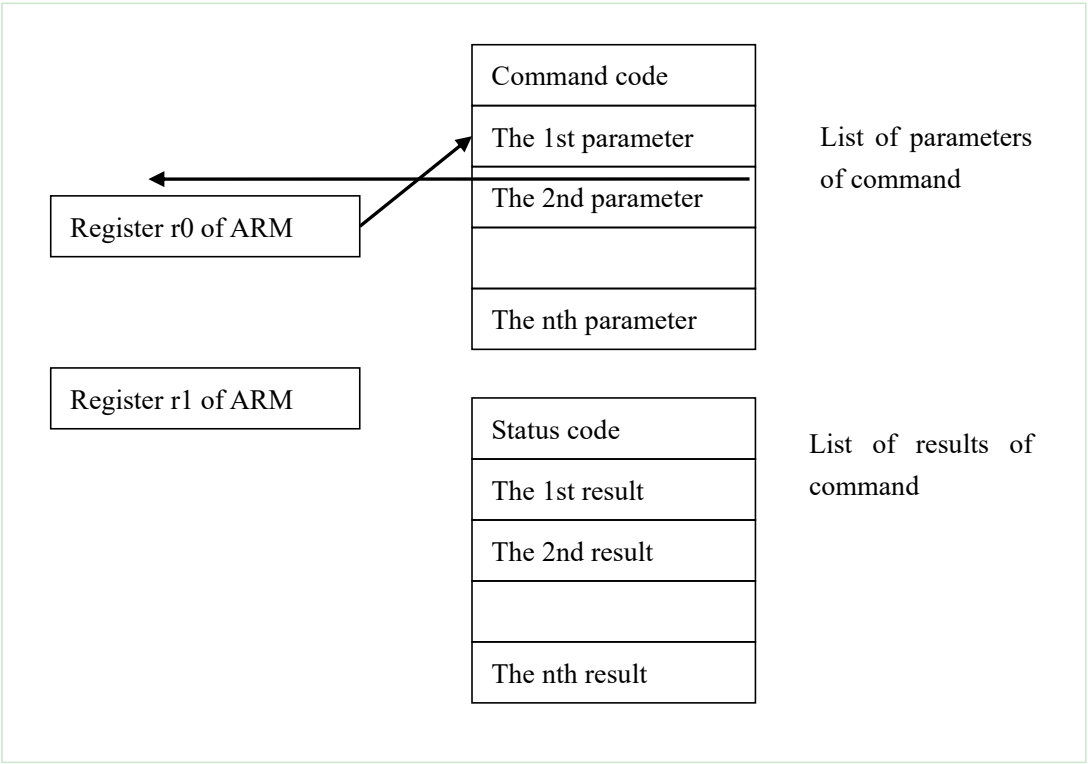
Return Code（ASCII code）	**Mark**	**Description**
0	CMD_SUCCESS	Successfully executed command. Only after successfully executed command, ISP will send this code
1	INVALID_COMMAND	Invalid command
2	INVALID_PARAM	Invalid parameter (ASCII of parameter is not 0-9)
3	INVALID_BAUD_RATE	Invalid baud rate
4	INVALID_STOP_BIT	Invalid stop bit
5	ADDR_NOT_ALIGN	Address is not for boundary with byte
6	COUNT_ERROR	Byte count is not in multiples of four
7	ADDR_NOT_MAPPED	Address have space of crossing the line
8	INVALID_SECTOR/INVALID_PAGE	Invalid SECTOR_NUM or PAGE_NUM

9	SECTOR _NOT_BLANK	SECTOR is not empty
10	SRC_ADDR_NOT_ALIGN	Source address is not for boundary with byte
11	SRC_ADDR_NOT_MAPPED	Source address have space of crossing the line
12	DST_ADDR_NOT_ALIGN	Destination address is not for boundary with byte
13	DST_ADDR_NOT_MAPPED	Destination address have space of crossing the line
14	COMPARE_ERROR	Contrast Error
15	FM_MODE_ERROR	Memory model error
16	ADDR_NOT_THUMB	The address is not Thumb command
17	INVALID_PASS	Wrong password

30.4 In-Application Programming (IAP)

About In-Application Programming, we should call programs of IAP by word pointer in the register r0, the word pointer point to RAM that contains the command code and parameters. Result of IAP command return to results table which register r1 is pointing to. User can give the same value to pointer in the register r0 and r1, so we can reuse the command table to hold the result. Parameter table should be big enough to save all the result. About parameter passing , please see table 18-2. The number of parameters and the results depend on IAP command. “Flash programming”, The maximum number of for command parameters, the number of result is 1. Command processor send status code(INVALID_COMMAND) after receive an undefined command. Program of IAP is Thumb code, address is 0x1800_1c01.

Figure18-2 IAP parameter passing



30.4.1 IAP Command

Table 19- 19 IAP Command

IAP command	Command code	Instructions
Flash page erase	0x50	See the section of ISP

Flash block erase	0x51	See the section of ISP
Flash chip erase	0x52	See the section of ISP
Flash block blank check	0x53	See the section of ISP
Flash programme	0x58	See the section of ISP
Enable NVM	0x5a	See the section of ISP
Analog reset by software	0x5b	See the section of ISP

30.4.2 IAP Usage

The IAP is used in two ways:

- ◎ Online upgrade (update FLASH);
- ◎ Customer data information is updated;

Flash erase/write operations are required for online upgrades.Flash erase/write operations last about 4ms, which increases the processing delay of interrupts occurring during this period.

An IAP implementation:

When users need to implement online upgrade, they need to add a program segment for IAP upgrade in the software design. This program segment implements receiving programs or data from a remote host via a communication port (e.g., UART) and writes these programs or data to the internal FLASH of the SoC using the IAP interface provided by the SoC.

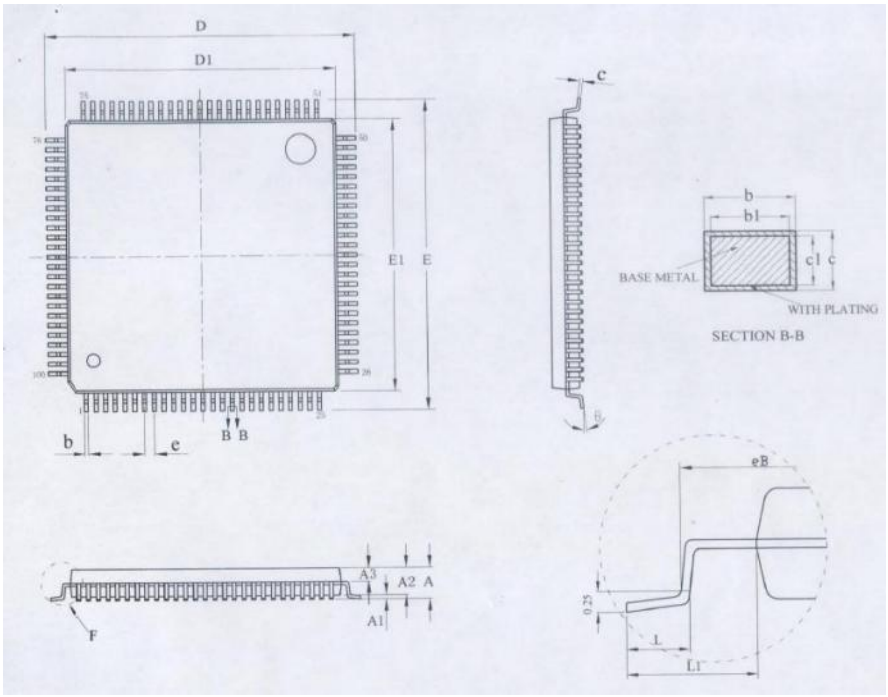
31 Package size and soldering conditions

31.1 Mass production platforms

Renergy provides a variety of programming methods, Specific elaborate can refer to 《RN821x_RN831x Application Note 008 - Programming Platform Usage Instructions》。

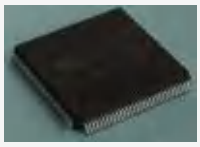
31.2 Package size

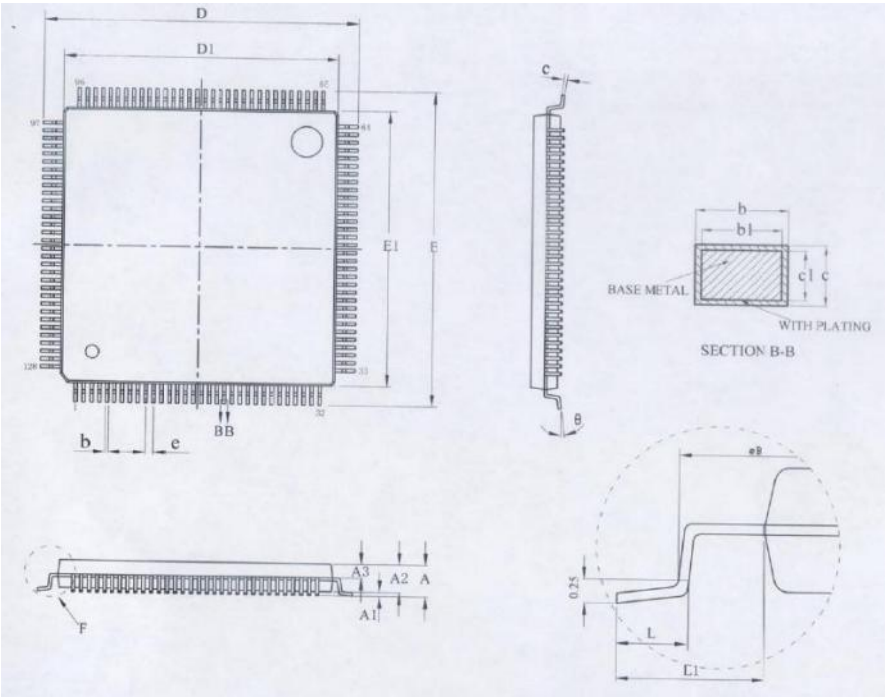
LQFP100L (1414×1.4)		14.00×14.00×1.40	e=0.50



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	---	0.27
b1	0.18	0.20	0.23
c	0.13	---	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20

E1	13.90	14.00	14.10
eB	15.05	---	15.35
e	0.50BSC		
L	0.45	---	0.75
L1	1.00BSC		
θ	0	-----	7°

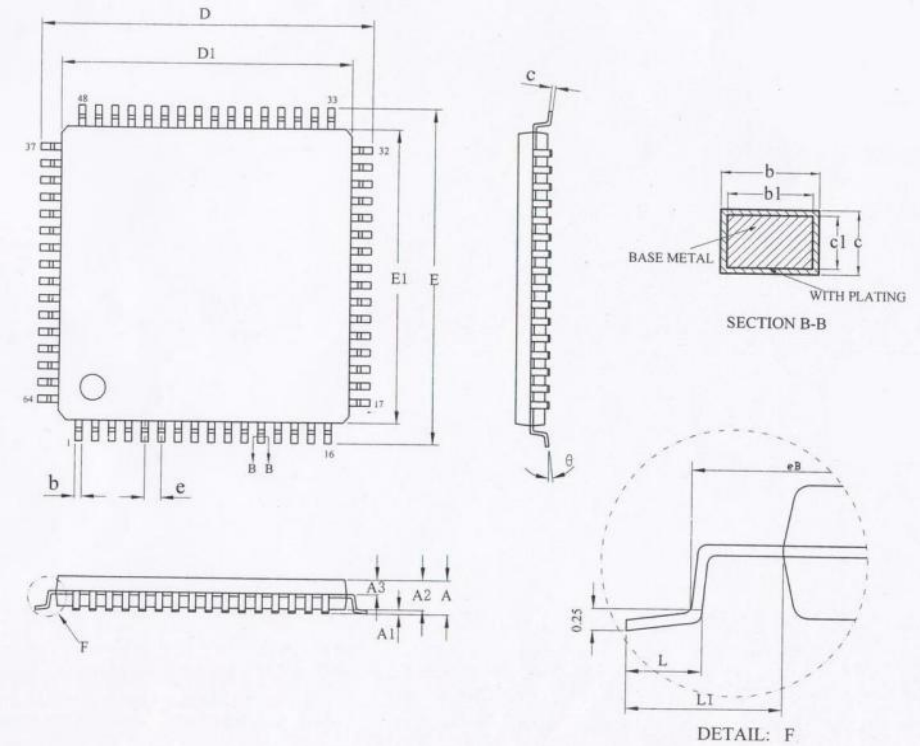
LQFP128L (1414×1.4)		14.00×14.00×1.40	e=0.40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.15	---	0.23
b1	0.14	0.16	0.19
c	0.13	---	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10

eB	15.05	---	15.35
e	0.40BSC		
L	0.45	---	0.75
L1	1.00BSC		
θ	0	-----	7°

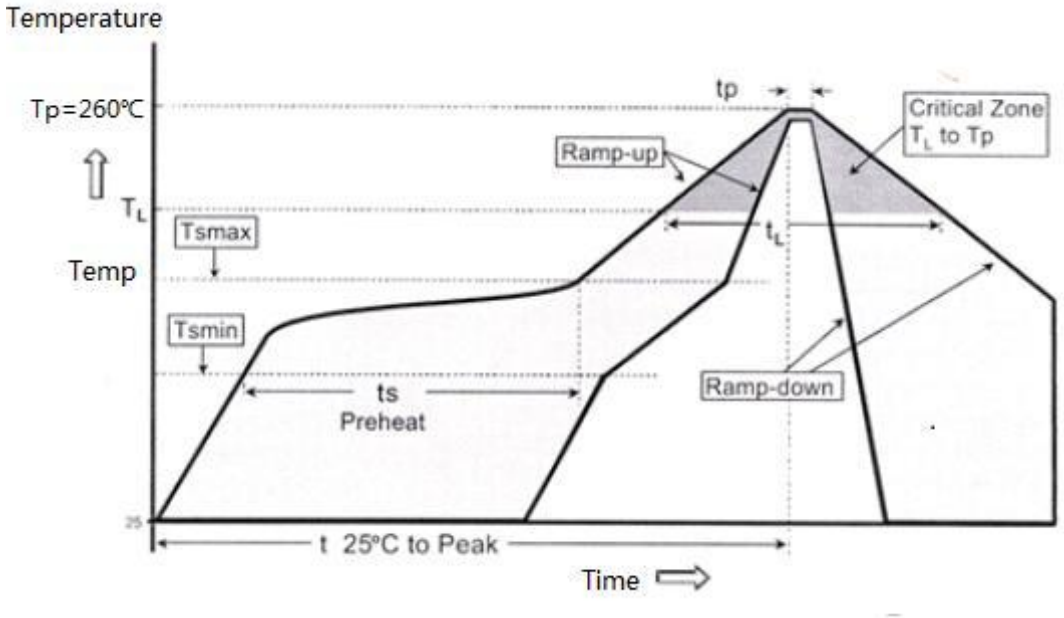
LQFP64L (0707×1.4)		7.00×7.00×1.40	e=0. 40



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.6
A1	0.05	---	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	---	0.25
b1	0.16	0.18	0.20
c	0.13	---	0.18
c1	0.12	0.127	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20

E1	6.90	7.00	7.10
eB	8.10	---	8.25
e	0.40BSC		
L	0.40	---	0.65
L1	1.00BSC		
θ	0	-----	7°

31.3 Reflow oven temperature setting conditions



Temperature setting curve of reflow oven

Distribution map feature	Value
Holding temperature TL Peak temperature Tp Average tilt rate of rise(TL to Tp)	217℃ 260℃ Max 3℃/Second
Warm up Minimum temperature（Ts min） Maximum temperature（Ts max） Time（min-max）（ts）	 150℃ 200℃ 60-180 second
Ts max - TL tilt rate of rise (Ts max to TL)	Max 3℃/Second